High Efficiency Transformerless Interleaved Step- Down Conversion Ratio Dc-Dc Converter

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ABSTRACT:

This project presents, a novel transformerless interleaved high step-down conversion ratio dc–dc converter with low switch voltage stress. In the proposed converter, two input capacitors are series-charged by the input voltage and parallel discharged by a new two-phase interleaved buck converter for providing a much higher step-down conversion ratio without adopting an extreme short duty cycle. Based on the capacitive voltage division, the main objectives of the new voltage-divider circuit in the converter are for both storing energy in the blocking capacitors for increasing the step-down conversion ratio and reducing voltage stresses of active switches. The proposed converter topology possesses the low switch voltage stress characteristic. This will allow one to choose lower voltage rating MOSFETs to reduce both switching and conduction losses, and the overall efficiency is consequently improved.

Keywords: *MOSFET-Metal Oxide Semiconductor Field Effect Transistor.*

I.INTRODUCTION

A DC-to-DC converter is an electronic circuitswhich converts a source of direct current (DC) from one voltage level to another. It is a class of power converter.DC-DC power converters are employed in a variety of applications, including power supplies for personal computers, office equipment, spacecraft power systems, laptop computers, and telecommunications equipment, as well as dc motor drives.The input to a dc-dc converter is an unregulated dc voltage Vg. The converter produces a regulated output voltage V, having a magnitude that differs from Vg. Such electronic devices often contain several sub-circuits, each with its own voltage level requirement different from that supplied by the battery or an external supply (sometimes higher or lower than the supply voltage). Additionally, the battery voltage declines as its stored energy is drained. Switched DC to DC converters offer a method to increase voltage from a partially lowered battery voltage thereby saving space instead of using multiple batteries to accomplish the same thing.

Step down transformers are a standard type of single phase distribution transformers, with primary voltages of 120, 240 or 480 volts and secondaries typically of 12, 16, 24, 32 or 48 volts. They are available in sizes ranging from 50 volt amperes to 10 kilo-volt amperes. Thus the universal range AC supply is step down to our required AC voltage range.

INTERLEAVED BUCK CONVERETER:

Interleaving technique is used in some applications due to its advantages regarding filter reduction, dynamic response, and power management.Using interleaving, the power stage of a converter is divided into several and smaller power stages. Therefore, the size of each component is reduced. With a very high number of interleaved phases, the current stress is greatly reduced and using a different technology becomes a possibility.

This change of technology may bring several advantages:

- power converter is made of surface mount technology(SMT) components;
- automatic assembly;
- absence of heat sinks (usually heat sinks require manual assembly);
- magnetic components can be planar or SMT. Repetitively is greatly increased;
- very small input and output filters

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II. CONVENTIONAL SYSTEM

A. *INTRODUCTION*

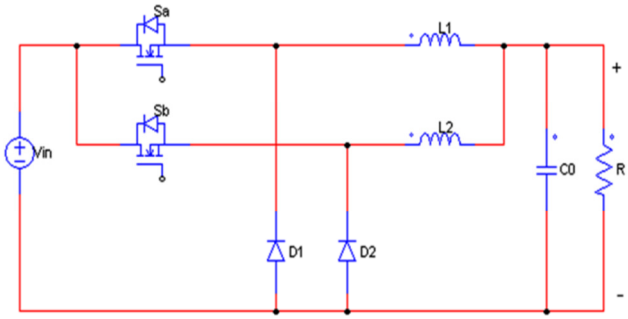

Figure.2.1 Configuration of conventional IBC

The conventional circuit consists of two active power switches, two diodes and two inductors. Conventional IBC shown in Fig.2.1, because active switch devices suffer from the input voltage, high voltage devices rated above the input voltage should be applied. High-voltage-rated devices are generally with poor characteristics such as high cost, large ON-resistance, large voltage drop, severe reverse recovery, etc.

B. *DRAWBACK OF EXISTING SYSTEM:*

The above parameters limit the switching frequency of the converter and impact the power density improvement. For high-input and low-output voltage regulation applications, pursuing higher power density and better dynamics, it is required operating at higher switching frequencies that will increase both switching and conduction losses. Consequently, the efficiency is further deteriorated. Also, it experiences an extremely short duty cycle in the case of high input and low-output voltage applications.

III. PROPOSED SYSTEM

A. *INTRODUCTION*

Recently, high-performance dc–dc converters havebeen called for the increasing high step-down ratios with high output current rating applications, such as VRMs of CPU boards and battery chargers, and distributed power systems. For nonisolation applications with low output current ripple requirement, an interleaved buck converter (IBC) has received a lot of attention due to its simple structure and low control complexity.

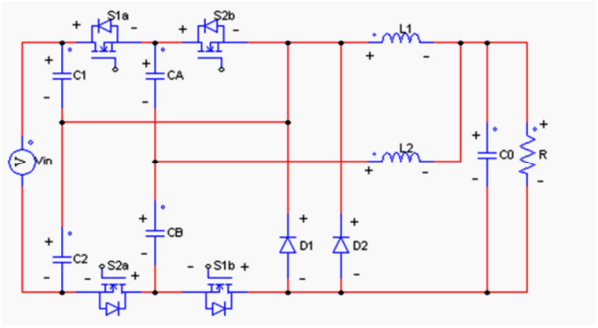

Figure 3.1.configuration of proposed converter

To overcome the drawbacks of the conventional IBC, many step-down converters have been proposed .A quadratic buck converter is synthesized by cascading two dc–dc buck converters which have the voltage conversion ratios of two cascaded converters but with fewer switches. It can operate with wider ranges of step-down conversion ratio than those of conventional single-switch converters without an extremely short duty ratio. However, it operates two cascaded converters and thus processes energy so that the efficiency is worse. A three-level buck converter is proposed to reduce the switch voltage stress to half of the input voltage. By using the aforementioned converter, low-voltage MOSFETs have higher efficiency and better performance compared with the conventional buck converter. However, so many components are required for the use of IBC.

B. *OPERATING PRINCIPLE*

The proposed novel transformerless IBC is shown in Fig. 3.1.From Fig. 3.1, the proposed converter consists of two inductors, four active power switches, two diodes, and four capacitors.

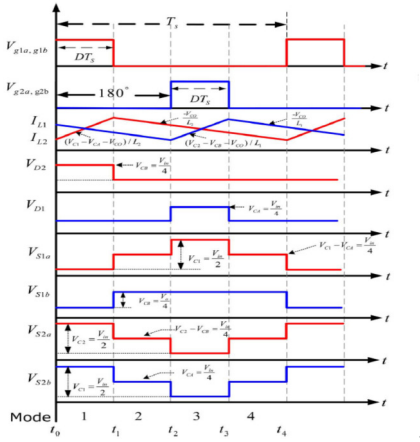

Figure 3.2.Key waveforms of the proposed converter at CCM

The main objectives of the four capacitors are twofold. First, they are used to store energy as usual. Second,based on the capacitive voltage division principle, they are used to reduce the voltage stress of active switches as well as to increase the step-down conversion ratio. Basically, the operating principle of the proposed converter can be classified into four operation modes. The interleaved gating signals with an 180◦ phase shift as well as some key operating waveforms are shown in Fig. 3.3. As the main objective is to obtain a high step-down conversion ratio and as such characteristic can only be achieved when the duty cycle is less than 0.5 and in CCM, hence the steady-state analysis is made only for this case. However, in DCM, as there is not enough energy transfer from the blocking capacitors to the inductors, output capacitors, and load side, and as, consequently, it is not possible to get the charge balance ofthe blocking capacitor, then the nice automatic uniform current sharing property will be lost, and additional current-sharing control between phases should be included under this condition.

C.MODES OF OPERATION

1) Mode 1[t0 < t ≤ t1]:

During this mode, S1a, S1b, and D1 are turned on, while S2a, S2b, and D2 are turned off. Thecorresponding equivalent circuit is shown in Fig. 3.4(a). FromFig. 3.4(a), one can see that, during this mode, current iL1freewheels through D1, and L1 is releasing energy to the outputload. However, current iL2 provides two separate current pathsthrough CA and CB. The first path starts from C1, through S1a,CA, L2, CO and R, and D1 and then back to C1 again. Hence,the stored energy of C1 is discharged to CA, L2, and outputload. The second path starts from CB, through L2, CO and R,and S1b and then back to CB again. In other words, the storedenergy of *CB* is discharged to L2 and output load. Therefore,during thismode, *iL*2 is increasing, and *iL*1 is decreasing, as can be seen from Fig. 3.3. Also, from Fig. 4(a), one can see that VC1is equal to VCA plus VCB due to conduction of S1a, S1b, and D1. SinceVC1 = Vin/2 and VCA = VCB = VC1/2 = Vin/4,

one can observe from Fig. 3.4(a) that the voltage stress of D2 is equal to VCB =Vin/4 and the voltage stresses of S2a and S2bare clamped to VC2 = Vin/2 and VC1 = Vin/2, respectively.

The corresponding state equations are given as follows:

$$L_1\frac{di_{L1}}{dt} = -V_{CO} \qquad (3.1)$$

$$L_2\frac{di_{L2}}{dt} = V_{C1}-V_{CA}-V_{C0}$$
$$= Vcb-Vc0 \qquad (3.2)$$

$$(C_1+C_2)\frac{dv_{C1}}{dt} = -i_{CA} \qquad (3.3)$$

$$C_A\frac{dv_{CA}}{dt} = i_{L2}+ i_{CB} \qquad (3.4)$$

$$C_B\frac{dv_{CB}}{dt} = i_{CA}- i_{L2} \qquad (3.5)$$

$$C_0\frac{dv_{C0}}{dt} = i_{L1}+ i_{L2}-\frac{v_{C0}}{R} \qquad (3.6)$$

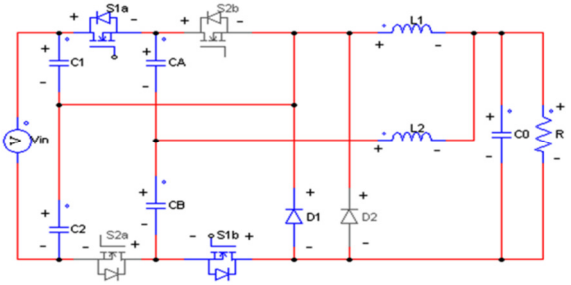

Figure 3.3(a). Equivalent circuit for the proposed converter for Mode 1

2) Mode 2 [t1 < t ≤ t2]:

During this mode, S1a, S1b, S2a, andS2*b* are turned off. The corresponding equivalent circuit is shown in Fig. 3.4(b). From Fig. 3.4(b), one can see that both *iL*1 and *iL*2 are freewheeling through D1 and D2, respectively. Both VL1 and VL2 are equal to −VCO, and hence, iL1 andiL2 decrease linearly. During this mode, the voltage acrossS1*a*, namely, VS1a, is equal to the difference of VC1 and VCA,

And VS1b is clamped at *V*CB. Similarly, the voltage across S2*a*,namely, VS2a, is equal to the difference of VC2 and VCB, and VS2bis clamped at VCA. The corresponding state equations are given as follows:

$$L_1\frac{di_{L1}}{dt} = -V_{CO} \qquad (3.7)$$

$$L_2\frac{di_{L2}}{dt} = -V_{C0} \qquad (3.8)$$

$$(C_1+C_2)\frac{dv_{C1}}{dt} = 0 \qquad (3.9)$$

$$C_A \frac{dv_{CA}}{dt} = 0 \quad (3.10)$$

$$C_B \frac{dv_{CB}}{dt} = 0 \quad (3.11)$$

$$C_0 \frac{dv_{C0}}{dt} = i_{L1} + i_{L2} - \frac{v_{C0}}{R} \quad (3.12)$$

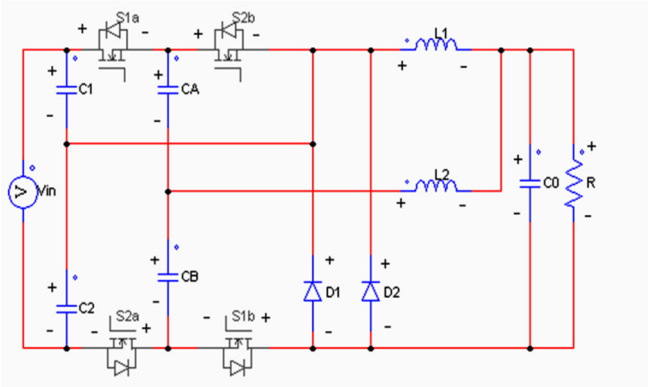

Figure 3.3(b). Equivalent circuit for the proposed converter for Mode2

3) Mode 3 [t2 < t ≤ t3]:

During this mode, S2*a*, S2*b*, and D2are turned on, while S1*a*, S1*b*, and D1 are turned off. The corresponding equivalent circuit is shown in Fig. 3.4(c). From Fig. 3.4(c), one can see that, during this mode, current iL2is freewheeling through D2, and L2is releasing energy to the output load. However, current iL1 provides two separate current paths through CAand CB. The first path starts from C2, through L1, COand R, D2, CB, and S2aand then back to C2 again.Hence, the stored energy of C2 is discharged to CB, L1, andoutput load. The second path starts from CA, through S2b, L1, COand R, and D2 and then back to CAagain. In other words, the stored energy of CAis discharged to L1 and outputload. Therefore, during this mode, iL1 is increasing, and iL2is decreasing, as can be seen from Fig. 3.3. Also, from Fig. 3.4(c), one can see that VC2 is equal to VCA plus VCBdue to conduction of S2*a* and S2*b*. Since VC2 = Vin/2 and VCA=VCB =VC2/2 = Vin/4, one can observe from Fig.3.4(c) that the voltage stress of D1 is equal to VCA = Vin/4and the voltage stresses of S1*a* and S1*b* are clamped toVC1= Vin/2 and VCB = Vin/4, respectively. The corresponding state equations are given as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{in} - V_{C1} - V_{CB} - V_{C0} \quad (3.13)$$

$$L_2 \frac{di_{L2}}{dt} = -V_{C0} \quad (3.14)$$

$$(C_1 + C_2) \frac{dv_{C1}}{dt} = -i_{CB} \quad (3.15)$$

$$C_A \frac{dv_{CA}}{dt} = i_{CB} - i_{L1} \quad (3.16)$$

$$C_B \frac{dv_{CB}}{dt} = i_{CA} + i_{L1} \quad (3.17)$$

$$C_0 \frac{dv_{C0}}{dt} = i_{L1} + i_{L2} - \frac{v_{C0}}{R} \quad (3.18)$$

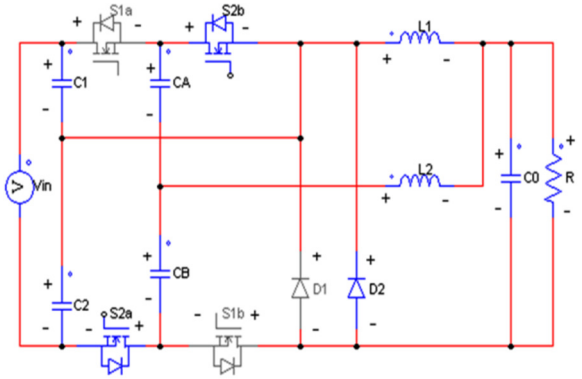

Figure 3.3(c).Equivalent circuit for the proposed converter for Mode 3

4) Mode 4 [t3 < t ≤ t4]:

For this operation mode, as can beobserved from Fig. 3, S1a, S1b, S2a, and S2bare turned off. The corresponding equivalent circuit turns out to be the same as Fig. 3.4(b), and its operation is the same as that of mode 2. From the aforementioned illustration of the proposed converter, one can see that not only the control is very simple but also the operations of two phasesare both symmetric and rathereasy to understand. Also, from the key operating waveforms of the proposed converter shown in Fig. 3.3, one can see clearly the low voltage stress characteristic of four active switches and two diodes as well as the uniform current sharing.

D.STEADY-STATE ANALYSIS

In order to simplify the circuit analysis of the proposed converter, some assumptions are made as follows.

1) All components are ideal components.

2) The capacitors are sufficiently large such that the voltages across them can be considered constant. Also, assume that C1 = C2 and CA = CB.

3) The system is under steady state and is operating in CCM with duty ratio being lower than 0.5 for high step-down conversion ratio purposes.

E. CONTROL STRATEGIES

In all cases, it is shown that the average value of the output voltage can be varied. The two types of control strategies (schemes) are employed in all cases. These are: (1) Time-ratio control, and (2) Current limit control

1) TIME-RATIO CONTROL

In the time ratio control the value of the duty ratio, K= T_{ON}/T is varied. There are two ways, which are constant frequency operation, and variable frequency operation.

2) CONSTANT FREQUENCY OPERATION

In this control strategy, the ON time, is varied, keeping the frequency (F=1/T), or time period T constant. This is also called as pulse width modulation control (PWM). Two cases with duty ratios, as (a) 0.25 (25%), and (b) 0.75 (75%) are shown in Fig.4.6. Hence, the output voltage can be varied by varying ON time.

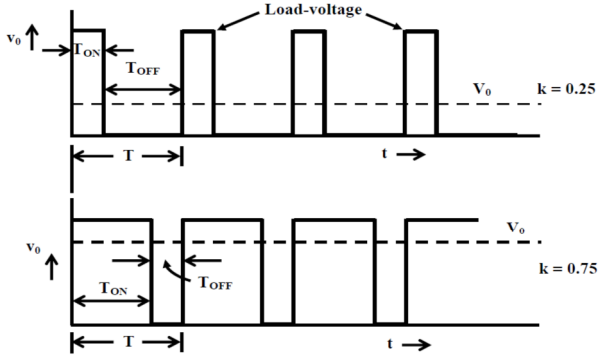

Figure 4.7 Pulse-width modulation control (constant frequency)

IV. SIMULATION OF PROPOSED CONVERTER

The performance of the proposed circuit is verified by theprototype.The IBCsare operated when the duty cycle is less than 0.5.The components are chosen and values are given in Table II.

The specifications of the proposed converter are the following:

i) input voltage of 400 VDC

ii) output voltage of 25 VDC

iii) power rating of 400 W

iv) switchingfrequency of 40 kHz.

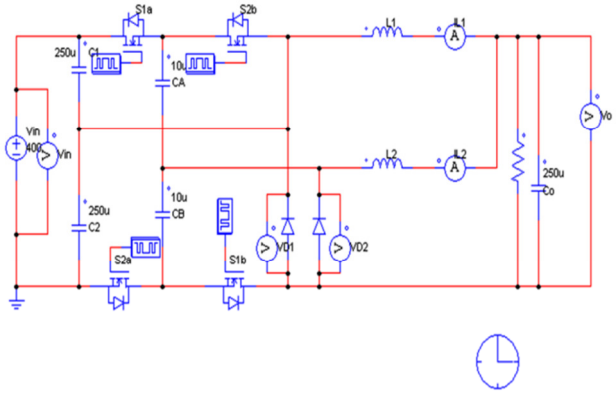

Figure.4.1 Simulation diagram of transformerless interleaved buck converter

TABLE II
COMPONENT PARAMETERS OF THE PROTOTYPE SYSTEM

Components	Specification
Inductors (L_1, L_2)	CM467060, 250μH
Active Switches (S_{1a}, S_{2a}, S_{2b})	IXFH100N25P, 250V, $R_{ds(on)}$=27mΩ
Active Switch S_{1b}	IXFH150N15P, 150V, $R_{ds(on)}$=13mΩ
Blocking capacitors (C_A, C_B)	10uF, 250V (R_c=4.6 mΩ)
Input capacitors (C_1, C_2)	250uF, 250V (R_c=46 mΩ)
Output capacitors (C_o)	250uF, 250V (R_c=46 mΩ)
Power diodes (D_1, D_2)	600V, 60A

A. *SIMULATION RESULTS OF VARIOUS OUTPUT*

1) *simulation output of input dc voltage*

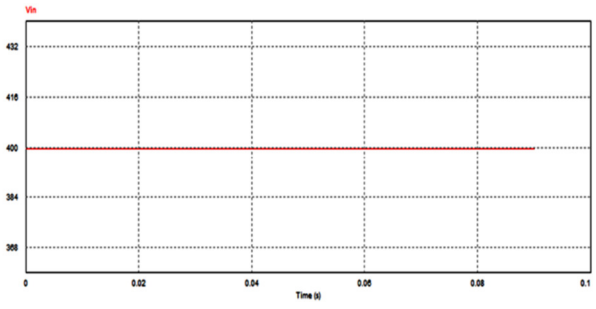

Figure 4.2(a).Waveform of input voltage

In this figure shows the input voltage of 400V dc supply for the proposed system.

2) *simulation output of output dc voltage*

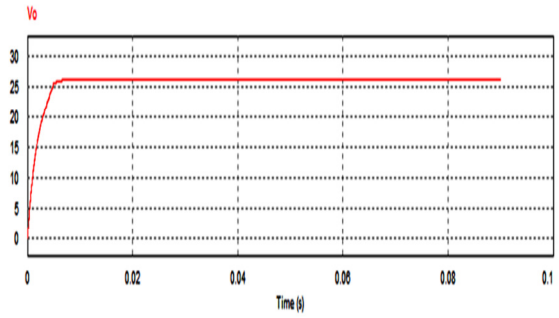

Figure 4.2(b) .Waveform of output DC voltage

This figure shows the constant DC voltage output of 25 volt for the proposed system.

3) simulation output of voltage stresses of v_{d1}voltage

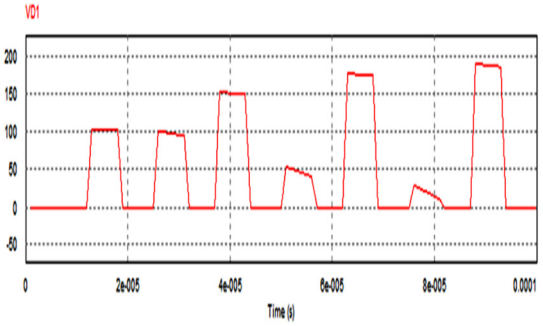

Figure 4.2(c).Waveform of voltage stresses of V_{D1} voltage

4) simulation output of inductor current i_{l1}

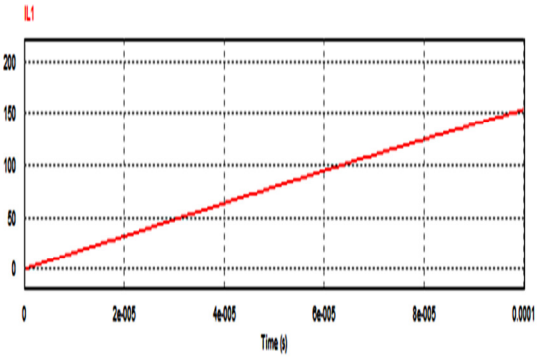

Figure 4.2(d).Waveform of inductor current I_{L1}

5) simulation output of inductor current i_{l2}

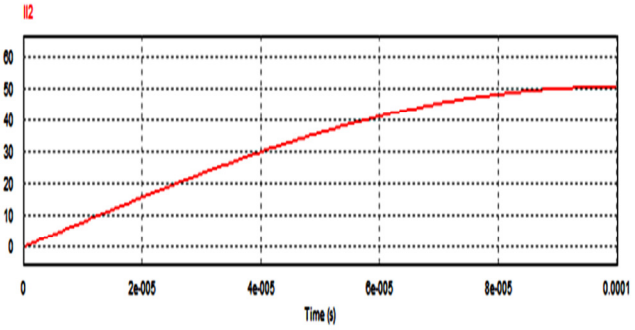

Figure .4.2(e) Waveform of inductor current I_{L2}

B. CONVERSION RATIO FOR VARIOUS DUTY CYCLE

As duty cycle increases the conversion ratio also increases and the output voltage is increases.

Thus the conversion ratio M is calculated by

$$M = \frac{V_0}{4} = \frac{D}{4}$$

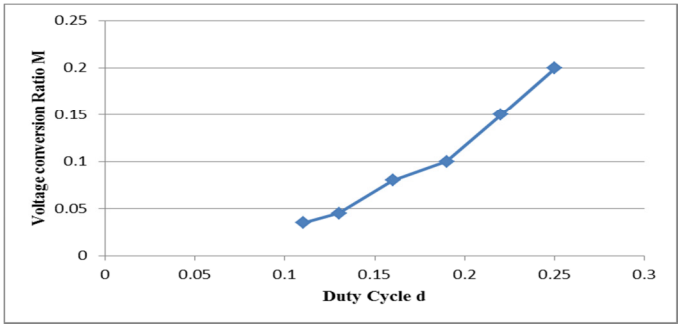

Figure 4.3 Conversion ratio for various duty cycle

C. MEASURED EFFICIENCY FOR VARIOUS INPUT VOLTAGE

Efficiency of the converter is calculated by

$$\eta = \frac{POUT}{PIN} X\ 100$$

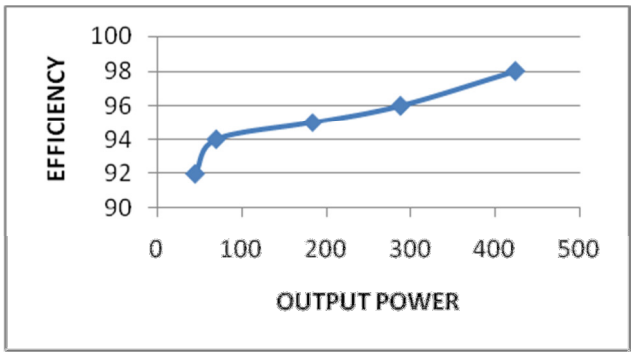

Figure 4.4 Efficiencycurve for various input voltage

The above graph shows the efficiency for various input voltages. As input voltage increases the input power and also the output power increases. Due to that the efficiency of the converter is increased.

V. CONCLUSION

Thus the proposed, a novel transformerless interleaved high stepdownconversion ratio dc–dc converter with low switch voltage stress has been simulated and results are obtained. In this project, two inputcapacitors are series-charged by the input voltage and paralleldischargedby a new two-phase IBC for providing a much higher step-down conversion ratio without adopting an extreme short duty cycle. Based on the capacitive voltage division, the main objectives of the new voltage-divider circuit in the converter are both storing energy in the blocking capacitors for increasing the step-down conversion ratio and reducing voltage stresses of active switches. It will allow to choose lower voltage ratingMOSFETs to reduce both switching and conduction losses, and the overall efficiency is consequently improved. This is very suitable forapplications requiring high step-down conversion ratio.

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