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FAST AND EFFICENT PIPELINING ARCHITECTURE FOR ELECTICAL CAPACITANCE TOMOGRAPHY

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ABSTRACT

The process industry is concerned with the processing of crude resources into other products. Such crudes consist of multiphase components that introduce major challenges to the operators; hence the need for efficient instrumentations that address such challenges is highly desirable. One major need is an early deposit detection system that detects deposit before it builds-up in a pipeline or equipment to prevent any possible hazard.Electrical-capacitance tomography (ECT) is a technique for the non-invasive internal visualization of industrial processes such as mixing, separation and multiphase flow, involving electrically non-conducting mixtures. The emerging electrical capacitance tomography VLSI architecture demands faster operation and hardware scalability.In this paper we present a new architecture of ECT tomography algorithm using FPGA technology. The architecture is flexible enough to host three computationally intensive reconstruction algorithms simultaneous matrix-level and bit level designs was conducted to finely reduce the hardware cost and power consumption.Because of using individual pipelining, the throughput are increased and delay are reduced.

1. INTRODUCTION

Electrical Capacitance Tomography (ECT) is an effective technique to measure a process non-Intrusively by reconstructing the 2D or 3D dielectric distribution of its different constituencies [1][2][3]. This makes ECT a good candidate for several industrial applications such as two-phase flow monitoring, quality control in manufacturing industry, and corrosion detection [4]. In the last few years, several ECT systems have already been suggested [1]. Most of them used a desktop computer as a main processing unit and focused their research mainly on improving the accuracy and execution time of the algorithms on general purpose computers. Nevertheless, the tremendous computation complexity of the tomography algorithms let them to be executed still relatively slowly (in few seconds order), preventing them to sustain real-time applications. Hence, only few research works have been done on designing dedicated hardware architectures for ECT tomography using either DSP processor or FPGA technology. The usage of FPGA instead of DSP processors by other researchers was motivated by the fact that FPGA can host a good portion of the control/data flow of the reconstruction algorithm, without the need of series of sequential memory accesses. Hence, recently, an FPGA-based Electrical Impendence Tomography (EIT) system was disclosed in[4]. Hence, the system could achieve a throughput of around 100 frames/second. The relatively low performance of the system can be

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justified by the fact that the IMMs modules are mainly involved in data acquisition and electric current generation for the electrodes, rather than in the image reconstruction task itself. Another similar FPGA-based ECT device was disclosed to digitally modulate (i.e. amplitude and phase modulations) the ac signal with various carrier frequencies and let the receivers to band-pass filter the transmitted signal to their allocated carrier frequency . This allows simultaneous data acquisition as well as avoiding the usage of CMOS analog switches. Other works were also suggested for FPGA-based image reconstruction targeting other tomography modalities such as computed tomography (CT) and Single-Photon Emission Computed Tomography (SPECT). In [4], a dedicated architecture for SPECT imaging using a scalable multicore onChip Architecture for on-chip communication was proposed. The hardware which consists of 128 processing elements mapped onto an FPGA module could achieve a speed-up by a two orders of magnitude over 2 GHz Intel core 2 Duo Processor by exploring the intrinsic fine parallelism exhibited by the corresponding algorithm. A reconfigurable and modular interconnection switching network was used to dynamically and arbitrarily interconnect the processors array by eliminating data starvation. Other architectures using Graphics Processing Unit (GPU) for SPECT Tomography were also suggested by exploring their significant performance for arithmetically intensive algorithms that have structured data accesses and limited branching, which is the case of SPECT tomography algorithms. However, compared to FPGA, their performance was lower because of the frequency and randomness of memory access which was off-chip The system consists of a 32-bit DSP RISC processor, running at 66.67 MHZ, interfaced with a custom core to perform event timing, energy determination-discrimination, position determination, and coincidence processing in real-time. In this paper, we present a new architecture of ECT tomography algorithm using FPGA technology. The architecture is flexible enough to host three computationally intensive reconstruction algorithms, namely the LBP, Landweber, and modified-Landweber algorithms. It explores some of the new features of recent FPGA devices such as the DSP blocks and the Block RAM (BRAM). A simultaneous matrix-level and bit level designs was conducted to finely reduce the hardware cost and power consumption, while keeping the overall execution of the algorithms low. To the best of the authors' knowledge, this is the first embedded system which explores the intrinsic parallelism which is available in modern FPGA for ECT tomography. Extensive simulations indicate that the proposed architecture achieves a speed-up of up to three orders of magnitude over the software version when the reconstruction algorithm runs on 2.53 GHZ-based Pentium processor

2 ECT HARDWARE IMPLEMENTATION

Electrical capacitance tomography (**ECT**) is a method for determination of the dielectric permittivity distribution in the interior of an object from external capacitance measurements. It is a close relative of electrical impedance tomography and is proposed as a method for industrial process monitoring, although it has yet to see widespread use. Potential applications include the measurement of flow of fluids in pipes and measurement of the concentration of one fluid in another, or the distribution of a solid in a fluid.

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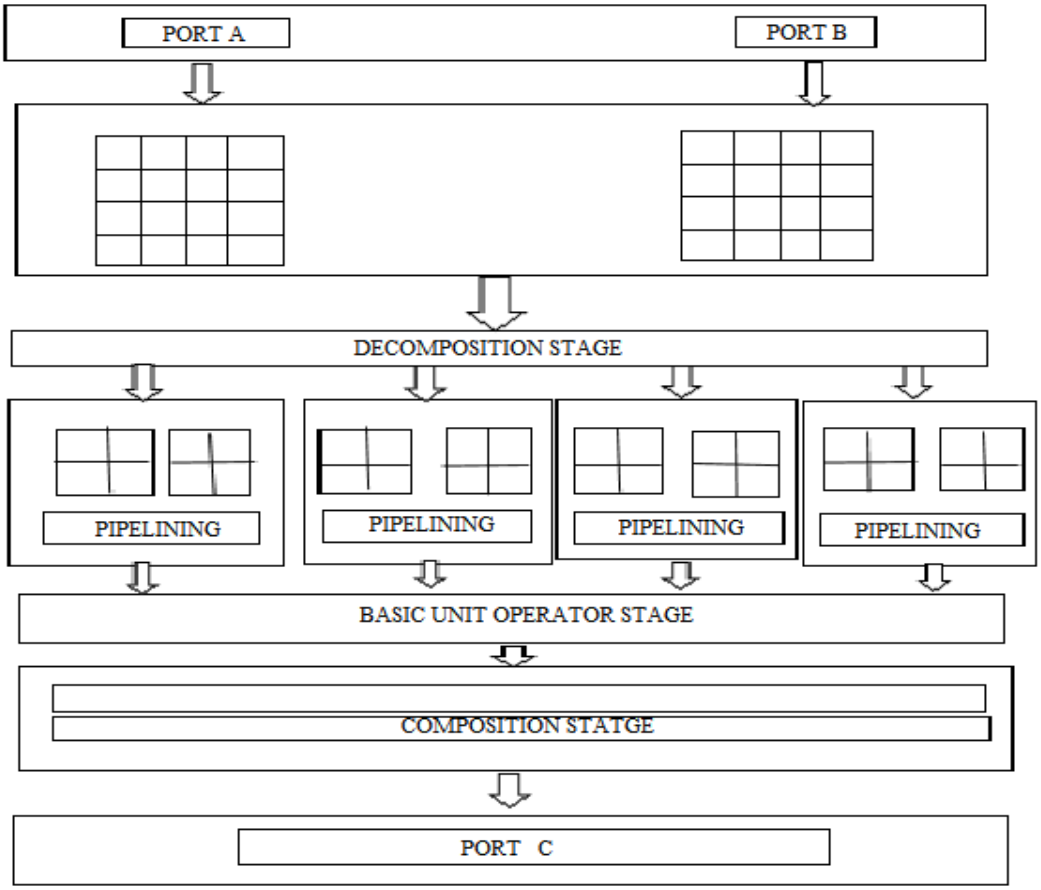
Although usually called tomography, the technique differs from conventional tomographic methods, in which high resolution images are formed of slices of a material. The measurement electrodes, which are metallic plates, must be sufficiently large to give a measureable change in capacitance. This means that very few electrodes are used and eight or twelve electrodes is common. An N-electrode system can only provide N(N−1)/2 independent measurements.. However, ECT is fast, and relatively inexpensive.

BLOCK DIAGRAM



2.2 STAGES

The parallel processing module is a parallel like architecture which is composed of several similar adder/multiplier processing units .Each of these units is scalable and consists of three pipelined stages:

- Decomposition stage
- Basic unit operation
- Composition stage

2.2.1 DECOMPOSITION STAGE

The matrix decomposition consist to divide the two matrices to multiply into regular square blocks (q×q) which are then simultaneously processed by the parallel processing units using bit decomposition techniques .The matrix level decomposition ,a bit

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level decomposition take place. For the three afro-mentioned algorithms, the matrix decomposition consists to divide the two matrices to multiply into regular square blocks (q * q) which are then simultaneously processed by the parallel processing units using bit decomposition techniques

2.2.2 BASIC UNIT OPEARATION STAGE:

A basic operator consists of a set of registers, R basic, two (p+1)) bit multipliers, one adder, and a multiplexor.

Each operation takes four inputs. The outputs from the multipliers are added for the final output, (p+2) bit elements of the working sub matrix are loaded in order into registers.

The basic unit operator stage in matrix level covers decomposition stage in bit level, basic unit operation stages in bit level; add composition stage in bit level as described in below. The overall operations in basic unit operation stage. Port A and port B are the input ports of the k-processing unit

2.2.3 COMPOSITION STAGE:

The composition unit consists of registers and an adder tree with 0-mp adders. At the input of the composition unit, a finite set of data (i.e., equal to the number of basic operators) is available at each *T* basic. At the basic operators and the composition unit interface, the number of registers needed is equal to the total

3. VERIFICATION AND RESULT

PARAMETE R	EXSISTING TECHNIQUE	PROPOSED TECHNIQUE
TIMING SUMMARY	4.639ns for each block	5.324ns for entire block
MEMORY SPACE	477128 kilobytes	418248 kilobytes

4. CONCLUSION

This paper presented a VLSI implementation of the ECT algorithm using FPGA chip (Virtex XC7VX1140T). An analysis of our implementation regarding the quantization effect caused by finite bit widths indicates that 18 - 24 bits are enough to generate less than 15 % relative error. The hardware explored the implicit parallelism for matrix multiplication. Its advantage is that it is flexible to accommodate various bit-widths and image sizes, in addition to consume less power since the most significant bits of the sensitivity matrix are usually equal zero. In order to achieve 1 pixel per clock cycle throughput, a new pipelined architecture was suggested. Extensive simulations indicate that the proposed architecture achieves a speed-up of up to three orders of magnitude over the software version when the reconstruction algorithm runs on 2.53 GHZ-based Pentium processor.This performance was achieved using an array of [2×2] × [2×2] processing units. This satisfies the real-time constraint of many industrial applications

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