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IMPLEMENTATION OF MUX DESIGN IN ON CHIP COMMUNICATION NETWORK

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ABSTRACT:
As a high performance on-chip communication method,the code division multiple access (CDMA) technique has recently been applied to network on chip (NoCs). Network on Chip (NoC) has been proposed to address the scalability, reliability issues of on chip communication. However, conventional packet switched NoC suffer from nondeterministic transmission latency and limited opportunities for parallel data transfer, since multiple flows cannot get through a link at the same time. To resolve these problems, the Code Division Multiple Access technique as an effective method for implementing high performance on-chip communication was applied to NoC. To reduce the delay of the NoC, we implement the multiplexer using AND operation in the encoder and decoder. In the transmitter module, source data from various sender is individually encoded with an orthogonal code of a standard basis by using multiplexer, this different coded data is mixed into one. After that, through the on chip communication infrastructure the sums of data can be transmitted to their destinations. In the receiver module, by taking an XOR operation between the sums of data and the corresponding orthogonal code a sequence of chips is retrieved. Finally, original data can be reconstructed. This method achieves 56.11% less delay, 11.21% area saving and achieves maximum throughput than the existing one.

INTRODUCTION:

The Network-on-Chip (NoC) concept has mostly used technique of diffi cult System-on-Chip (SoC) designs for handling the large on-Chip communication requirements [1]. A traditional Intellectual Property (IP) blocksare collide with each other to communicate over the shared bus based interconnection scheme that does notscale well to very large SoCs. To route the information between IP blocks and it results achieve a very largebandwidth, delay and power within the chip by using the packet-switching paradigm. The previously proposedCDMA NoCs based on a digital encoding and decoding method and it requires spreading codes with orthogonalcodes. To this end, the standard basis code is typically used. However, the Standard Basis Code (SB) encodingand decoding method has disadvantages, which are given as follows.

. Data loss: While transferring data parallel between the transmitter and receiver, data will collideand it will cause data loss and fi nally result in transmission delay also. The proposed system is to eliminate this data loss and the resulting transmission delay. To address the aforementioned weakness, we proposed a Standard Basis (SB) Encoding/Decodingmethod, which outperforms the Standard Basis encoding/decoding method. The SB encoding/decoding method can be applied to any CDMA NoCs to improve their performance. The rest ofthis brief is organized as follows. In Section 2 and 3, wedetail the SB encoding/decoding method and formally prove its correctness. The simulation resultsand comparisons between the previously proposed Standard Basis method and the newly proposed standard basis method.

PROPOSED WORK:

2.1. Code Division Multiple Access (CDMA) Network Onchip (NOC)

A new standard based encoding and decoding method to force the cost and performance of Code Division Multiple Access (CDMA) Network on Chip in delay, area and network throughput is proposed. In the transmittermodule, source data from varies senders are individually encoded with an orthogonal code of a standard basisand by using multiplexer these coded data are mixed together. After that, through an on chip communicationinfrastructure the sums of data can be transmitted to their destinations.

In the receiver module, by taking an XORoperation between the sums of data and the corresponding orthogonal code a sequence of chips is retrieved.Finally, original data can be reconstructed.In this figure 5, Parallel-to-Serial (P2S) module, Serial-to-Parallel (S2P) modules, Network Interface (NI),Programmable Element (PE). A Programmable Element executes the application tasks and data's are divided byusing network interface from Programmable Element into packets and reconstruct data flows by using packetsfrom Network-on-Chip (NoC).

In the sender, via a Parallel-to-Serial (P2S) module packets from Networkinterface are switched to a bit stream [7]. This bit is joined with some code words. By using addition module,the coded data from varies

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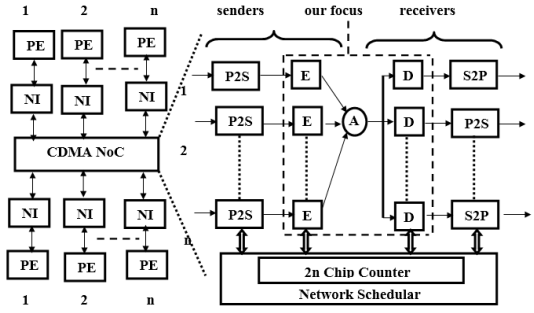
encoding modules are joined together. Then, the outputs of data's are transferredto receivers. In the receiver, using sums of data from transmitter, original data is reconstructed. Then thesecontinuous bit streams are transmitted to packet flits by Serial to Parallel (S2P) modules. Finally, these packet flits are transferred to Network interface. Finally, these packet flits are transferred to Network interface. CDMA is an example of multiple access, where several transmitters can send information simultaneously over a single communication channelThis allows several users to share a band of frequencies (see bandwidth). To permit this without undue interference between the users, CDMA employs spread spectrum technology and a special coding scheme (where each transmitter is assigned a code). CDMA is used as the access method in many mobile phone standards



2.2. Standard Basis (SB) Encoding Scheme

The *n* number of inputs of data is collected from n number of sources. These n number of collected signalsare given as input to the encoder in bit-by-bit manner. Consider a code word is X bit. By using PN sequencegenerator in this code word is generated. The input signal is separated into n bits by taking AND operation usingmultiplexer with X as code word. In AND operation "When both input's are '1' then output will be '1'

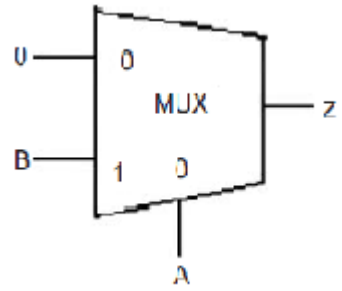


Fig 1: mux using and operation

2.3. Standard Basis Decoding Scheme

When the binary sum signal arrives at receivers, multiplexer operation is taken between the binary sum and thecorresponding orthogonal code in chip-by-chip manner. Then, the result chips are sent to an accumulator. Afterm-chips are accumulated (m is the length of the orthogonal code), the output value of the accumulator will bethe corresponding original data.
Note that there is always only one chip equal to 1 and all other chips are equal to 0 for an orthogonal code in standard basis.Hence, the maximal accumulated value in the Standard Basis accumulator is 1 and it can bestored in a 1-bit register.

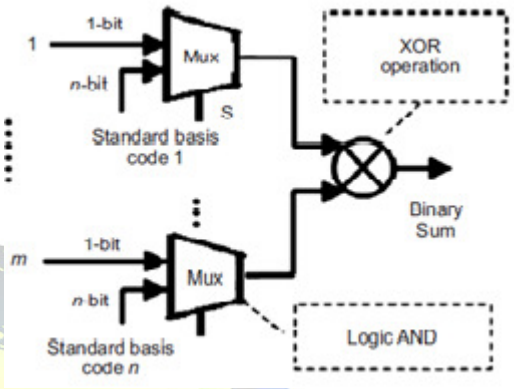


Fig: 2 standard basis encoding process

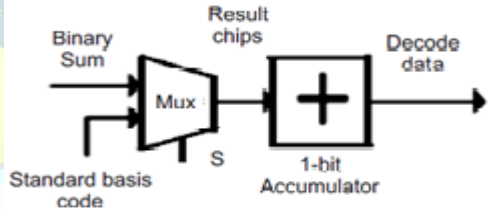


Fig :3 standard basis decoding process

Therefore, in the Standard Basis decoding module, only one gate and an accumulatorwith one 1-bit register are used, resulting in less logical resources.thesame as like that, we can perform *n*number of operations with an n number of gates. For example, in fi gure7consider input data is 0, standard basisspreading code word is 1 and the select line is 1. When Input has given of bits to the encoder. There multiplexerwill perform AND operation and produces an outputs. The same operation will be taken in n encoders .Both ofthe outputs will be mixed together by taking an multiplexer XOR operation .The resulting output is in binaryas 0 or 1.The binary output result will be given as input of decoder. In decoder, this dummy data is converted into original user friendly format. If spreading code word ofdecoder is same as the spreading code of encoder then perform AND operation.
The resultant output will beapplied to the accumulator, which performs XOR operation and produces the result. Finally, the output is sameas the input data .By using multiplexer for performing AND and XOR operation it will reduce the data

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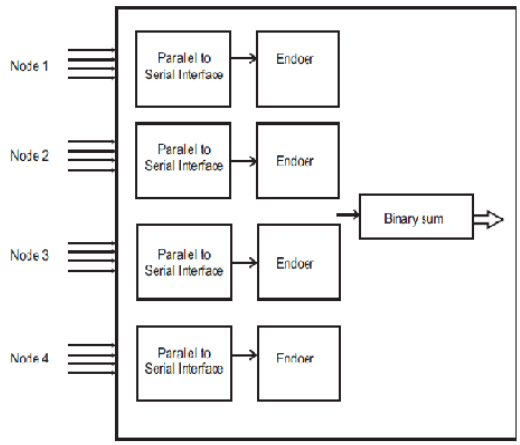
transferdelay and area size. A multiplexer is a circuit that accept many input but give only one output. The technique oftransmitting multiple signals over a single medium is called multiplexing. It is used for digital applications, alsocalled digital multiplexe, is a circuit with many input only one output. By applying control signals, we can steerinput to the output. Multiplexer are used in various fi elds where multiple data need to be transmitted usinga single line. Multiple signals can be isolated and eventually, the desire signals reach the intended recipients.By performing multiple data transfer we can achieves high timing. Mainly we used multiplexer instead of ANDgate, it has very low number of gates because of that it occupies very less area and for data transferring also ittakes very less timing.

NETWORK SCHEDULAR:

In the Code Division Multiple Access Network-on-Chip (NoC), network scheduler receives the transmittingrequests from senders and assigns proper spreading codes to the senders and requested receivers. Note thatall-zero code word is assigned to nodes having no data to transmit/ receive.Moreover, when there are multiplesenders requesting the same receiver, the scheduler will apply an arbitration scheme, for example, round-robin.The chip counters calculate how many orthogonal chips are used in one encoding/decoding operation.Each node needs two chip counters, one for the sender and the other for the receiver. Note that packet flitsfrom Network Interface can also be transformed to multiple bit streams in the Parallel-to-Serial(P2S) moduleto make tradeoffs between power/area cost and packet transfer latency, and the scheduler should provide abit-synchronous scheme to maintain the orthogonally of the transmitted channels.



Four bits of Data from many nodes are given to parallelto serial interface and encoded. The resulting output are added and then transmitted. The receiver decodes the data and sent to serial to parallel interface. Finally the decoded data is delivered to the nodes. Figure 8 has four nodes each and every nodes are primaryinputs. Each packet contains Data, source node address and destination node address.

For example taking node1four bits as input bits and node 3 four bits as output bits. Those source and destination bits are kept in a packet.When Input has given of four bits from node 1 to Parallel to serial interface. The parallel to serial interface willselects one out of four bits from right to left and will transfer it to the encoder. And the encoder will performAND operation between the received bit from parallel to serial interface and data bits.The above said operation to be performed in node with received output from this node 2 operation to be added with the node 1thisoutput to be given as an input in decoder and this has to be decoded with data bits. The result will be transferredto accumulator and this will perform XOR operation with each and every bits and it will produce single bit as output. These same operations to be performed for the remaining bits in the node1and the fi nal output are equal to the input.

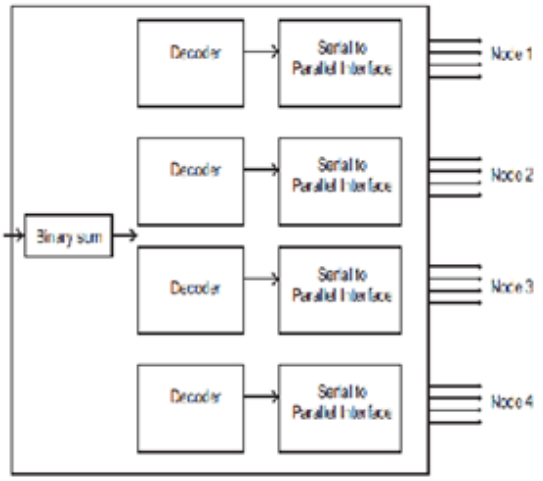


Fig 4: block diagram of proposed system

SIMULATION RESULT:

The simulation results for the comparison of Standard basis encoding and decoding with AND gate and Standardbasis encoding and decoding multiplexer using AND operation is using Xilinx ISE Simulator as shown infi gure. A network is implemented in verilog with 6,8 and 16 nodes. Synopsys DC with a 40mm standard celllibrary is used to synthesize the delay and area consumption results.

CDMA Encoder/Decoder Power and Area cost:

We compare the power and area cost of the two encoding/decoding methods. Here, encoder and decoder besidesits chip counters are taken into consideration.Normally chip counters are implemented by using registers. Thereare 6, 8 and 16 nodes, the standard basis code with AND gate length

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is p and new standard basis code lengthis q respectively. In table 2 it shows, area and power consumption of encoder/decoder. From the table, wecan easily fi nd out the best performance. Power value =Maximum power achieves from the both decoder and encoder of existing method - Maximum power achieves from the both decoder and encoder of proposed method/Maximum power achieved.

COMPARISION OF CDMA NETWORK ON CHIP:

By using two encoding/decoding schemes we have compared the performance of CDMA Network on Chips.Besides the decoder module and encoder module, other on-chip modules, such as parallel-to-serial modules,serial-to-parallel modules and network scheduler are all included in the Network on Chips. we can find that the New Standard Basis code with multiplexerusing AND operation Code Division Multiple Access Network on Chip (CDMA NoC) has lower area, delay and power cost than the existing standard basis Code Division Multiple Access Network on Chip. Since both NoCs contain the parallel-to-serial module, scheduler module, and serial-to-parallel module, the percentage of power and area saving of the new code division multiple access, is as much as the previously calculated Standard basis code. However, the SB CDMA NoC still gains 14.10% – 25.27% power saving and 18.25%– 2 4.11% aresaving..Throughput = No of output bits X Maximum Operating Frequency.

CONCLUSION:

In this paper, Standard Basis Code Multiplexer using AND operation for an on chip interconnection networkhas been presented. Standard basis codes are used to modulate the packet data to handle a large number ofparallel data transfer. Compare to the the existing standard basis code method, the proposed standard basiscode of CDMA approach provides reduction in delay, power, and area and achieves maximum throughput. AStandard Basis Code Multiplexer using AND operation for an on chip achieves very less delay than the existingmethod. In proposed method low number of gates is used than the existing method. So, it occupies less areathan existing one. Normally multiplexer is used in many areas for data transferring. Multiplexer sends digitalor analog signals at higher speed on a single line in one shared device. The Standard Basis Code Multiplexerusing AND operation for an on chip interconnection network (NoC) performance is improved than the existing
standard basis code method.

FUTURE WORK:

Future work includes Design of Low Power & Reliable Networks on Chip through Joint Crosstalk Avoidance and Multiple Error Correction Coding.

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