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BROADBAND TRANSMISSION OVER RESIDENTIAL POWER LINES EMPLOYING VDSL2: THE IMPEDANCE MATCHING ANALYSIS

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ABSTRACT

Bridging and Transmission of VDSL2 broadband over power lines has received considerable attention recently to cater to broadband distribution within the premises of a residence. Powerline, that often already exist to support energy distribution, can provide aneconomical broadband medium for high-speed reliable communication traffic,forsupporting the smart home technology. The low-voltage electrical network provides anunfriendly environment for data communications. Besidesinterferences, noise, attenuation, and multi-path reflections, theextremes as well as the unpredictability of the access impedanceare limiting factors in the performance of PLCs.Power lines are fundamentally different from telephone lines both in topology and load impedance. Power lines have a thicker gauge and shorter straight lengths, apart from a large number of bridge taps (BT) with inductive load terminations, which are not matched to line impedances.Although there are many impedance matching techniques, but one of the biggest problems they face is their static nature i.e. they are designed to match a particular load. Due to time varying nature of residential loads a static impedance matching circuit fail to achieve its purpose.

This paper presents a preliminary study about a possible methodology of designing an optimal broadband impedance matching proceduresfor providing gain equalization and mitigation of the effects of low-impedance loads on the PLC modem in a wide frequency range.

Key words—Impedance matching, powerline communication (PLC).

I. INTRODUCTION

Powerline communication (PLC) exploits the existing power delivery network to convey data information signals. The communication medium exhibits high frequency selectivity due to mismatching effects from discontinuities andunmatched loads. A highly frequency-dependent behavior is also shown by the line impedance, i.e., the impedance at the transmitter port or at the receiver port [1]. The transmitter is coupled to the line via a capacitive coupler (to eliminatethe dc or ac mains signal) and a transformer to provide galvanicisolation. Furthermore, impedance matching has to be implemented to maximize the signal transfer into the powerline. Matching networks were considered in the PLC literature, showing benefits in terms of an increase of the received signal power [1]–[2]. However, from a communication perspective, it is important to maximize the signal-to-noise ratio (SNR) atthe receiver side and not only the signal power [4]. Impedancematching is relevant also in radio communications systems, asdiscussed in [5]. Furthermore, the effective formulation of theSNR is in terms of signal amplitude rather than in terms ofpower, although the two quantities are related once the receiverimpedance is given. In PLC, the maximum power transfercondition does not imply the maximization of the SNR becausepower matching may turn into a higher noise contribution as itwas found in [4] in which the problem of designing the optimalreceiver impedance was addressed.In this brief, we turn our attention to impedance matching at the transmitter side, and we study the effect of three main criteria to impedance design: A) complex conjugate matching, which is the most commonly used method in transmission lines for maximum power transfer [7]; B) equal impedance matching in which the voltage reflected wave from the line input to the generator is minimized [8], [9]; and C) voltage maximization matching in which

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the voltage at the line input is maximized. In this brief, we will show that Method C) is optimal for the maximization of the SNR at the receiver side.In Section II, we describe the impedance matching criteria deriving the input–output signal relations. The SNR at the receiver port is studied in Section III. Since the line impedance is highly frequency selective, assuming transmission in the broad frequency range of 2–100 MHz, we also propose the usage of simplified impedance matching methods in SectionIV. In Section V, SNR and capacityperformanceresults are shown using measured channel responses and line impedances in an in-home PLC scenario. [6] presented a brief outline on Electronic Devices and Circuits which forms the basis of the Clampers and Diodes.

II. ADOPTED IMPEDANCE MATCHING METHODS

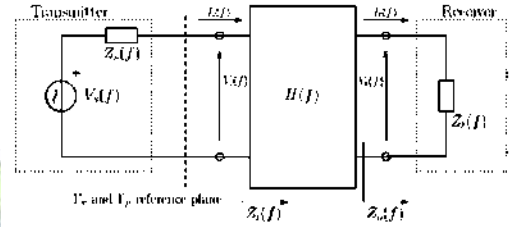

Fig. 1. Equivalent circuit for a system.

An equivalent model for the PLC link between a transmitter and a receiver is depicted in Fig. 1. The transmitter comprises the voltage source $V_s(f)$ with an internal impedance Zs(f). The voltage $V_i(f)=V_s(f)-I_i(f)Z_s(f)$ is applied at the input port of the PLC network. The receiver front-end has an impedance $Z_r(f)$ so that the received signal voltage is

$V_r(f)=I_r(f)Z_r(f)$ .....(1)

where$I_r(f)$ is the current at the receiver load. The relation between the input and output voltages and currents can be obtained by using the ABCD matrix H(f) [10] associated to the two-port network as follows:

$V_i(f)=A(f)V_r(f)+B(f)I_r(f)$ $I_i(f)=C(f)V_r(f)+D(f)I_r(f)$..... (2)
In (2), the adopted ABCD matrix sees the outgoing direction for the current toward the load, as reported in [11]. This choice allows us to retrieve a positive voltage at the load $V_r(f)$ when $Z_r$is fed by the current $I_r(f)$. Furthermore, the input line impedance $Z_i(f)$, i.e., the impedance seen at the input port of the channel (looking toward the load), can be obtained as
$Z_i(f) = V_i(f) / I_i(f)$
$Z_i(f) = [Z_r(f)A(f)+B(f)]/[Z_r(f)C(f)+D(f)$.. (3)

The input impedance depends on the receiver impedance $Z_r(f)$. In the following, we assume $Z_r(f)$ to be set to a fixed value. It is clear that, to maximize the voltage amplitude at the receiver port, given a constraint on the source voltage $V_s(f)$, the input voltage amplitude $|V_i(f)|$ must be maximized. In turn, $V_i(f)$ depends on the choice of the source impedance $Z_s(f)$, i.e., on the impedance matching criterion as discussed hereinafter,since

$V_i=V_s(Z_i/Z_i + Z_s)$.....(4)

where we have dropped the dependence on frequency to ease the notation. Furthermore, the impedance matching criterion determines the value of the active power at the input port computedas

$P_i = Re\{V_iI^*_i\}= (|V_s|^2R_i)/(|Z_i + Z_s|)^2$..... (5)

In the following,we will denote the real part and the imaginary part of the impedance with R and X, respectively, e.g., the source impedancewill be denoted as $Z_s= R_s+ jX_s$.
A. Complex Conjugate Matching (Method A)

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In this approach, the source impedance is designed to minimize the power reflection coefficient [7] calculated at the reference plane highlightedin Fig. 1 and defined as

$\Gamma_p = (Z_i - Z^*_s)/(Z_i + Z_s)$..... (6)

Thus, for minimizing Γ_p, the transmitter impedance Z_s must satisfy the following condition:
$Z_s = Z^*_i$.....(7)
Then, the voltage and the active power at the input port read as
$V_{i,A} = V_s [Z_i/ 2R_i]$ $P_{i,A} = [|V_s|^2/ 4R_i]$..... (8)

It should be noted that, differently from our scenario, this criterion assures maximum power transfer to the load Z_i when Z_s is constrained while Z_i can be varied.

B. Equal ImpedanceMatching (Method B)

In this method,it is necessaryto introducethevoltagereflectioncoefficientΓv calculatedatthechannelinputport,asshown in Fig. 1. The voltage reflection coefficient is defined as
$\Gamma v = V_-/V_+$,
whereV_- is the voltage wave reflected by the load and V_+ is the incident voltage wave to the load [8]. In the designof radio systems, this parameter is rendered as low as possible, thus eliminating the reflected voltage wave and preventing the source damage. By exploitingthe telegraph equations
$V_i = V_+ + V_-$
$I_i = (V_+ - V_-)/Z_s$ .....(9)
and after some manipulation, we can write the voltage reflection coefficient as expressed in [9] and here reported with the notation of Fig. 1

$\Gamma_v = Z_i - Z_s Z_i + Z_s$..... (10)

Therefore, to obtain $\Gamma_v = 0$, the matching condition is simply $Z_s = Z_i$. It follows that the input voltage and power become
$V_{i,B} = V_s/ 2$
$P_{i,B} = |V_s|^2(R_i/ 2|Z_i|^2)$..... (11)

C. Voltage Maximization Matching (Method C)

The two previous criteria do not assure maximum voltage amplitude at the input port. To do so, the choice of $R_s = 0$ and $X_s = -X_i$ assuresmaximumvoltageamplitudeandactive power as it can be understood by looking at (4). Therefore, if the imaginary part of the generator impedance is the opposite of the load one and the real part is zero, the input voltage and active power will read as

$V_{i,C} = V_s (1+j(X_i/R_i))$ $P_{i,C} = (|V_s|^2/R_i)$... (12)

It follows that with this matching criterion, the input active power is four times the one achieved with Method A, whereas it is twice the one in MethodB if the input impedanceis real. It should be noted that in this matching method, the magnitude of the voltage reflection coefficient (10) can be greater than unity since the conditions reported in [9] apply. Furthermore, the magnitude of the power reflection coefficient defined in (6) is one. To solve this issue, a practical implementation that protects the transmitter from the reflected waves can deploy an isolator as proposedin [11].

III. VOLTAGE AND SNR AT THE RECEIVER

The voltage at the receiver port can be written as
$V_r = V_i(A+(B/Z_r))^{-1}$.....(13)
Substituting the value of $Z_r$computedwith (3), it is possible to express the load voltage V as a function of Z_i. Moreover, it is possibletowritetheinputvoltageV_i as afunctionofthe source voltage V_s and the matching

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impedance Z_s by applying (4). After some algebraic manipulation, the voltage at the receiver can be expressed as

$V_r=V_i/ (A + B(Z_iC-A)/(B-Z_iD))$
$=V_i(Z_iD-B) / \Delta_H Z_i$
$=V_s(Z_iD-B)/\Delta_H(Z_i+Z_s)$.....(14)
where Δ_H is the determinantof the ABCD matrix H.

A. SNR at the Receiver

The performance of the communication system depends on the SNR at the receiver. The SNR is defined as the ratio of the power spectral density (PSD) of the signal of interest and the PSD of the total noise components at the receiver as detailed in [4]. The noise components to be considered in a PLC network comprise the following: 1) active noise generated by devices connected in certain nodes of the network; 2) noise generated by the resistive components of the network; and 3) noise generated by the resistive components of the receiver load. In principle, all noise components at the receiver port depend on both the source impedance Z_s and the receiver impedance Z_r. However, the resistive noise components are negligible with respect to the active noise component. Furthermore, once Z_r is fixed, the effect of a change in $Z_s$to the active noise at the receiver node is negligible due to the decoupling between the two ports introduced by the complex PLC network. Therefore, the SNR can be simplified into the following expression:
$SNR(f)=[|V_s(f)|^2/|V_n(f)|^2][|Z_iD-B|^2/|\Delta_H(Z_i+Z_s)|^2]$..(15)
whereV_n denotes the noise voltage and all quantities are frequencydependent.

CONCLUSION

An increasing interest has raised around PLCs over the last decade, due to the fact that they can provide an economical solution for the home networking. However, powerlines present an extremely harsh environment for the transmission of high-speed wideband signals. The frequency-dependent and time varying impedance of the channel, which is affected by the loads connected to the network, is one of the major problems. It leads to mismatch between the modem impedance and the network load impedance, causing low reliability of the whole system.

This paper discusses on design optimization procedure such as i) *Complex Conjugate Matching ,ii) Equal Impedance Matching, iii) Voltage Maximization Matching* forthe mitigation of the effects of low-impedance loads on the PLC modem in a wide frequency range. The proposed methodology is efficient and robust, leading to coupling units capable of maximizing the level of the transit signals in the prescribed frequency range. The voltage maximization method (Method C) ensures data rates exceeding 1.53Gbps with a probability of 80% while exceeding 1.42Gbps when matching is done to a constant reference impedance profile. It has also been shown that in complex PLC networks the optimal source impedance matching doesnot depend on the receiver impedance.

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