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FPGA SIMULATION OFACCESS TIMER, HEAD TIMER, PAY LOAD TIMER AND DATA MUX MODULES OF BLUETOOTH TRANSMITTER

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ABSTRACT

This paper presents FPGA simulation ofAccess Timer,Head Timer, Pay load Timer and Data Mux modules of Bluetooth Transmitter. Bluetooth is a universal short range radio link and is designed to provide low-cost and robust networking. Our Bluetooth transmitter is designed in Verilog -hardware description language (HDL) and is implemented in to FPGA. So, performed top level functional verification and debugging as well as detailed subsystem simulations of all the modules. This paper presents the development of Access Timer,Head Timer ,Pay load Timer and Data Mux modules of Bluetooth Transmitter. The prototyping board equipped with Xilinx Spartan-3E FPGA device is used for hardware evaluation of system design. For simulation part, Xilinx ISE Design Suite 14.2 is used as the simulation tool and architecture was implemented by Verilog. The proposed system has been validated for different sub-modules with simulation results.

Keywords— FPGA Simulation; Bluetooth; Transmitter;Spartan3E ;Xilinx ISE

I. INTRODUCTION

Bluetooth is a short-range wireless communication standard designed with an intention of replacing cables connecting portable and desktop devices and build low cost networks for such devices. Bluetooth operates in the ISM band (2.4 GHz –2.48 GHz) with GFSK (Gaussian Frequency Shift Key) modulation. The operating band of 83.5 MHz is divided into 1 MHz spaced Channels, each signaling data at 1 MSPS [1].Bluetooth provides point-to-point connections, ad-hoc networking capabilities. Bluetooth specification details how the technology works and how specific applications work to ensure interoperability. Due to the unrestricted nature of the ISM band, Bluetooth must overcome interference from other systems and minimize its interference on other systems. Bluetooth does this by using a Frequency Hopping Spread Spectrum (FHSS) technique. This spreads the RF power across the spectrum which reduces interference and the spectral power density [2].

Bluetooth is a combination of hardware and software technology. The hardware is riding on a radio chip. On the other hand, the main control and security protocols have been implemented in the software. By using both hardware and software, Bluetooth has become a smart technology for efficient and flexible wireless communication system. Bluetooth radio chip supports communication among a group of electronic devices [3].Bluetooth establishes ad-hoc voice and data connections and operates in the 2.4 GHz unlicensed ISM band. Its specification is open and royalty-free. The symbol rate is 1 Ms/s to exploit a maximum available channel bandwidth of 1 MHz. Fast frequency hopping is applied to combat interference and fading. A shaped, binary FM modulation is applied to minimize transceiver complexity [4].

II. IMPLEMENTED SYSTEM MODULE

The simulation module shown in Fig 1 consist of various sub modules and it can be divided in to 4 different groups like in group 1- Access FIFO, Head Info, PayLd FIFO, Access Timer, Head Timer, PayLd Timer, in group 2-DataMux and state machine controller, in group 3-ByteTiBit, Preamble Trailer ,HECGen, CRCGen and in group 4 only one module i.e. SerialDataMux .As it is not possible to show the simulation results of all these modules in this paper, only some selected modules in group-1 i.e. Access timer,Head timer and Pay

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load timer and in group 2-DataMux are simulated here and their results are presented. So, remaining modules of group 1, 2, 3 and 4 will not be discussed further in this paper.

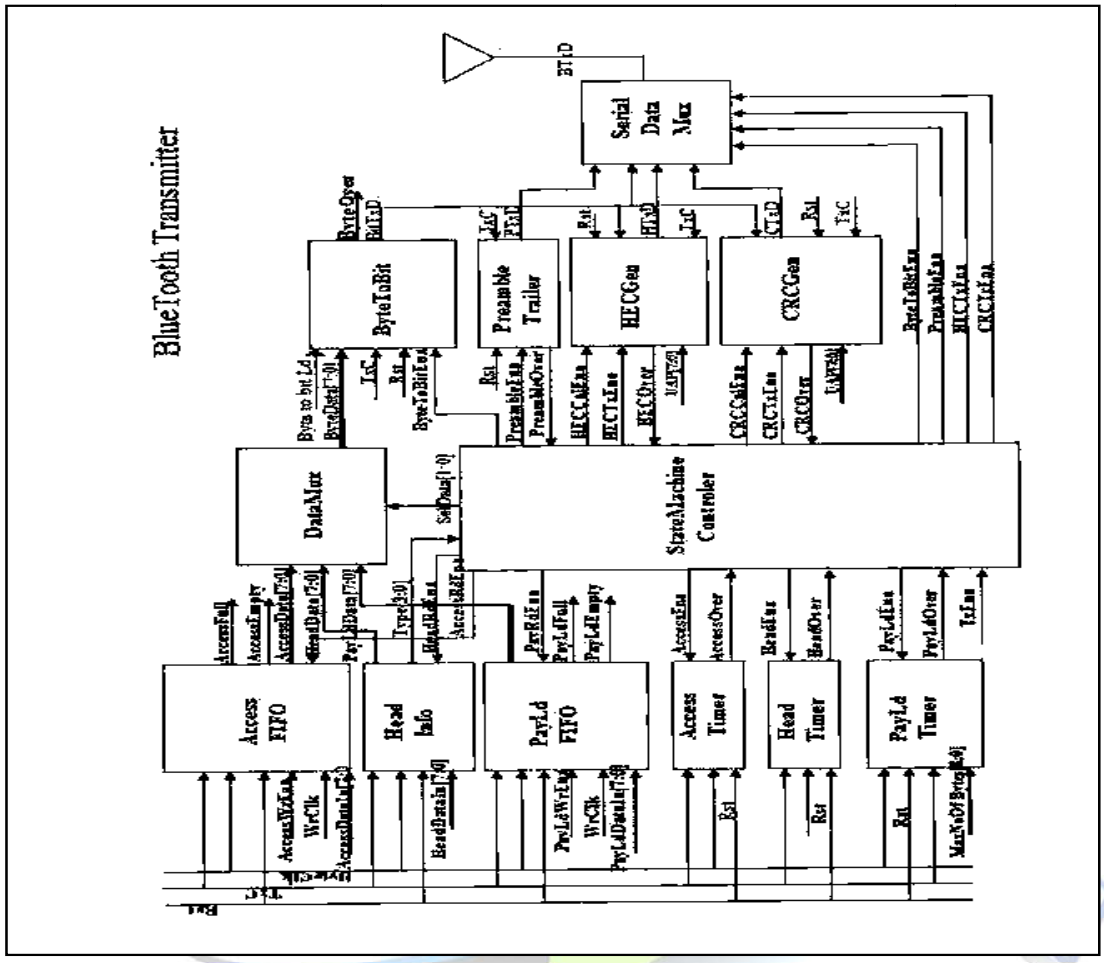

Fig. 1 Simulated Bluetooth transmitter module

III. FPGA SIMULATION AND SIMULATION RESULTS

Field Programmable Gate Arrays (FPGA) can be used in Digital Signal Processing and Communication Systems providing various advantages like multimillion gate counts, massive parallelism capabilities, in memory reduction, and circuit complexity reduction etc. FPGA chip can be reprogrammed many times in the matter of second depend on the need of designer. Spartan3E field programmable gate array (FPGA) is used as an implementation platform to verify the design. The Spartan-3E FPGA family offers the low cost and platform features you're looking for, making it ideal for gate-centric programmable logic designs. Sparatan-3E is the seventh family in the groundbreaking low-cost Spartan Series and the third Xilinx family manufactured with advanced 90nm process technology. Spartan-3E FPGAs deliver up to 1.6 million system gates, up to 376 I/Os, and a versatile platform [6].In this prototype, we have used pure hardware implementation by using VHDL (VHSIC hardware description language) to describe the hardware architecture in FPGA.[7].The prototyping board equipped with Xilinx xv200e target device, along with cs144 target package at a target speed of -6 was used in a FPGA device for hardware evaluation of system design. For simulation part, Xilinx ISE Design Suite 14.2 is used as the simulation tool and architecture was implemented by Verilog. [5] proposed a system which can achieve a higher throughput and higher energy efficiency. The S-BOX is designed by using Advanced Encryption Standard (AES). The AES is a symmetric key standard for encryption and decryption of blocks of

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data. In encryption, the AES accepts a plaintext input, which is limited to 128 bits, and a key that can be specified to be 128 bits to generate the Cipher text. In decryption, the cipher text is converted to original one. By using this AES technique the original text is highly secured and the information is not broken by the intruder. From that, the design of S-BOX is used to protect the message and also achieve a high throughput, high energy efficiency and occupy less area.

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3.1 Access Timer

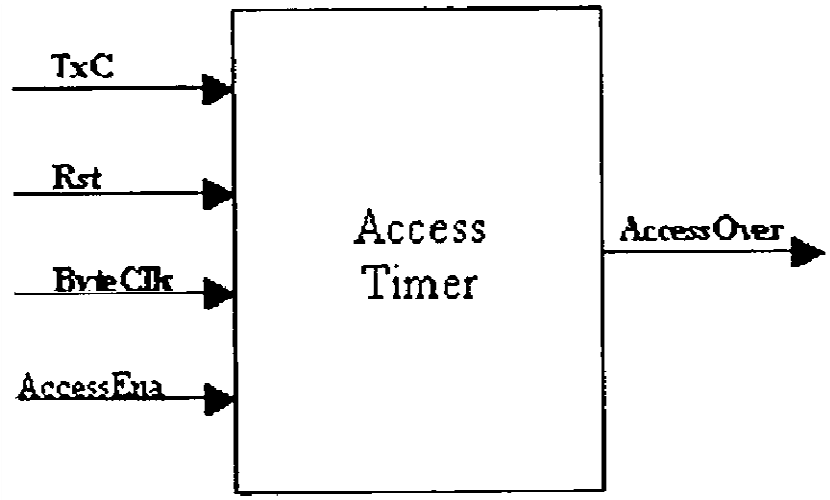

Fig. 2 Access Timer

SIGNAL DESCRIPTION

S.No.	Part name	Mode	Description
1.	TxC	Input	Synchronizing clock
2.	Rst	Input	It initializes all internal registers
3.	ByteClk	Input	Write Clock for Access FIFO
4.	AccessEna	Input	Enables the Timer to Count
5.	AccessOver	Output	Indicates that the FIFO is Full

DESCRIPTION:

It is the timer which counts the no. of bytes being written in the FIFO. Access timer is shown in Fig.2 and simulated waveforms are shown in Fig.3.

Simulation Result

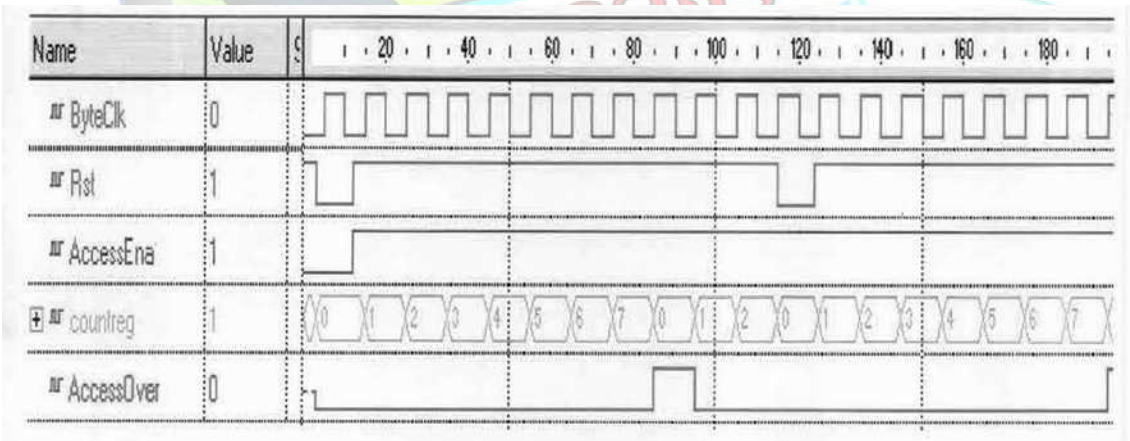

Fig. 3 Simulation waveforms of Access Timer

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3.2 Head Timer

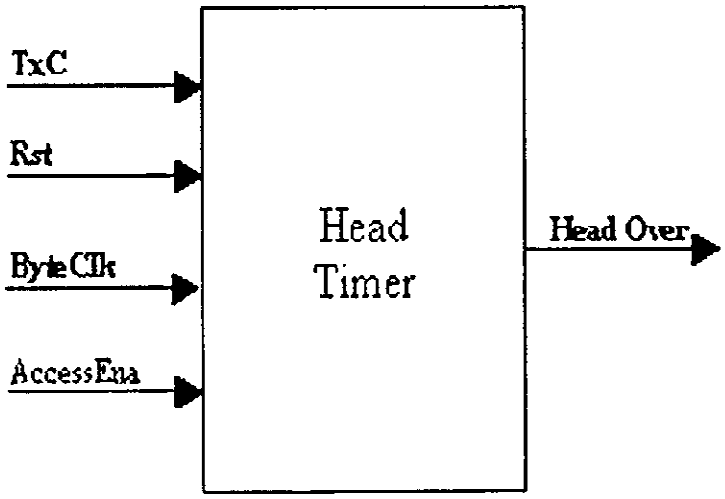

Fig. 4 Head Timer

SIGNAL DESCRIPTION

S.No.	Part name	Mode	Description
1.	TxC	Input	Synchronizing clock
2.	Rst	Input	It initializes all internal registers
3.	ByteClk	Input	Write Clock for Access FIFO
4.	HeadEna	Input	Enables the Timer to Count
5.	HeadOver	Output	Indicates that the FIFO is Full

DESCRIPTION:

It is the timer which counts the no. of bytes being written in the header register. Head Timer is shown in Fig.4 and simulated waveforms are shown in Fig.5.

Simulation Result

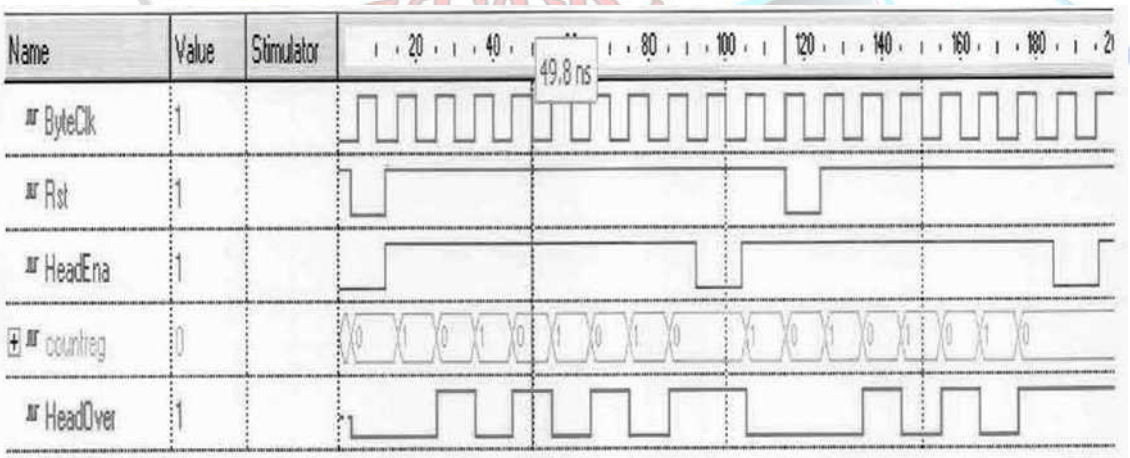

Fig. 5Simulation waveforms of Head Timer

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3.3 PayLd Timer

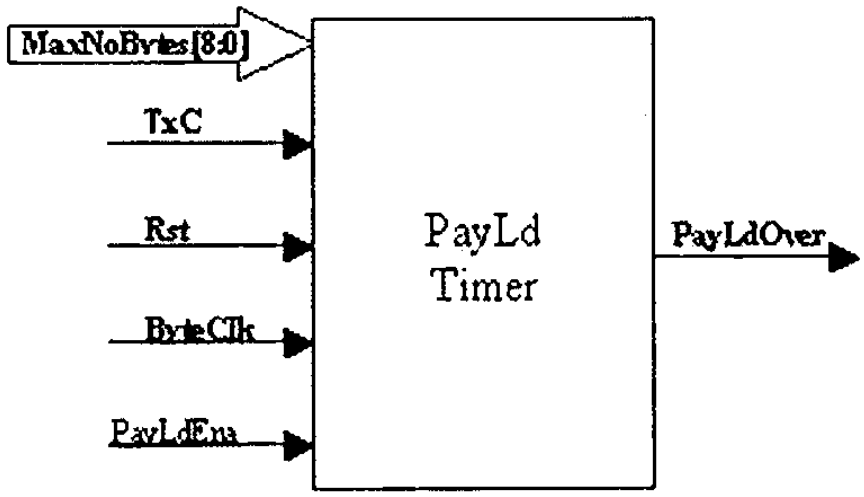

Fig. 6PayLd Timer

SIGNAL DESCRIPTION

S.No.	Part name	Mode	Description
1.	TxC	Input	Synchronizing clock
2.	Rst	Input	It initializes all internal registers
3.	ByteClk	Input	Write Clock for Access FIFO
4.	PayLdEna	Input	Enables the Timer to Count
5.	Maxnobytes (8.0)	Input	Specifies the size of FIFO
6.	PayLadOver	Output	Indicates that the FIFO is Full

DESCRIPTION:

It is the timer which counts the no. of bytes being read from the FIFO. Pay Ld Timer is shown in Fig.6 and simulated waveforms are shown in Fig.7.

Simulation Result

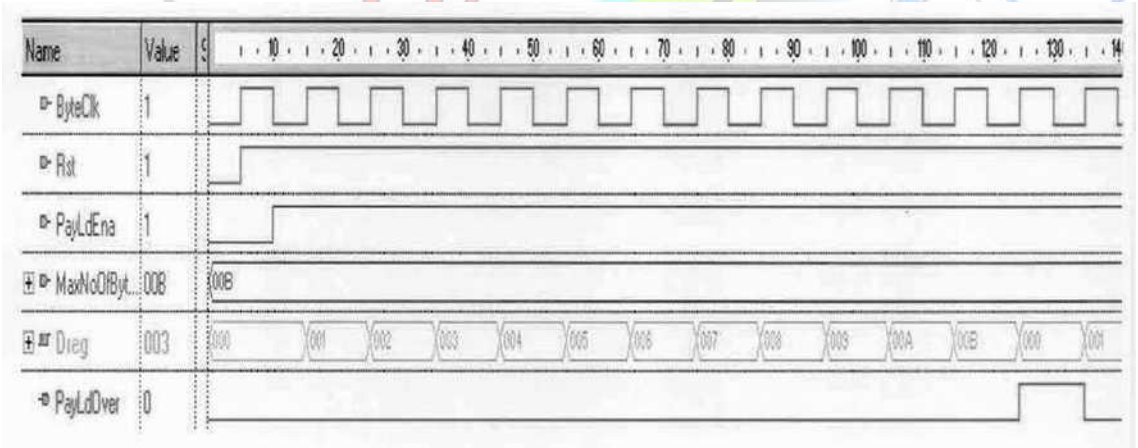

Fig.7 Simulation waveforms ofPayLd Timer

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3.4 Data MUX

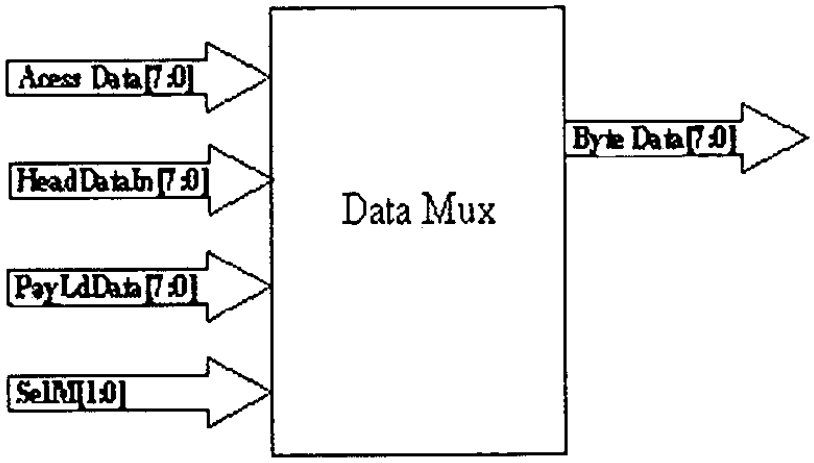

Fig. 8 Data MUX

SIGNAL DESCRIPTION

S.No.	Part name	Mode	Size	Description
1.	Access Data	Input	[7:0]	Data to write into Byte to Bit
2.	Head Data	Input	[7:0]	Data to write into Byte to Bit
3.	Pay Ld Data	Input	[7:0]	Data to write into Byte to Bit
4.	selM	Input	[1:0]	Selects the output port.
5.	Byte Data	Out	[7:0]	Data port to Byte To Bit

DESCRIPTION:

This is used to multiplex the data and selects one of the available data depending on the corresponding enable highlighted. Data Mux is shown in Fig.8 and simulated waveforms are shown in Fig.9.

Simulation Result

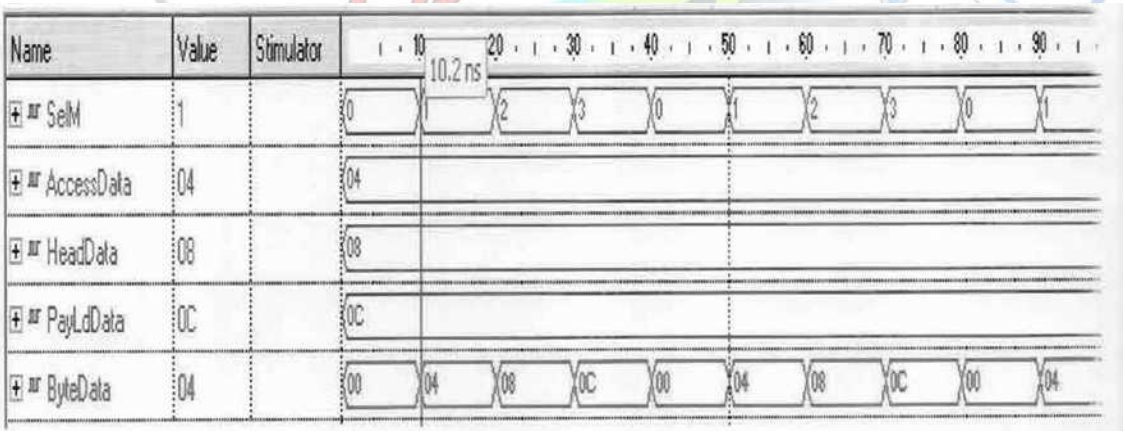

Fig.9 Simulation waveforms of Data MUX

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IV. CONCLUSION

The proposed scheme has been synthesized and simulated using Xilinx Software. In this paper, I have presented a methodology for modeling and simulation of Bluetooth transmitter using VHDL-FPGA. All the modules of the proposedsystem are implemented. The proposed scheme has been synthesized and simulated for target device of Spartan FPGA family. The proposed scheme can be synthesized and implemented on any of the existing CPLD and FPGA systems as per the requirement. The results have been presented in the form of various waveforms. Future work will implement the receiver part using the Verilog code on FPGA.

V.FPGA RESOURCE USAGE

Target Device: xv200e
Target package: cs144
Target speed:-6
Number of errors: 0, Number of warnings: 1
Logic utilization:
Total number of slice registers-571 out of 4704-12%
Number used as Flip Flops-569
Number used as Latches-02, Number of 4 inputs LUTs-662 out of 4704-14%
Logic Distribution:
Number of occupied slices: 584 out of 2352- 24%
Number of Slices containing only related logic: 584 out of 584- 100%
Number of Slices containing unrelated logic: 0 out of 584- 0%
Total number of 4 input LUTs-854 out of 4,704-18%
Number used as Logic-662
Number used as a route-throu: 192
Number of bonded IOBs-34 out of 94-36%
IOB Flip Flops: 8

REFERENCES

[1] Hemant Savla, "Design and Simulation of a Low Power Bluetooth Transceiver",A Technical Report, January 2004.
[2] Jamel Lynch,"Bluetooth Wireless Technology", IBM Corporation, 2003.
[3] Nateq Be-Nazir Ibn Minar, Mohammed Tarique, "Bluetooth Security Threats and Solutions: A Survey", International Journal of Distributed and Parallel Systems (IJDPS) Vol.3, No.1, January 2012, pp 127-148
[4]Bluetooth Special Interest Group, The Bluetooth System: Part B: Baseband Specification Draft Ver1.1, 2000.
[5] Christo Ananth, H. Anusuya Baby, "S-Box using AES Technique", International Journal of Engineering Research & Technology (IJERT), Vol. 3 Issue 3, March – 2014, pp 285-290
[7]Chun-Tang Chao, Nopadon Maneetien, Chi-Jo Wang, Juing-Shian Chiou "Performance Evaluation of Heart Sound Cancellation in FPGA Hardware Implementation for Electronic Stethoscope", Hindawi Publishing Corporation, TheScientific World Journal, Article ID 587238, , March 2014, pp 01-07