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# Versatile Unified Power Quality Conditioner Applied to Three-Phase Four-Wire Distribution Systems Using a Dual Control Strategy

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**Abstract- This paper presents the study, analysis and practical implementation of a versatile unified power quality conditioner (UPQC), which can be connected in the three-phase, three-wire or three-phase, four-wire distribution systems for performing the series-parallel power-line conditioning. Thus, even when only a three-phase three-wire power system is available at a plant site, the UPQC is able to carry out power-line compensation for installed loads that require a neutral conductor to operate at Distribution systems. Different from the control strategies used in the most of UPQC applications in which the controlled quantities are non-sinusoidal, this UPQC employs a dual compensation strategy, such that the controlled quantities are always sinusoidal. Thereby, the series converter is controlled to act as a sinusoidal current source, whereas the parallel converter operates as a sinusoidal voltage source. Thus, because the controlled quantities are sinusoidal, it is possible to reduce the complexity of the algorithms used to calculate the compensation references. Therefore, since the voltage and current controllers are implemented into the synchronous reference frame, their control references are continuous, decreasing the steady-state errors when traditional proportional-integral controllers are employed. Static and dynamic performances, as well as the effectiveness of the dual UPQC are evaluated by means of simulation results.**

## I. INTRODUCTION

The use of sophisticated equipments/loads at distribution level has been increased considerable in recent years due to the developments in the semiconductor device technologies for conversions in industrial purposes. These devices need clean power in order to function properly. At the same time these device involving switching operation generates current harmonics resulting a polluted distribution system. The power electronics based devices have been used to overcome the major power quality problems at the distribution side [1].

PQ problems, such as voltage sags/swells and voltage unbalances can also affect the proper operation of sensitive equipment causing malfunction.Furthermore, additional procedures should be taken into account in order to overcome PQ problems associated with harmonic currents generated by nonlinear loads, load unbalances and reactive power demanded by the load being used.Several procedures have been adopted to mitigate PQ problems, which can be carried out by means of active powerline conditioners, such as unified power quality conditioners (UPQCs), shunt, series and hybrid active power filters (APFs), and dynamic voltage restorers.

Active power filters (APF) have shown to be an effective technology to eliminate harmonics and to compensate nonlinear loads [2-3]. The shunt connection has been the most studied topology, where the APF is connected in parallel with the load. One of its traditional uses is the elimination of current harmonics produced by loads which generates such disturbances; this is HCS loads (Harmonic Current Source) [4,5]. However, the parallel APF is not suitable in situations where the load generates voltage harmonics; HVS loads (Harmonic Voltage Source). A Series connection APF configuration has been proposed and different control strategies have

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been tried out . [6] presented an Elaborate Study On Electronic Devices & Circuits to acquaint the students with the construction, theory and operation of the basic electronic devices such as PN junction diode, Bipolar and Field effect Transistors, Power control devices, LED, LCD and other Opto-electronic devices.

However, the cost of shunt active filters is high, and they are difficult to implement in large scale. Additionally, they also present lower efficiency. For thesereasons, different solutions are being proposed to improve the practical utilization of active filters. One of them is the use of a combined system of shunt passive filters and series active filters. This solution allows one to design the active filter for only a fraction of the total load power, reducing costs and increasing overall system efficiency [7].

On the other hand, UPQC systems can perform, simultaneously, the series-parallel active power-line compensation by using both series and parallel APFs. Thus, for overcoming utility PQ problems, UPQCs have been employed based on different concepts and solutions [8-10], comprising single-phase distribution systems [11] or in three-phase applications, considering three-phase three-wire (3P3W) distribution systems [12-13] or three-phase four-wire (3P4W) systems [14-15].

UPQCs have been presented as an attractive solution for resolving most of the power quality problems in distribution systems [16]. A typical UPQC configuration consists of two back-to-back voltage source inverters (VSI) which share the same DC-bus capacitor. Normally, the VSI placed in parallel with the load operates as a shunt APF, compensating reactive power and suppressing any harmonic currents generated by non-linear loads. On the other hand, the VSI connected in series between the utility and the load operates as a series APF, eliminating the disturbances of utility grid voltages such as voltage sags and/or swells, voltage harmonics and unbalances.

In addition, the dual compensation strategy has also been tested in UPQC applications [17-18]. Thus, different from the conventional conditioning strategy, which uses non-sinusoidal control references, the dual compensating strategy uses only sinusoidal references to control the PWM converters. As a result, the generation of the control references is easier to obtain, allowing the use of simpler algorithms to accomplish this aim.Moreover, since the output voltages are controlled to be in phase with the utility voltages, the use of a Phase-locked Loop (PLL) system operating with constant amplitude is necessary in order to generate the sinusoidal output voltage references.

Synchronous Reference Frame (SRF) based controllers (dq0-axes) are implemented in this paper to control the input currents and the output voltages of the UPQC. Due to the voltage and current references being sinusoidal, the use of continuous control references into the SRF-based controllers is allowed, leading to a reduction in steady-state errors when conventional Proportional-Integral (PI) controllers are chosen to be implemented in this same reference frame, representing another important advantage when the dual compensation strategy is compared to the conventional one. The UPQC input currents are also controlled to be in phase with the utility voltages. Thereby, the estimated utility phaseangle (θ) obtained from the PLL is also employed to generate the sinusoidal input current references.

The main objective of this paper is to present the practical implementation of a 3P4W distribution system based on UPQC topology. This versatile UPQC topology can be connected either in three-phase three-wire (3P3W) or in threephase four-wire (3P4W) distribution systems, to perform active power-line conditioning [19-20]. Nevertheless, its main application is indicated for 3P3W systems. Thus, if only a 3P3W power supply system is available at a plant site, the implemented UPQC is able to perform the power-line compensation even when the installed single-phase loads require the neutral conductor to operate.

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This paper presents two power quality conditioners (PQCs) applied to three-phase four-wire (3P4W) systems, such that one of them operates as UPQC and the other one as UPS system. As a result, the following power quality improvements are obtained: (i) suppression of load harmonic currents; (ii) compensation of load reactive power; (iii) load unbalance compensation; (iv) utility voltage unbalance compensation; (v) utility voltage harmonic suppression; (vi) regulation of the output voltages (load voltages); and (vii) uninterruptible power for critical loads when the PQC is acting as UPS.

This paper is organized as follows: Section II describes the structure of the UPQC topology and its main features are highlighted. Section III presents the modeling of series and parallel converters, while the stability analysis is treated in Section IV. The strategies used to generate the sinusoidal references of voltages and currents are presented in Section V. In Section VI the static and dynamic performances of the UPQC are evaluated by means of simulation results. Finally, Section VII presents the conclusions of the paper.

## II. UPQC TOPOLOGY DESCRIPTION

The UPQC topology employed to implement the dual compensation strategy presented in this paper is shown in Fig. 1. It is comprised of both Three-Leg (3-Leg) and Four-Leg (4- Leg) PWM converters sharing the same DC-link.

The UPQC is connected between a 3P3W power supply distribution system and a 3P4W plant site composed of several types of three-phase and single-phase loads. It is assumed that the single-phase loads use the neutral conductor to operate. In this case, a 3P4W distribution system is necessary, which is composed of three power conductors and a neutral conductor to feed the loads. Thus, as can be noted in the UPQC-based 3P4W distribution system shown in Fig. 1, the neutral current flows through the wire conductor connected to the fourth leg of the shunt 4-Leg PWM converter.

The 4-Leg PWM converter [11], [12], [13] was chosen to act as the shunt APF, because it is able to operate with lower DC link voltage amplitude when compared to the 3-Leg PWM split-capacitor topology [15]. In addition, the 3-Leg split capacitor topology requires an additional control loop to compensate its inherent DC-link capacitor voltage unbalances. Although the 4-Leg converter has a greater number of switches, the power rating of the devices that compose its fourth leg is reduced, because the current that flows through the neutral conductor in most cases is low.

### *A. Dual Compensation Principle:*

In order to make the input currents sinusoidal, balanced and in phase with the utility voltages, in the dual compensating strategy, the series PWM converter is controlled to operate as a sinusoidal current source. In this case, its impedance must be high enough to isolate the harmonic currents generated by the non-linear loads. On the other hand, the parallel PWM converter also makes the output voltages sinusoidal, balanced, regulated and in phase with the utility voltages. In other words, it is controlled to operate as a sinusoidal voltage source, such that its impedance must be sufficiently low to absorb the load harmonic currents [16].

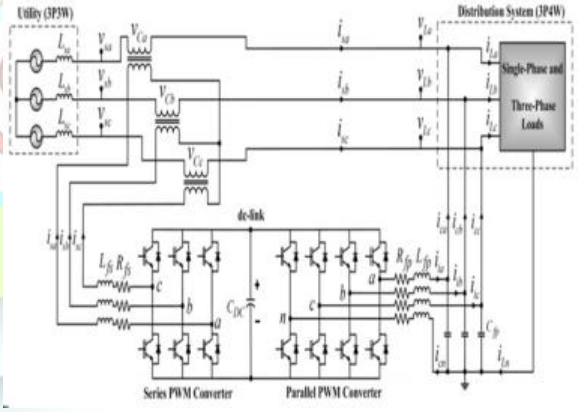


Fig. 1. 3P4W distribution system based on UPQC topology connected to 3P3W power system.

Since the series and parallel converters have high and low impedances, respectively, the load harmonic currents flow naturally through the parallel converter.

On the other hand, the utility harmonic voltages and unbalances are compensated ensuring that the controlled output voltages follow sinusoidal and balanced references, such that the amplitude

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differences between the input and output voltages will appear across the series coupling transformers, meaning that any utility voltage disturbances are naturally compensated. [14] presented a book, this book makes students to expose themselves to basic electronic devices, be familiar with the theory, construction, and operation of Basic electronic devices.

## III. MODELING OF SERIES AND PARALLEL CONVERTERS

The modeling of the series and parallel PWM converters are presented in this section. In addition, the voltage and current controllers implemented in the SRF (dq0-axes) are discussed.

### *A. Series Converter Modeling*

The state-space system and the transfer functions of the series converter in the dq-axes are obtained based on a mathematical model. The modeling is accomplished considering that all involved inductances and resistances are identical, as follows: $L_{fsa} = L_{fsb} = L_{fsc} = L_{fs}$ and $R_{fsa} = R_{fsb} = R_{fsc} = R_{fs}$. By means of Fig. 1, the equations that represent the system are given by (1) and (2).

$$u_{sab\_pwm} = v_{Lfsa} + v_{Rfsa} + v_{Cab} - v_{Rfsb} - v_{Lfsb} \quad (1)$$

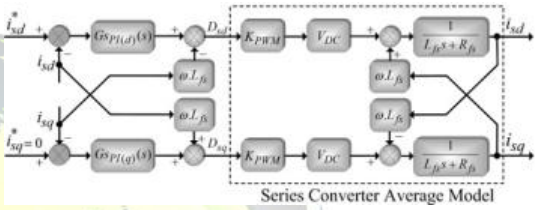
$$u_{sbc\_pwm} = v_{Lfsb} + v_{Rfsb} + v_{Cbc} - v_{Rfsc} - v_{Lfsc} \quad (2)$$

Where, $u_{sab\_pwm}$ and $u_{sbc\_pwm}$ are the respective PWM voltages at the 3-Leg series converter terminals.

Considering the voltages of the PWM series converter in the dq-axes ($u_{sab_{pwm}} and u_{sbc\_pwm}$), the state-space equation is given by:

$$\dot{x}_{sdq}(t) = A_{sdq} \cdot x_{sdq}(t) + B_{sdq} \cdot u_{sdq}(t) + F_{sdq} \cdot w_{sdq}(t) \quad (3)$$

Thereby, based on (3), the series converter average model represented as a signal flow graph is shown in the dotted area of Fig. 2(a). In addition, the current controller into the dq-axes is also shown, where the transfer functions of the PI current controllers; $D_{sd} and D_{sq}$ are the duty cycles; $V_{DC}$ is the DC-bus voltage; and $K_{PWM}$ is the gain of the PWM modulator given by $K_{PWM} = {}^{1}/_{K_{PWM}}$, where $P_{PWM}$ is the peak value of the PWM triangular carrier implemented in the digital signal processor (DSP). The current coupling between the dq-axes, shown in the average model of Fig. 2(a), is eliminated by using the scheme presented in Fig. 2(b), where the dotted blocks represent the decoupling effects [32] implemented in the block diagram shown in Fig. 2(a).




(a)

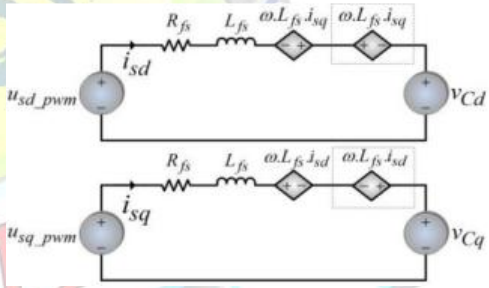



Fig. 2. Series converter: (a) Signal flow graph of the current controllers and average model; (b) Model of the uncoupled system in SRF dq-axes.

Thus, based on Fig. 2(a), the transfer functions of the closed loop system can be represented by (4), where $Kp_{s(d,q)}$ and $Ki_{s(d,q)}$ are the proportional and integral controller gains, and $i^{*}_{s(d,q)}(S)$ represents the continuous current references in the dq coordinates.

$$\frac{i_{s(d,q)}(S)}{i^{*}_{s(d,q)}(S)} = \frac{X_1(Kp_{s(d,q)}s + Ki_{s(d,q)})}{L_{fs}s^2 + (R_{fs} + X_1 Kp_{s(d,q)})s + X_1 Ki_{s(d,q)}} \quad (4)$$

### *B. Parallel Converter Modeling*

The state-space system and the transfer functions of the parallel converter in the dq0-axes are obtained based on a mathematical model. The modeling is accomplished considering that all involved inductances, resistances and capacitances

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are identical, as follows$L_{fpa} = L_{fpb} = L_{fpc} = L_{fpc} = L_{fpn} = L_{fp}$ , $R_{fpa} = R_{fpb} = R_{fpc} = R_{fpc} = R_{fpn} = R_{fp}$ and $C_{fpa} = C_{fpb} = C_{fpc} = C_{fp}$By means of Fig. 1, the equations that represent the system are given by (5), (6) and (7), as follows:

By means of Fig. 1, the equations that represent the system are given by (5), (6) and (7), as follows:

$$u_{pan\_pwm} = R_{fpa}.i_{ia} + L_{fpa}\frac{di_{ia}}{dt} + v_{La} + L_{fpn}\frac{di_{cn}}{dt} + R_{fpn}.i_{cn} \quad (5)$$

$$u_{pbn\_pwm} = R_{fpb}.i_{ib} + L_{fpb}\frac{di_{ib}}{dt} + v_{Lb} + L_{fpn}\frac{di_{cn}}{dt} + R_{fpn}.i_{cn} \quad (6)$$

$$u_{pcn\_pwm} = R_{fpc}.i_{ic} + L_{fpc}\frac{di_{ic}}{dt} + v_{Lc} + L_{fpn}\frac{di_{cn}}{dt} + R_{fpn}.i_{cn} \quad (7)$$

The capacitor currents of the output filters $(i_{cfpa}, i_{cfpb} and i_{cfpc})$are given by:

$$i_{cfpa} = c_{fpa}\frac{dv_{La}}{dt} = i_{ia} - i_{ca} \quad (8)$$

$$i_{cfpb} = c_{fpb}\frac{dv_{Lb}}{dt} = i_{ib} - i_{cb} \quad (9)$$

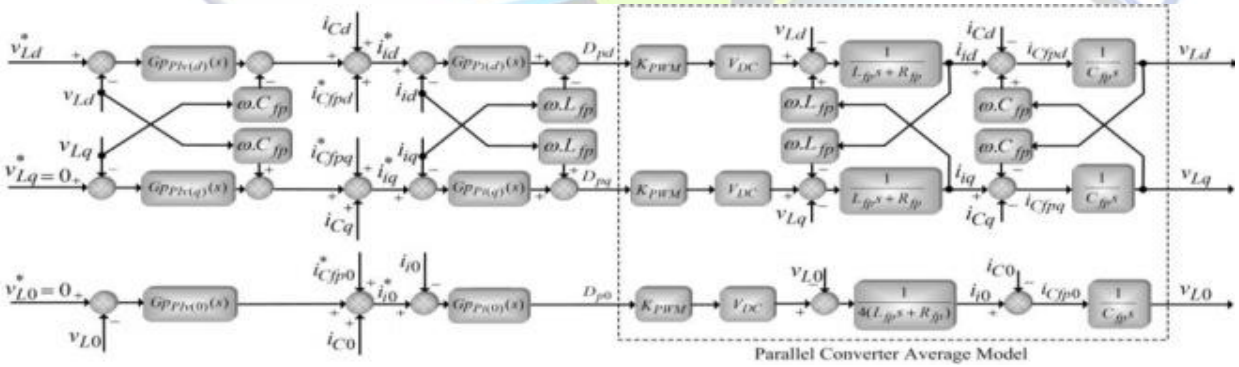
$$i_{cfpc} = c_{fpc}\frac{dv_{Lc}}{dt} = i_{ic} - i_{cc} \quad (10)$$

Considering the PWM converter voltages of the parallel synchronous rotating frame, $u_{pd\_pwm}, u_{pq\_pwm} and u_{po\_pwm}$ the state-space equation is found as:

$$\dot{x}_{pdq0}(t) = A_{pdq0}\cdot x_{pdq0}(t) + B_{pdq0}\cdot u_{pdq0}(t) + F_{pdq0}\cdot w_{pdq0}(t) \quad (11)$$

Thereby, based on (11), the parallel converter average model represented as a signal flow graph is shown in the dotted area of Fig. 3(a). In addition, the voltage and current controllers into the dq0-axes are presented, where $G_{pPIv(d)}, G_{pPIv(q)} and G_{pPIv(0)}$ represent the transfer functions of the PI voltage controllers (outer loops); $G_{pPIv(d)}, G_{pPIv(q)} and G_{pPIv(0)}$ are the transfer functions of the proportional current controllers (inner loops); and $D_{pd}, D_{pd} and D_{po}$ are the duty cycles. The current and voltage coupling between the dq-axes shown in the average model of Fig. 3(a) is eliminated by using the scheme presented in Fig. 3(b), where the dotted blocks represent the decoupling effects, which are implemented in the block diagram shown in Fig. 3(a).

Thus, based on Fig. 3(a), the transfer functions of the closed loop system can be represented by (12) and (13), where $K_{p_{p(d,q)}}, K_{i_{p(d,q)}} and K_{i_{p(0)}}$ are the proportional and integral gains of the controllers (outer voltage control loop), $K_{p_{pi(d,q)}} and K_{p_{pi(o)}}$ are the proportional gains (inner current control loop), and $v^*_{L(d,q,o)}(s)$ represents the continuous voltage references in the dq0 coordinates.

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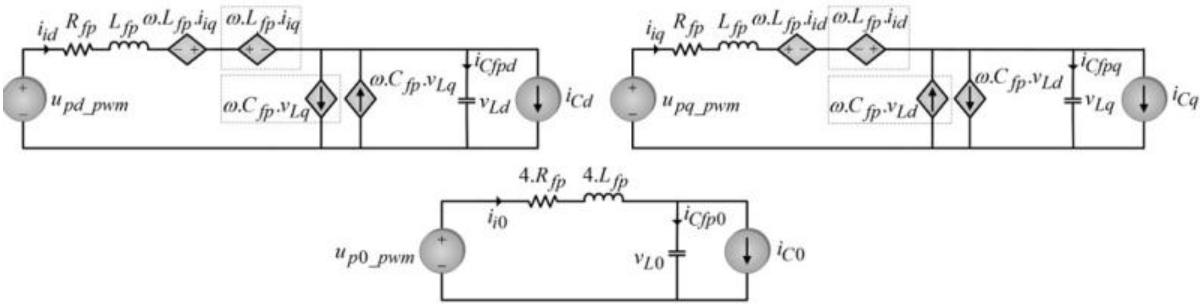


(b)

Fig. 3. Parallel converter: (a) Signal flow graph of the voltage controllers and average model; (b) Model of the uncoupled system in SRF dq0-axes.

The currents of the filter capacitors $i_{cfpd(d.q,o)}$ shown in Fig. 3(a) are estimated considering the derivatives of the measured output voltages $(v_{La,b,c})$ and the respective capacitances $(C_{fa,b,c})$.

$$\frac{v_{L(d,q)(S)}}{v^*_{L(d,q)(S)}} = \frac{X_{1(d,q)}s^2+X_{2(d,q)}s+X_{3(d,q)}}{Y_{1(d,q)}s^3+Y_{2(d,q)}s^2+Y_{3(d,q)}s+Y_{4(d,q)}} \quad (12)$$

$$\frac{v_{L(0)(S)}}{v^*_{L(0)(S)}} = \frac{X_{1(0)}s^2+X_{2(0)}s+X_{3(0)}}{Y_{1(0)}s^3+Y_{2(0)}s^2+Y_{3(0)}s+Y_{4(0)}} (13)$$

## VI. STABILITY ANALYSIS OF THE SYSTEM

This section presents the stability study of the UPQC system, which involves the series and parallel converters. The aim of this study was to verify the ability of the system to remain stable even under load disturbances.

### *A. Series APF*

Considering the signal flow graph of the current controller and the series converter average model shown in Fig. 2(a), the closed loop transfer function in the dq coordinates can be represented by (4). Thereby, the stability analysis of the series converter involves only the second order denominator of (4). Therefore, since the reference currents are always sinusoidal, it is possible to assume that the series converter remains acting as a sinusoidal current source even when load transients occur.

### *B. Parallel APF*

Considering the signal flow graph of the voltage controllers and the parallel converter average model shown in Fig. 3(a), the closed loop transfer functions in the dq0 coordinates can be represented by (12) and (13). Considering that the PI controller gainand the same transfer function is obtained for each control loop implemented in the d, q and 0 coordinates as given by (14), allowing the study of the voltage control loops by means of a unique transfer function . In addition, it is assumed that the individual control loops in the dq0 coordinates are obtained taking into account the coupling effects between the dq coordinates shown in Fig. 3.

$$G_v(s) = \frac{v_{L(d,q,0)}(s)}{v^*_{L(d,q,0)}(s)} = \frac{(1+K)[X_{1(d,q,0)}s^2+X_{2(d,q,0)}s+X_{3(d,q,0)}]}{Y_{1(d,q,0)}s^3+Y_{2(d,q,0)}s^2+Y_{3(d,q,0)}s+Y_{4(d,q,0)}} (14)$$

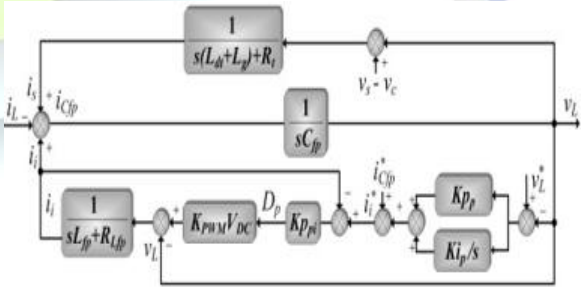


Fig. 4. Parallel converter equivalent model used to stability analysis for the dq0 voltage control loops

Fig. 4 presents the block diagram, which is based on the control loops shown in Fig. 3(a), as well as the aforementioned considerations. In addition, in order to obtain an adequate representation of the

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system, the source current is calculated from both the output voltage ($v_L$)and input voltage , taking into account the leakage inductances and resistances of the series coupling transformers , as well as the grid equivalent inductances Thereby, from Fig. 4, the closed loop transfer function can be obtained by (15).

By applying the Routh-Hurwitz stability criterion, two conditions must be met: i) all the polynomial coefficients of the denominator must have the same sign; ii) the inequality must be respected. Therefore, by inspecting the denominator of (15), the first condition is always met. On the other hand, the second condition can be met by adjusting the PI controller gains. Thus, taking into account the aforementioned conditions, the system will always be stable, even when load transients occur.

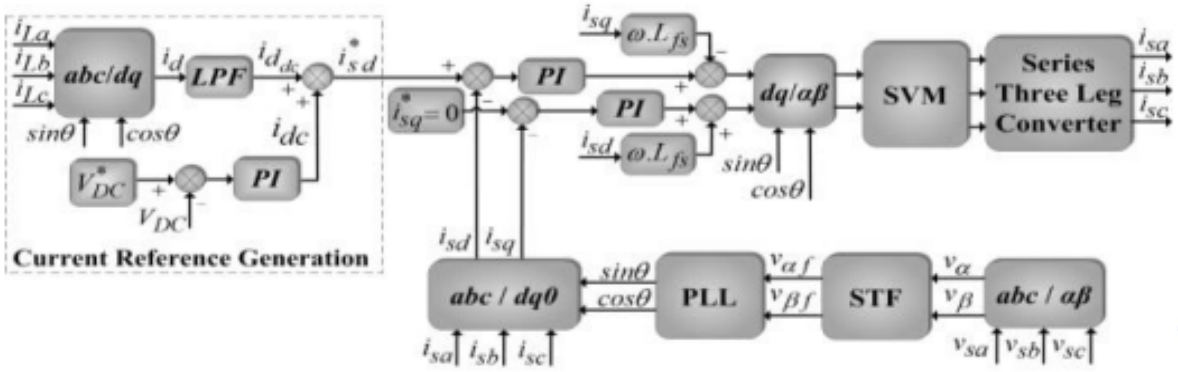
$$G_{vi}(s) = \frac{v_{L(d,q,0)}(s)}{i^*_{L(d,q,0)}(s)} = \frac{X_1 s^2 + X_2 s + X_3}{Y_1 s^3 + Y_2 s^2 + Y_3 s + Y_4} \qquad (15)$$

## V. CONTROL REFERENCES OF THE SERIES AND PARALLEL CONVERTERS

In this section the strategies used to generate the sinusoidal reference quantities used to control the series and the parallel converters are presented. As aforementioned, both the current and voltage control references are controlled to be in phase with the utility voltages.

### *A. Series Converter Reference Currents*

The current control loop of the series converter is shown in the signal flow graph of Fig. 5(a). The continuous reference current in the SRF direct axis d is defined by , which is able to make the serial converter synthesize the sinusoidal input currents.




(a)

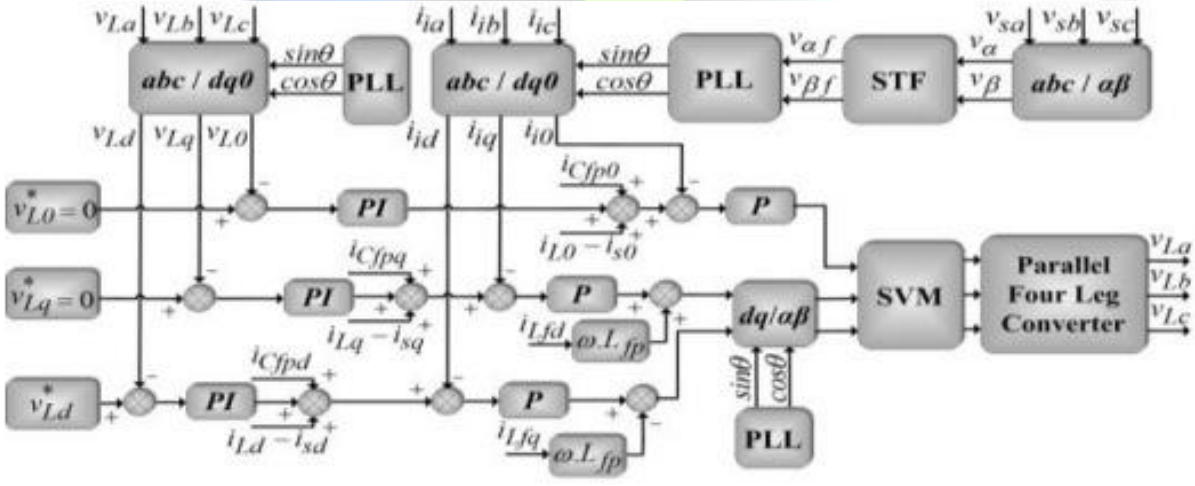



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Fig. 5. Signal flow graphs of the reference generation and control scheme of both series and parallel PWM converters: (a) Reference current generation and the input current controllers; (b) Output voltage controllers.

The reference current $i_{sd}^{*}$ is obtained by measuring the load currents $(i_{La}, i_{Lb} i_{Lc})$ and converting them to the rotating reference frame. Thus, the direct current$(i_d)$ is achieved by means of (16) and (17), whereas the utility phase-angle $\theta$, used to calculate the coordinates of the unit vectors $sin\theta$ and $cos\theta$, is obtained from the three-phase PLL system. Next, a low-pass filter (LPF) is employed to obtain the direct component $(i_{d_{dc}})$which represents, in the SRF, the active portions of the load currents$(i_{La}, i_{Lb} i_{Lc})$ .

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (16)$$

$$i_d = i_\alpha \cos\theta + i_\beta \sin\theta \quad (17)$$

The control of the power balance flow through the UPQC must be take into account in order to maintain the DC-bus voltage constant. Thereby, the final reference current $i_{sd}^{*}$ is calculated by using (18), where $(i_d)$is added to$i_{d_{dc}}$ . In addition, $i_{dc}$ controls the balance of the power flow through the UPQC when different amplitudes between the input voltages $(v_{sa}, v_{sb} v_{sc})$ and output voltages $(v_{La}, v_{Lb} v_{Lc})$ occur [30].

$$i_{sd}^{*} = i_{dc} + i_{d_{dc}} \quad (18)$$

The reference current of the quadrature axis q $(i_{sd}^{*})$ and $i_{sO}^{*}$ are set to zero since the series converter synthesizes only positive sequence components (active currents), such that sinusoidal and balanced currents are achieved.

### *B. Parallel Converter Reference Voltages*

The voltage control loop of the parallel converter is shown in the signal flow graph of Fig. 5(b). The reference voltage in the SRF direct axis d is defined by $V_{Ld}^{*}$. Its constant and continuous value represents the AC voltages $(v_{La}, v_{Lb} v_{Lc})$ provided to the load. The reference voltages of the quadrature axis q $(V_{Lq}^{*})$and $V_{Lo}^{*}$are set to zero since sinusoidal and balanced voltages are desirable. As can be noted, the 3-DSVM technique is employed in the parallel converter.

## VI. SIMULATION RESULTS

The main parameters used in the experimental tests are shown in Table I, whereas the controller parameters, such as the phase-margins and crossover frequencies used to determine the PI controller gains are shown in Table II. The controllers were tuned based on the frequency response method adopting the gain crossover frequency at 0dB and the phase-margin as design parameters [19]. Finally, the three-phase non-linear loads adopted in the experiments are described in Table III.

Fig. 7 presents the static behavior of the currents involved in the UPQC operation, considering the loads presented in Table III. The unbalanced load currents, $(i_{La}, i_{Lb}, i_{Lc}, i_{Ln})$ the compensated source currents ( $i_{sa}, i_{sb}, and i_{sc}$) and the compensation currents $(i_{ca}, i_{cb}, i_{cc}, i_{cn})$ are shown in Fig. 7(a), considering the unbalanced three-phase load (1). As can be noted, the source currents are sinusoidal, balanced, and with very low harmonic contents. In addition, it can be seen that the load neutral wire current $(i_{Ln})$flows to the fourth leg of the parallel 4-Leg converter$(i_{cn})$.

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TABLE I
Gains ofthe PI Controllers and Design Specifications

| | Parallel Converter | | | Series Converter | |
|---|---|---|---|---|---|
| *dq0-axes* | Outer Loop | | Inner Loop | $Kp_s$ | $Ki_s$ |
| | $Kp_p$ | $Ki_p$ | $Kp_{pi}$ | | |
| *dq* | 0.2333 $\Omega^{-1}$ | 549 $\Omega^{-1}$/s | 90 Ω | 233.10 Ω | 1217639 Ω/s |
| *0* | 0.2381 $\Omega^{-1}$ | 526 $\Omega^{-1}$/s | 361 Ω | --- | --- |
| DC-bus voltage | | | | $Kp_{dc}$= 0.0357 $\Omega^{-1}$ | $Ki_{dc}$= 0.1202 $\Omega^{-1}$/s |
| Crossover frequency of the parallel converter inner current loop | | | | $\omega_{ci_p} = 2\pi f_s/6\ rad/s$ | |
| Phase margin | | | | $MF_{ip}$= 75° | |
| Crossover frequency of the parallel converter outer loop voltage | | | | $\omega_{cv_p} = 0.16\omega_{ci_p}\ rad/s$ | |
| Phase margin | | | | $MF_{vp}$= 55° | |
| Crossover frequency of the series converter current loop | | | | $\omega_{ci_s} = 2\pi f_s/9\ rad/s$ | |
| Phase margin | | | | $MF_{is}$= 50° | |
| Crossover frequency of the DC bus loop voltage | | | | $\omega_{c_{vcc}} = 42\ rad/s$ | |
| Phase margin | | | | $MF_{v_{cc}}$= 87.5° | |

TABLE II
Parameters Used In the TestsCarried Out On theUPQC

| | |
|---|---|
| Apparent power of the unbalanced three-phase load (1) | $S_a$= 1590 VA, $S_b$= 1260 VA, $S_c$= 950 VA |
| Apparent power of the unbalanced three-phase load (2) | $S_{La}$= 1940 VA, $S_{Lb}$= 1260 VA, $S_{Lc}$= 1590 VA |
| Apparent power of the three-phase load | $S_L$= 4170 VA |
| Effective nominal voltage of the utility (line-to-neutral)) | $V_{sa,b,c}$= 127 V |
| Nominal utility grid frequency | $f_s$= 60 Hz |
| Switching frequency of the converters | $f_{ch}$= 20 kHz |
| Coupling inductance of the parallel converter | $L_{fpa,b,c}$= 1.0 mH |
| Series resistance of the coupling inductors (parallel converter) | $R_{Lfpa,b,c}$ = 0.12 Ω |
| Capacitances of the parallel filters | $C_{fpa,b,c}$= 85 µF |
| Coupling inductance of the series converter | $L_{fsa,b,c}$= 1.5 mH |
| Series resistance of the coupling inductors (series converter) | $R_{Lfa,b,c}$ = 0.15 Ω |
| Dispersion inductance of the series coupling transformer | $L_{di}$= 0.42 mH |
| Resistances of the series coupling transformers | $R_{ta,b,c}$= 0.26 Ω |
| Transformation ratio of the series coupling transformers | $n$= 1 |
| DC-bus voltage | $V_{dc}$= 400 V |
| DC-bus capacitance | $C_{dc}$= 9400 µF |
| DSP sampling frequency | $f_a$= 40 kHz |
| Gain of the PWM modulator | $K_{PWM}$= 2.66.$10^{-4}$ |

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In Fig. 7(b) the experimental results for the unbalanced three-phase load (2) are shown, where the load currents $(i_{La}, i_{Lb}, i_{Lc})$, the currents related to phase "a" , $(i_{La}, i_{ca}, i_{sa})$ and the input and output currents and voltages related to phase "a" $(v_{sa}, i_{sa}, v_{La} and i_{La})$ can be seen. It can be noted that both the input currents, as well the output voltages are controlled to be in phase with the utility voltages.

The results obtained for the balanced three-phase load (1) are presented in Fig. 7(c), where the load currents $(i_{La}, i_{Lb}, and i_{Lc})$ , the output voltage $v_{La}$ , the parallel converter compensation currents $(i_{ca}, i_{cb} and i_{cc})$ , and the balanced source currents $(i_{sa}, i_{sb} and i_{sc})$ are shown.

The results presented in Fig. 7 show the ability of the UPQC to perform the power-line compensation even when only a 3P3W system is available at a plant site is, and the installed loads require a neutral conductor for connecting one or more single-phase loads (3P4W). Table IV shows the THD of the load currents $(i_{La}, i_{Lb}, i_{Lc})$ and source currents $(i_{sa}, i_{sb} and i_{sc})$ , where a significant reduction in the THDs related to the compensated source currents is noted.

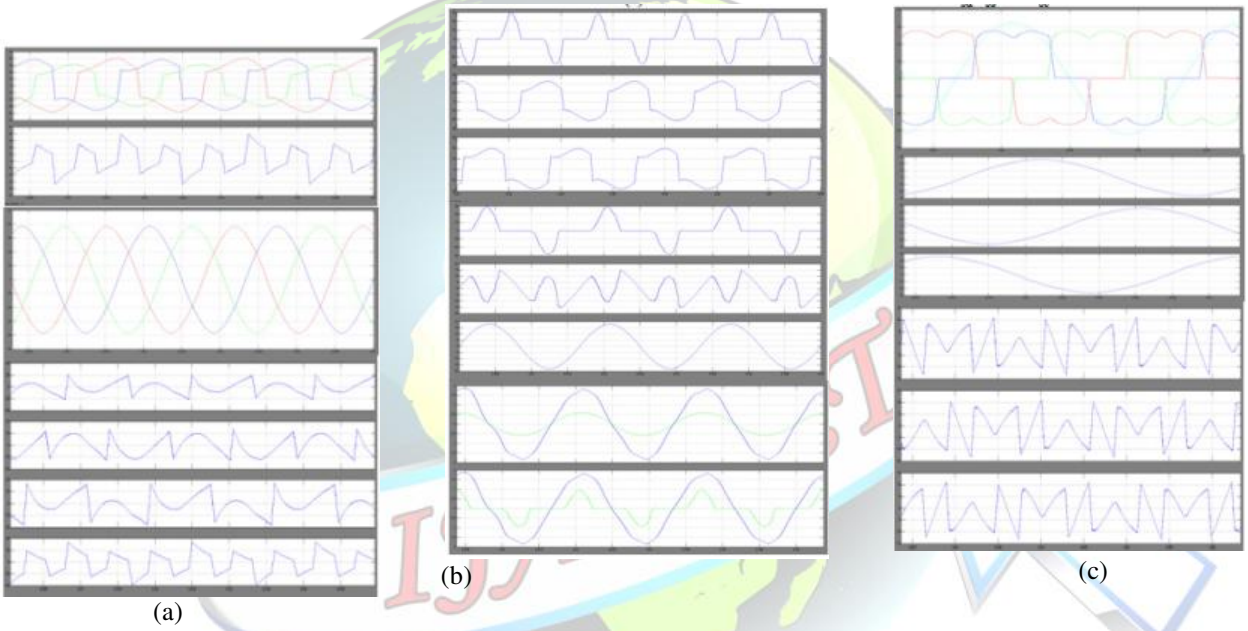


Fig. 7. Experimental results for the loads presented in Table III: (a) UPQC currents for unbalanced three-phase - phase load (1) (20 A/div, 5 ms/div): Load currents $(i_{La}, i_{Lb}, i_{Lc})$and $i_{Ln}$, Compensated source currents $(i_{sa}, i_{sb}, i_{sc})$, and Currents of the parallel converter $(i_{ca}, i_{cb}, i_{cc})$and$i_{Cn}$ ; (b) Currents and voltages of phase "a" of the UPQC for the unbalanced three-phase load (2) (20 A/div, 100V/div, 5 ms/div): Load currents $(i_{La}, i_{Lb}, i_{Lc})$; Currents of phase "a": load $i_{La}$, parallel converter $i_{ca}$and source$i_{sa}$ ; voltages and currents of phase "a": load current$i_{La}$ , source current$i_{sa}$ , utility voltage $v_{sa}$ and load voltage $v_{La}$ (c) UPQC currents for three-phase load (1) (2.5 ms/div): Load currents$(i_{La}, i_{Lb}, i_{Lc})$ (5 A/div), Source compensated currents $(i_{sa}, i_{sb}, i_{sc})$, (10 A/div), Parallel converter currents $(i_{ca}, i_{cb}, i_{cc})$ (10 A/div).

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TABLE III
LOAD PARAMETERS USED IN THE EXPERIMENTAL TESTS

| Unbalanced three-phase loads | | Phase A | Phase B | Phase C |
|---|---|---|---|---|
| Three single-phase full wave rectifiers | (1) | R=8.1 Ω<br>L=380 mH | R=10.12 Ω<br>L=346 mH | R=13.50 Ω<br>L=357 mH |
| | (2) | R=13.5 Ω<br>C=940 µF | R=10.12 Ω<br>L=346 mH | R=8.1 Ω<br>L=380 mH |
| Balanced three-phase load | | | Phases ABC | |
| Three-phase full wave rectifier | (1) | | R=17.7 Ω | |

TABLE IV
Load and Source Currents Total Harmonic Distortions

| Three-phase loads | Total Harmonic Distortion (THD %) | | | | | |
|---|---|---|---|---|---|---|
| | $i_{La}$ | $i_{Lb}$ | $i_{Lc}$ | $i_{sa}$ | $i_{sb}$ | $i_{sc}$ |
| Unbalanced three-phase load (1) | 30.7 | 25.0 | 24.9 | 1.2 | 1.0 | 1.0 |
| Unbalanced three-phase load (2) | 62.7 | 25.0 | 30.7 | 0.9 | 1.0 | 1.2 |
| Three-phase load (1) | 26.0 | 26.0 | 26.0 | 1.7 | 1.7 | 1.7 |

TABLE V
THDof The Input And Output Voltages For The Unbalanced Three-Phase Load (1)

| Three-phase load | Total Harmonic Distortion (THD%) | | | | | |
|---|---|---|---|---|---|---|
| | $v_{sa}$ | $v_{sb}$ | $v_{sc}$ | $v_{La}$ | $v_{Lb}$ | $v_{Lc}$ |
| Unbalanced three-phase load (1) | 12.3 | 12.3 | 12.3 | 1.8 | 1.7 | 1.7 |

Fig. 8 presents the static behavior of the voltages involved in the UPQC operation. Balanced, however distorted, input voltages, $(v_{sa}, v_{sb} and v_{sc})$ the compensated output voltages $(v_{La}, v_{Lb} and v_{Lc})$, and the compensation voltages across the series transformers $(v_{ca}, v_{cb} and v_{cc})$ are shown in Fig. 8(a), whereas unbalanced, however undistorted, input voltages, the compensated output voltages, and the compensation voltages across the series transformers $(v_{ca}, v_{cb} and v_{cc})$ are shown in Fig. 8(b), considering the unbalanced three-phase load (1). Table V presents the THD of the input and output voltages related to the experimental tests presented in Fig. 8(a). A significant reduction of the harmonic contents present in the output voltages is noted.

Fig. 9 presents the dynamic behavior of the DC-bus voltage $(V_{DC})$ and the source currents $(i_{sa}, i_{sb} and i_{sc})$, when the load of phase "a" is disconnected and reconnected after a few seconds. Fig.9(a) presents the DC-bus voltage and the unbalanced load currents $(i_{La}, i_{Lb}, i_{Lc})$,. As can be noted, even before and after the load transients, the source currents remain balanced as shown in Fig. 9(b). Fig. 9(c) shows the source currents in detail after the first transient. The action of the DC-bus voltage controller on the input currents keeps the voltage controlled at 400 V. The UPQC dynamic behavior under voltage sag (30%) during ten utility cycles is presented in Fig. 10 considering phase 'a'. As can be seen, the UPQC output voltage does not suffer with the voltage sag disturbance, remaining sinusoidal and regulated.

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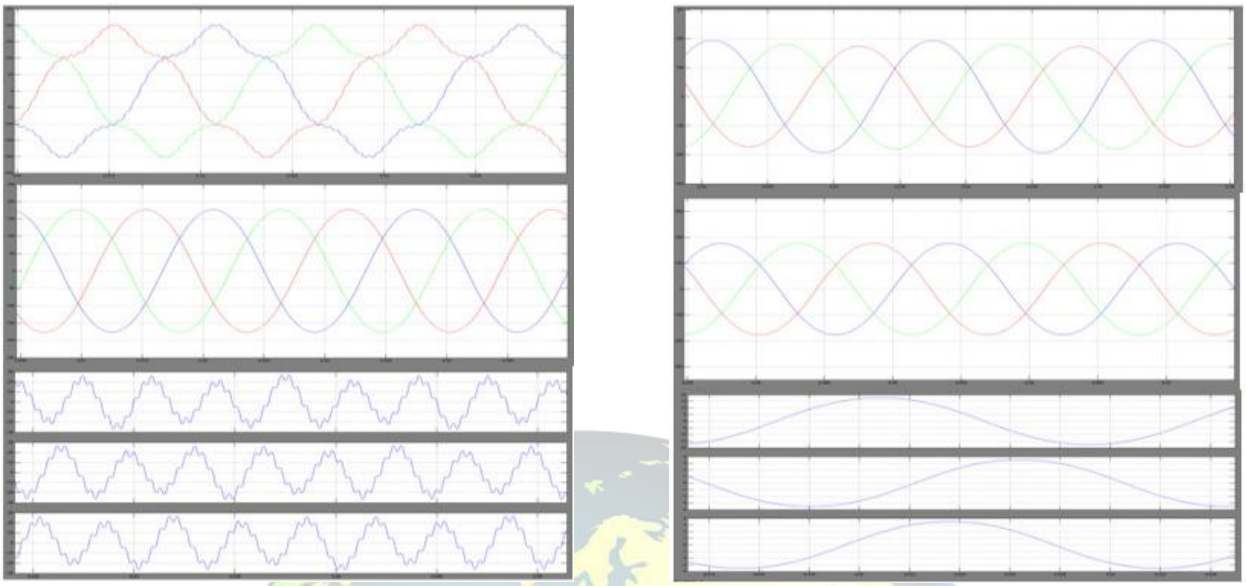
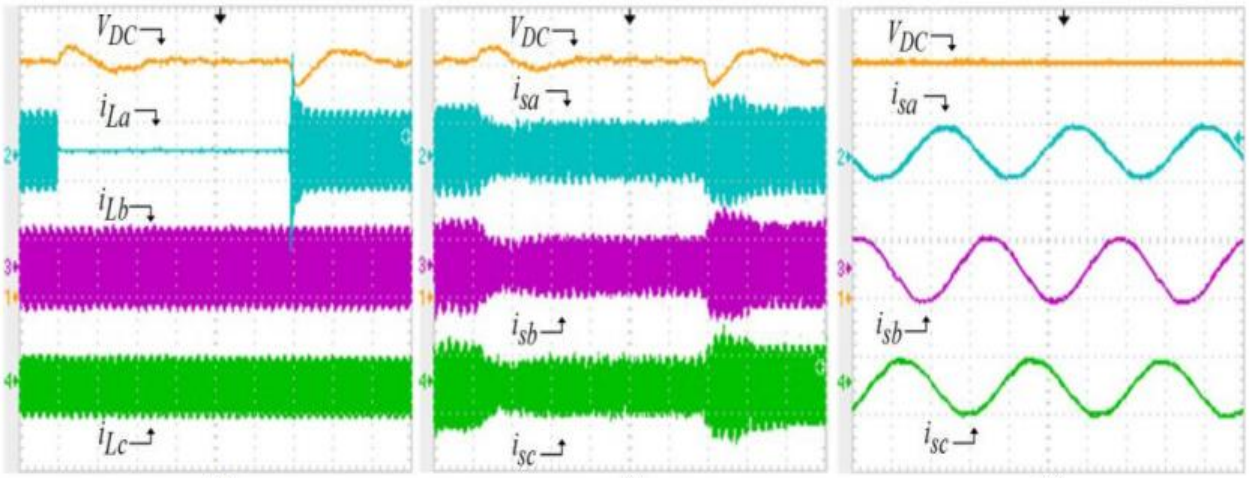


(a) (b)

Fig. 8. Voltages of the UPQC under utility harmonics and unbalances for the unbalanced three-phase load (1): (a) Utility voltages $(v_{Sa}, v_{Sb} and v_{Sc})$(50 V/div, 2,5ms/div), Load voltages $(v_{La}, v_{Lb} and v_{SL})$ (50 V/div, 2,5ms/div) and series compensating voltages $(v_{ca}, v_{cb} and v_{cc})$ (50 V/div, 2,5ms/div); (b) (a) Utility voltages $(v_{Sa}, v_{Sb}, v_{Sc})$(50 V/div, 2,5ms/div), Load voltages $(v_{La}, v_{Lb} and v_{SL})$ (50 V/div, 2,5ms/div) and series compensating voltages $(v_{ca}, v_{cb} and v_{cc})$(50 V/div, 2,5ms/div)




(a) (b) (c)

Fig. 9. Voltages and current of the UPQC for the unbalanced three-phase load 1: (a) DC-bus voltage $(V_{DC})$ (100 V/div, 500ms/div) and load currents $(i_{La}, i_{Lb}, i_{Lc})$ (20 A/div, 500ms/div); (b) DC-bus voltage $(V_{DC})$ (100 V/div, 500ms/div) and source currents $(i_{sa}, i_{sb}, i_{sc})$, (20 A/div, 500ms/div); (c) DC-bus voltage $(V_{DC})$ (100 V/div, 5ms/div) and details of the source currents $(i_{sa}, i_{sb}, i_{sc})$, after the first load transient (20 A/div, 5ms/div).

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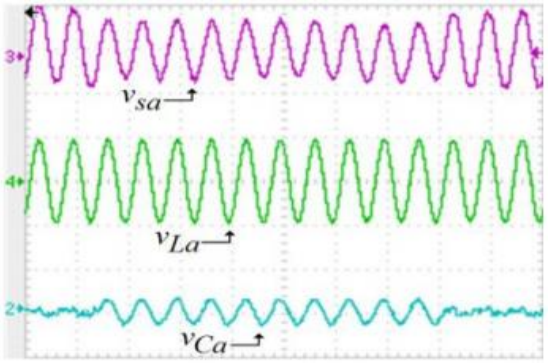


Fig. 10. UPQC under voltage sag disturbance (phase 'a'): utility voltage ($V_{sa}$), load voltage ($V_{La}$) and series compensating voltage ($V_{Ca}$) (200 V/div, 25ms/div).

## VII. CONCLUSION

This paper presents a practical and versatile application based on UPQC, which can be used in three-phase three-wire (3P3W), as well as three-phase four-wire (3P4W) distribution systems. It was demonstrated that the UPQC installed at a 3P3W distribution system was able to perform universal active filtering even when the installed loads required a neutral conductor for connecting one or more single-phase loads (3P4W). The series-parallel active filtering allowed balanced and sinusoidal input currents, as well as balanced, sinusoidal and regulated output voltages at the distribution system.

By using a dual control compensating strategy, the controlled voltage and current quantities are always sinusoidal. Therefore, it is possible to reduce the complexity of the algorithms used to calculate the compensation references. Furthermore, since voltage and current SRF-based controllers are employed, the control references become continuous, reducing the steady-state errors when conventional PI controllers are used.

Based on simulation tests, static and dynamic performances, as well as the effectiveness of the dual UPQC were evaluated, and can be said that it can be used effectively in distribution systems.

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