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# Integration Technique for Health Care Allied Equipment using Transistor Dense Flip Flop

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## ABSTRACT

The augmentation of Health care allied equipments manufacturing is escalating nowadays along with usual smart phone, digital camera and tablet PC. The most important issues arise in battery powered equipments are Power consumption that is due to the increasing demand in the manufacturing of power reduction equipment. To determination these tribulations, different types of circuit techniques have been projected previously. Transistor Dense Flip Flop (TDFF) proposes two methods which require diminutive area and Low power consumption when compared with other Flip-Flops. Topological Dense and Integrate connecting logically equivalent transistor with unconventional latch structure are the two methods which reduce the area and power consumption.

*Keywords* - TDFF, Reduced – delay, VLSI, low Power, clock.

## 1. Introduction

In olden days, low-power Flip-Flops (FFs) have been utilized for several purpose. Where as in definite chip design, the predictable Flip-Flop is still used mainly often due to its superior balanced power, performance and cell area. To apprehend the complete objective this technique focuses on power decrease without any outrageous environment of timing operation and cell area. The design of system using chips mostly depends upon the fundamental performance factor such as area, power dissipation and circuit speed. Due to this dropping of power dissipation and propagation delay this Flip-Flop is extremely significant one [1]. However their performance is not effectively sufficient for utilize in present elevated performance mobile application such as Silicon on Chips; but the power dissipation of the CMOS Flip-Flop is small with negatively slow speed.

A absolute investigation of the timing requirements of dissimilar clocking technique for the synchronous digital systems [2] with broaden sets of relations for assembly tradeoffs, possibility to acquire the majority of the clock frequency and the density of gratifying limitation on the logic path delay for Power requirement which is equally important. More than 50% of the random-logic power in Silicon on Chip is consumed by Flip-Flop which is appropriate to for redundant transition of the internal nodes, when the output and the input are in the identical position [3].

Several low-power techniques has been intended, but all of them expand transistor-count penalty, the majority significant to amplifying in the size, which it is too valuable since Flip-Flops typically account for 60% of random-logic area. As a result, in order to attain low-

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power designs, it is most important to reduce the clock technique power. In order to minimize the clock technique power, a clock voltage swing is flourishing to decrease [4]. Since the power consumption of the clock technique is related to the clock swing or to the square of the clock swing. Superior Pipelining method helps to achieve high speed in synchronous systems. The above technique deals with the latency which is correlated with the pipeline elements, such as the Flip-Flops and latches [6] which extremely helps to reduce the pipeline overhead by removing the delay and area connected with one or more logic step used in the Flip-Flop.

## 2. Proposed System

TRANSISTOR REDUCED FLIP-FLOP

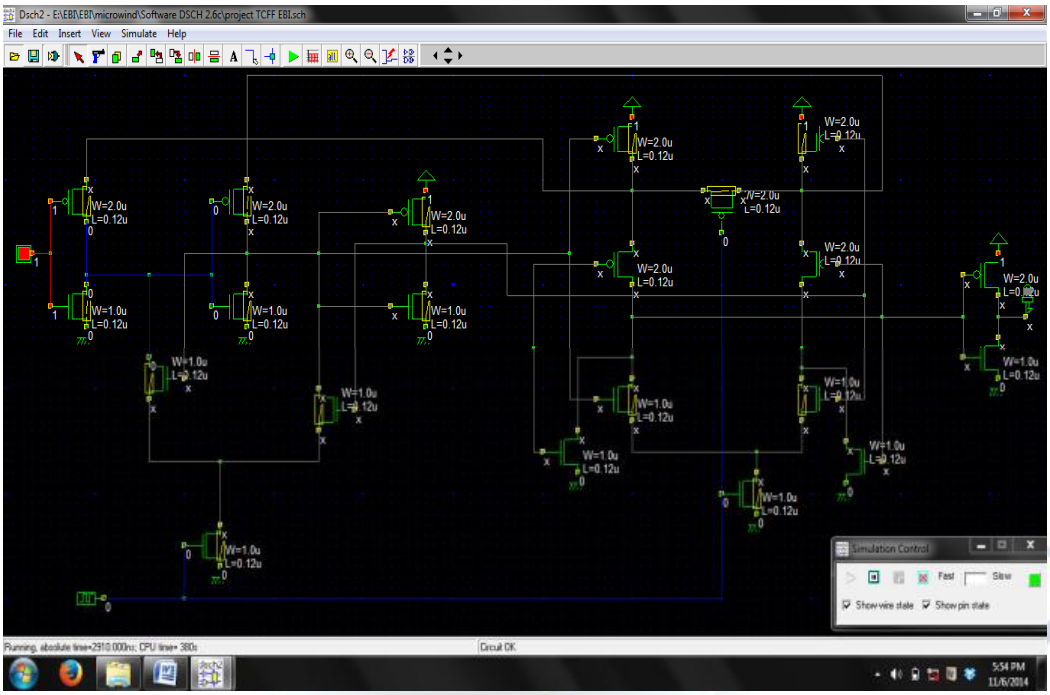


Figure 1. Transistor level schematic diagram of TDFF

The Proposed compressed FF transistor level schematic diagram is designed using the less number of transistor. This is made achievable by grouping and integration of the P-Channel MOSFET (PMOS) and N-Channel MOSFET (NMOS) transistors in which the clock applied with two states. In the first level the clock level is applied with extremely low state. Figure1 shows the clock state is low, in which the clock turns on which is associated with the PMOS transistor and the master latch which can develop into the data input mode. The input level represents Off when the clock is in zero state such that the voltages represents in both the level1 and level2 leads to the power-supply off, the NMOS transistor connected to clock turns on, and the slave latch becomes the information output mode.

During this circumstance, the information in the master latch is turning over to the slave latch, and leads the output to glow by keeping all nodes with entirely static and full

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swing. When the master latch and the slave latch develop into active interchange mode then the current from the power supply will not flow into the master and the slave latch concurrently. Hence, timing deprivation is small on cell appearance; even still several transistors are communal with no raise in transistor size. This Flip-Flop consists of extraordinary categories of latches in the master and the slave branch. The slave latch has renowned Reset-Set type, whereas the master-latch has irregular single data-input type.

Very Large Scale Integration (VLSI) designs require Flip-Flops with advance functions such as approximating scan, reset, and set. The performance and area of the cells are as well significant in VLSI design. These cells are easily recognize by TDFF with less transistor-count when compare with the conventional Flip-Flops. The transistor level schematic diagrams of the TDFF with scan reset and set can be designed with related structure. These Flip-Flops have only three transistors connected to the clock. Hence the power dissipation is more or less equivalent to TDFF.

## 3. Layout Process in TDFF

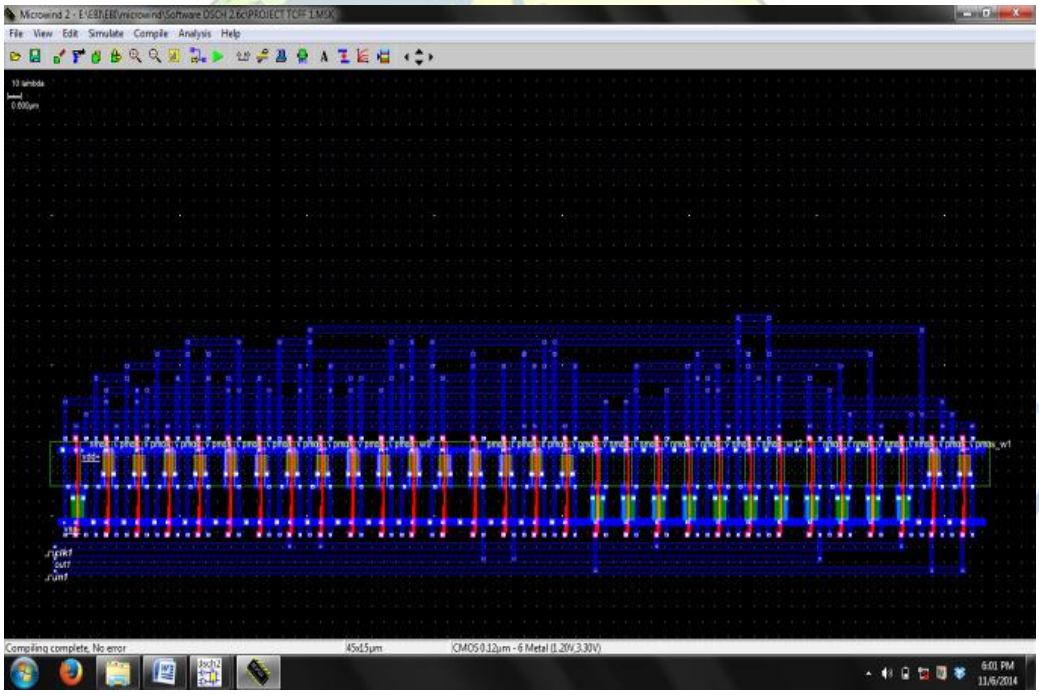


Figure 2. Layout diagram of TDFF

The proposed Transistor Reduced Flip Flop layout is shown in Figure 2. In this type the connections between the pins of the NMOS and PMOS are made by routing with metallic regions. This layout composed of 9 PMOS transistors and 12 NMOS transistors with one number of clocks. The blue color represent p+ diffusion in the layout, the green color represent N+ diffusion. The PMOS and NMOS connect with the metal via contact. White colour represent the node box in the layout represent the contact.

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## 4. Results and Discussion

This section deals with the analysis of the Transistor Reduced Flip-Flop. Simulation results are based on the Delay and Gain analysis

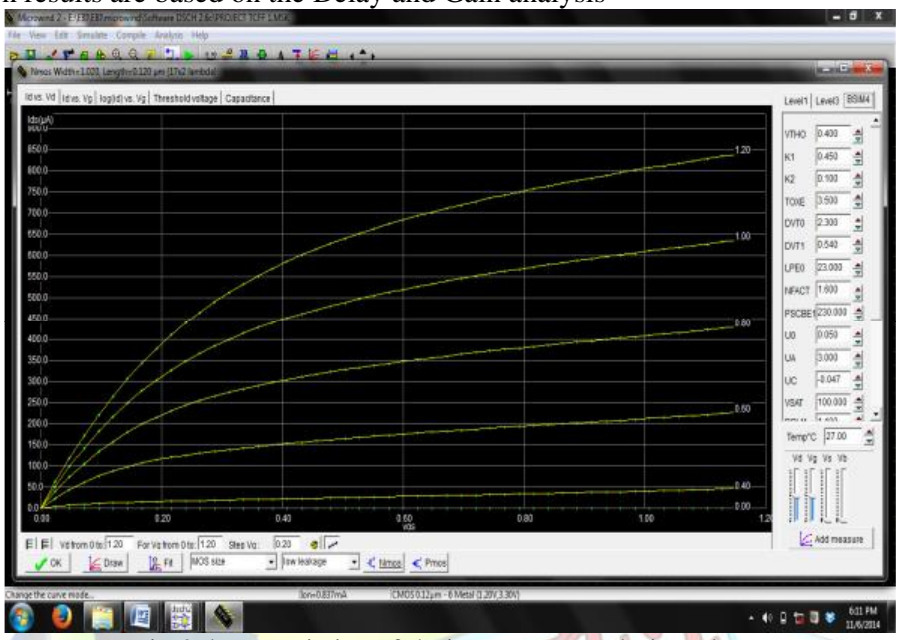

Fig 3characteristics of drain current Vs drain voltage

The simulation showing the characteristic of the drain current and the voltage are shown in the Figure 3. The proposed system result and the output waveform are obtained after the simulation. The output waveform of the Transistor Dense Flip Flop is analyzed with the characteristic waveform of current and the voltage of drain source. The layout and the simulation for the proposed system are completed with the final output obtained in three dimensional view of the system.

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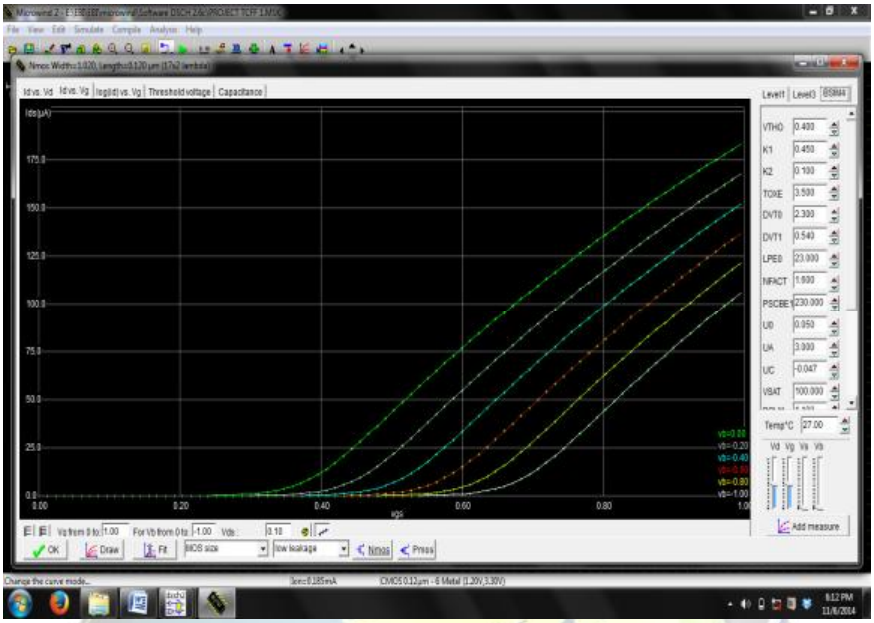

Figure 4 characteristics of drain current Vs gate voltage

The graph varies linearly in the active region once it crosses the cutoff region. The cutoff and active region of the drain source current versus gate source voltage characteristic graph is shown in the Figure 4.

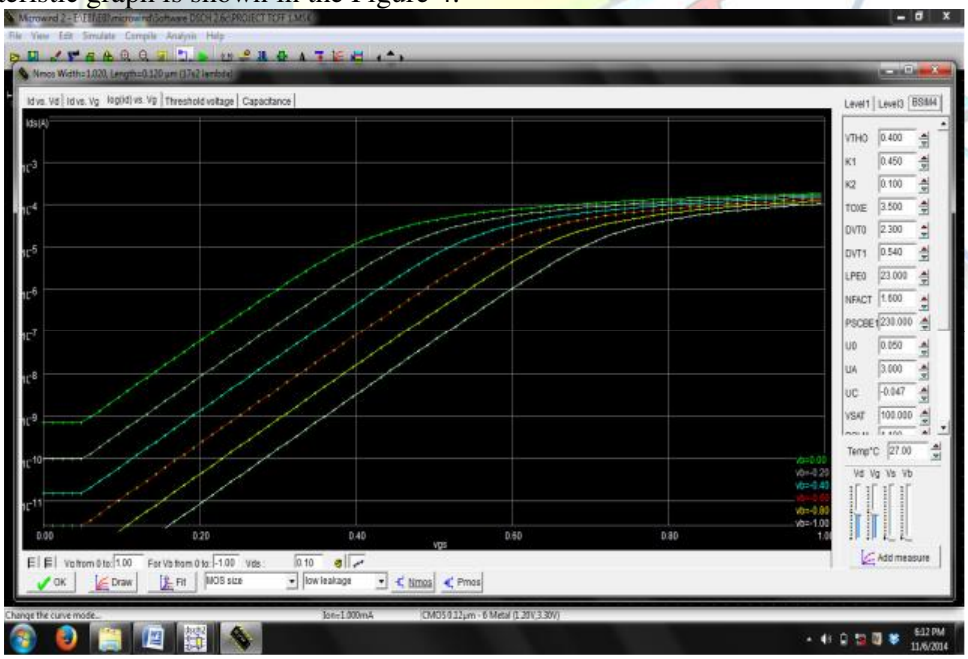

Figure 5 characteristics of logarithmic drain current Vs gate voltage

Figure 5 shown in the characteristics of logarithmic drain current versus gate voltage at varies levels of log Id. The saturation level is reached once it crosses the active region

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linearly. The clock pulse and the input propagation at the various nodes are computed with every unit which succeeds to the potency of the new TDFF structure. No deviation occurs practically among the various cell variation since the TDFF requires less wiring resources in the layout, it apply metal3 which is matched to Topological Grouped Flip Flop (TGFF) by using up to metal2. Other than the number of transistors in TDFF is lesser than that of the amount used in TGFFs, TDFF can be implicit in a modest way with a smaller amount of cell area than the conventional one.

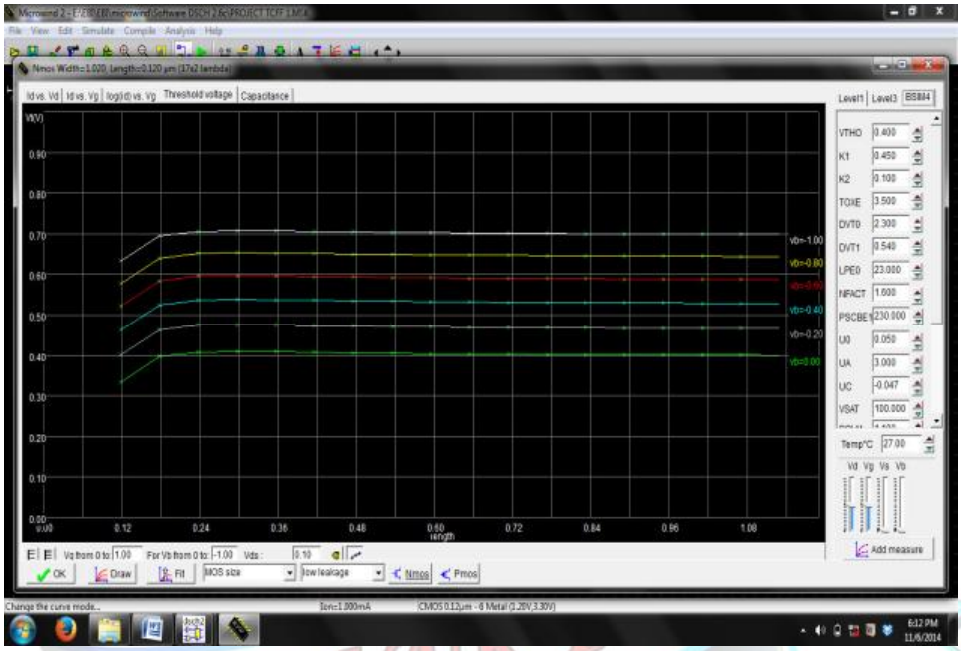

Figure 6 characteristics of length Vs Threshold voltage

Figure 6 shown in the length versus threshold voltage of the Proposed Flip Flop at the various levels of the threshold voltage. If the cell replacement process is executed after pre-layout and timing analysis. In the next section, how effectively TDFF is applied to actual chip design is shown by placement and routing experiment and also a three dimensional view displayed.

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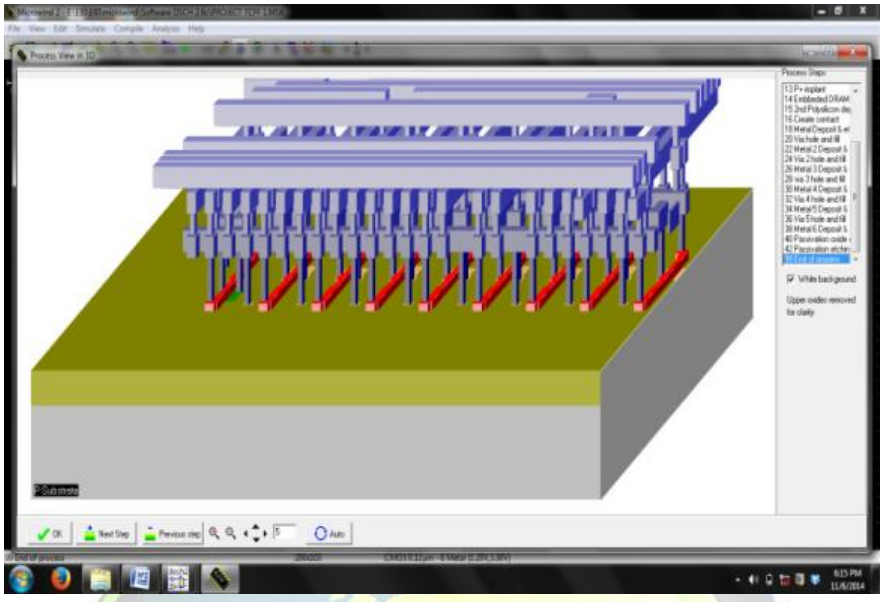

Figure 7. 3-D view of Transistor Reduced Flip-Flop

Figure 7 shows a three dimensional view of the proposed TDFF with the final output. An extremely low-power FF, TDFF, is proposed with Topological Compression design methodology. TDFF has reduced the number of transistor in almost all range of the data activity compared with the other Flip-Flops. Since data input or data output operation is controlled by one clock related transistors in 2-1 transistors of a TDFF circuit does not affect cell area much. A variety of clock-related transistor sizes, TDFF can be applied to various speed systems, and it can reduce the whole chip area and number of transistor count.

## 5. Performance Analysis

The performance of TDFF is verified by Microwind simulation with CMOS technology. The relationship with other Flip-Flops, the same transistor range is used for every transistor in which each FF includes TDFF in order to simulate the same conditions. Some standard values are implicit for transistor sizes for the reason of comparison; 2.0 um for width and 0.12 um for length in PMOS, and 1.0um for width and 0.12 um for length in NMOS with the standardize power indulgence versus number of clock measures for other Flip-Flops. TDFF consumes the least power among them in almost all ranges of numeral clock.

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Table 1

Performance analysis of Conventional Flip - Flop and Transistor Reduced Flip - Flop

| S.NO | Flip -Flop | Delay | Number of clock | Number of transistor |
|---|---|---|---|---|
| 1 | Conventional Flip – Flop | Rise delay - 0.009ns<br>Fall delay - 0.005ns<br>Propagation delay – 0.007ns | 4 | 28 |
| 2 | Transistor Reduced Flip – Flop | Rise delay - 0.007ns<br>Fall delay - 0.003ns<br>Propagation delay – 0.005ns | 1 | 21 |

Table 1 shows the performance analysis of conventional Flip-Flop and TDFF. Rise delay for Conventional Flip-Flop is 0.009ns whereas the Rise delay for TDFF is 0.007ns. Fall delay for Conventional Flip-Flop is 0.005ns whereas the fall delay for Proposed Flip-Flop is 0.003ns.Time taken for Propagation in the Conventional Flip-Flop is 0.007ns but the time taken for Propagation in the TDFF is 0.005ns only. Number of Clock in the Flip-Flops in a VLSI is greater than TDFF. The area condense of TDFF is 66% lower than that of TGFF.

Table 2 Performance analysis of CFF's and TCFF

| S.No | Parameters | Conventional Flip -Flop | Topologically Dense Flip-Flop |
|---|---|---|---|
| 1 | Metal Capacitance | 3.20 fF | 2.86 fF |
| 2 | Metal Resistance | 17 ohm | 15 ohm |
| 3 | Inductance | 0.04 nH | 0.04 nH |
| 4 | Cross talk | 0.11 fF | 0.10 fF |
| 5 | Diffusion | 0.24 fF | 0.24 fF |
| 6 | Rise delay | 0.006 ns | 0.008 ns |
| 7 | Fall delay | 0.005 ns | 0.003 ns |
| 8 | Transistor count | 28 | 21 |

The table 2 represents the performance of TDFF is demonstrated by SPICE simulation with CMOS technology. For comparison with other FFs, the same transistor size is applied for every transistor in each FF including TDFF in order to simulate the same conditions. Some standard values are assumed for transistor sizes for the purpose of comparison; 0.24 m

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for width and 0.04 m for length in PMOS, and 0.12 m for width and 0.04 m for length in NMOS. The normalized power dissipation versus data activity compared to other FFs. TDFF consumes the least power among them in almost all ranges of data activity.

These recapitulate the transistor-count, the Clock pulse delay, the setup/hold time, and the power ratio of each Flip-Flop. As for delay, TDFF is approximately the same as the conventional Flip-Flop, and better than other Flip-Flops. Setup time is the only poorer parameter to the conventional FF, and about 40 ns larger than the value of the predictable one. For hold time, TDFF is better than the conventional FF. In outline, only setup time is great, but TDFF keeps spirited presentation to the conventional and other Flip-Flops. The supply-voltage is reliant of the Clock-Pulse. Number of clock required for existing method is four, which is greater than the proposed method. Number of clock required for proposed TDFF method is one.

## 6. Conclusion

The existing system which is the Conventional Flip Flop the transistor count is more which is 28 transistors so that the area occupied by the system is more and with more delay so that the speed is less. In order to overcome this condition, the proposed system that is the TDFF uses the grouping and merging methodology so that the transistor count is less which is only 21 transistors hence the area is greatly reduced. The delay is further reduced by that the speed of the system is increased.

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