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Efficient approach to design a reversible fault tolerant division unit using Quantum dot cellular automata

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Abstract: Division is one of the important arithmetic operation that can be used in scientific computing and multimedia application. This division operation has been performed with reversible logic. In reversible logic there is no loss of information and also it is a parity preserve. The reversibility provide one to one mapping between input and output vectors. This paper presents a binary floating point division algorithm which can be used to perform n-bit reversible fault tolerant binary division. This algorithm performs precision rounding to its nearest. It also deals with the implementation of low latency software for binary floating point division. The proposed division operation has been performed with a newly proposed reversible gates such as KA gate 1, KA gate 2, KA gate 3, KA gate 4 and KA gate 5. The proposed new gates has a low quantum cost compared with an existing gates. These gates can be used to construct the components of division circuit. The proposed division circuit which can be constructed with the components such as reversible fault tolerant multiplexers, parallel-in-parallel out (PIPIO) left shift registers, D Latch, rounding register, normalization register and parallel adder. In this components the parallel adder has low quantum cost compared with the existing ones. The proposed division circuits performs more efficient than the previous circuits. The efficiency of proposed design has been shown interms of number of gates required, garbage output, quantum cost and maintaining their constant inputs. The proposed n-bit reversible fault tolerant binary division circuit can be simulate using a QCA designer tool.

Keywords**: Reversible logic, Fault tolerant, Quantum Cost, Delay.**

I. INTRODUCTION

One of the most promising nanotechnologies which can replace the present transistor based CMOS technology is the Quantum-Dot Cellular Automata. The major advantages of this technology are lesser power dissipation, improved speed and dense structures. Currently all logic gates are based on CMOS technology. With the current pace of scaling CMOS technology is set to hit a roadblock in the next few years, where it cannot be further scaled down due to several reasons like as tunnel currents, quantum effects, sub threshold leakage, fabrication costs and interconnect delay etc. Logic Design with Quantum Dots is one of the most recent technologies being which allows scaling to continue to atomistic dimensions. In this particular logic design approach Quantum Cells are arranged in particular fashion to define the logic.In (1) they presented a radix-10 division unit that is based on digit-recurrence algorithm. This will able to reduce the delay of the circuit. But it requires more iteration. The square root and division can be implemented in a same circuit by using Radix-4 SRT division recurrence method in (2).It has low delay and the Power consumption is high. Division is one of the important arithmetic circuit. It can be performed with reversible logic. In (3) they presented a novel design of sequential division circuit using reversible logic. In this two approaches has been used such as restoring division and non

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restoring division. They achieved a fixed point division but it works only on positive integer.

Restoring a remainder of division which plays a vital role in each stages. Then in (4) used a restoring binary division algorithm to perform a restoring operation in the circuit which gives throughput. The issues related to this paper is the circuit becomes large and performance is slow. N-bit new fault tolerant reversible divider has been proposed in (5).In this they used Two approaches to perform the division. They are n+1-bit fault tolerant reversible PIPO left-shift Register, n+2-bit fault tolerant reversible PIPO left-shift Register. Garbage output and cost low in approach 2 but it is low in approach 1.Pritam Bhattacharyya (6) presented a efficient binary division algorithm to performed binary division operation in unsigned integer. It requires lesser number of steps taken for performing the division .In worst case time consumption is high. The division operation can be performed in floating point divider in (7).They used two approaches conventional array divider and high speed array divider. Conventional array divider has high delay and high speed array divider has high cost.

Used a non-restoring binary divider algorithm in (8) to perform a design of non-restoring binary array divider in QCA. It is time-saving and easy to control .The issues is amount of cell is high. Precision is essential in division for this in (9) they used a Simplified single precision floating point arithmetic to perform division and square root operations. The Goldschmidt's algorithm can be used to Floating Point Division and Square root with precision. In floating point division area only reduced and in floating point square root delay only reduced.

In (10) they presented a one digit arithmetic logic unit for quantum arithmetics. This will effect in arithmetic operation with respect to minimization of cost metrics. This will effective in cost but it has no constant input. To optimize revesible logic blocks they used groovers algorithm in (11).Then this achieved a block with minimum cost but the hardware complexity is high in (12). They performed n-bit reversible fault tolerant binary division using an effective division algorithm. This gives reduced step for division operation and quantum cost is high.

A. Background and Existing division algorithm

In arithmetic circuit the basic operations are addition, subtraction, multiplication and division. These operation can be used to perform the logical operation. An algorithm can be find out to perform these operation. The algorithm should be able to process these basic operation and also it satisfy the efficiency constraints. This Section briefly explain the existing division algorithm.

a. Floating-point division algorithm

This algorithm presents the AMD-K7 IEEE754 and *87 compliant floating point division. It has high initial approximation performance. It assists in achieving low division latencies at high operating frequencies. It also describe a novel time sharing technique. But it requires extra multiplier hardware to support division.

b. Floating-point division using a Taylor-series expansion algorithm

In this algorithm fused floating point division unit can be implemented based on a Taylor-series expansion algorithm. The resulting arithmetic unit also exhibits high throughput and moderate latency as compared with other floating-point unit (FPU). This algorithm achieves fast computation and compute the higher-order terms significantly faster than traditional multipliers with a relatively small hardware overhead. It consumes a large area because the architecture consists of four multipliers.

c. Efficient division algorithm

This new technique can be used for binary floating point numbers. This division method based on four steps: In the First, it considers floating point data and rounding. In the Second step, it performs correctly rounded division. In the Third step, it performs correct rounding from one sided approximations. Finally, it calculates the result of the binary floating point division operation. It has high speed and low power consuming divider but the quantum cost is high

B. Basics of reversible logic

a. Reversible logic

Reversible logic is a emerging alternative for application in low power design and quantum computation in now a days due to its ability to reduce power dissipation in low power VLSI and ULSI design reversibility plays a vital role in quantum computation. The quantum gates and circuits which must be reversible.

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b. Reversible gate

Reversible gate can provides the circuit which is in the form of the number of inputs is equal to the number of output and there is one to one mapping between input and output vectors.

c. Optimization parameters

- *Garbage output:* It refers the unwanted or unused output of a reversible gate. It can be used maintain the reversibility of the circuit. This outputs are not used in the synthesis of function or further calculation.
- *Quantum cost*: Reversible gates can be measured by quantum cost. Every quantum circuit can be built by using 1×1 and 2×2 quantum primitives. The quantum gates are described in matrix form. In reversible logic the quantum cost can be calculated as 1×1 and 2×2 reversible gates. The cost of each 1×1 and 2×2 primitive's gate is taken as unit cost.
- *Delay:* The delay of the circuit refers the maximum number of between input and output path.
- *Constant input*: The constant inputs are 0 and 1 that must be maintained in a reversible logic.

I. PROPOSED FAULT TOLERANT GATES

Reversibility recovers bit loss but is not able to detect bit error in circuit. Fault tolerant gates which means the hamming weight of its input and output are equal. Parity preserving is used to realize fault tolerant in the circuit. Fault tolerant means even if a circuit is defect then it able produce a output without the consideration of its defect.

Proposed fault tolerant reversible gates

In this paper different gates can be proposed to perform the division operation .The gates are KA gate 1, KA gate 2, KA Gate 3 and KA gate 4. The details of these gate can be described in this section.

a. KA gate 1

KA gate 1 can operated as copying gate. It has 3×3 input(Iv) and output vectors (Ov).It can be represented as Iv=(A,B,C)and Ov=(P,Q,R). Block diagram of KA gate 1 is shown in Fig.6. It has a quantum cost of ten. It use a logic if (a,b=0, c=0), then the output vector(Ov) will be(a,a,a). The truth table of KA gate 1 is given in Table1.

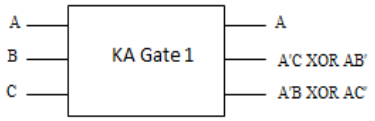

Fig.6.Block diagram of KA gate 1

b. KA gate 2

This is a parity preserving reversible gate which can perform all basic operation. This gate can extensively used by researchers. It is a 3×3 input (Iv) and output vectors (Ov).It can be represented as Iv=(A,B,C)and Ov=(P,Q,R).

Table 1
Truth table of the fault tolerant KA Gate 1

Inputs			Outputs		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Block diagram of KA Gate 1 is shown in Fig.7. It has a quantum cost of ten. This gate can be used to perform swappin operation. The swap operation can be performed between second and third input. If A=1, then the inputs B and C are swapped. If A=1, there is no swapping operation

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can performed the then outputs P, Q and R are directly connected to inputs. The truth table of KA gate 2 is given in Table 2.

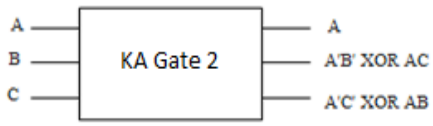

Fig.7. Block diagram of KA gate 2

Table 2
Truth table of the fault tolerant KA Gate 2

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	1	1	1
1	1	1	0	1	0

c. KA gate 3

It has 4×4 input (Iv) and output vectors (Ov).It can be represented as Iv=(A,B,C,D)and Ov=(P,Q,R,S). Block diagram of RR is shown in Fig.8. KA gate 3 has a quantum cost of nine. The truth table of KA gate 3 is given in Table3.

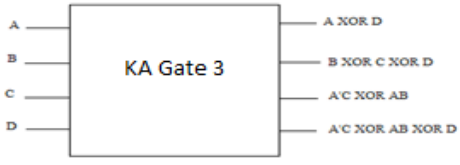

Fig.8.Block diagram of KA gate 3

Table 3
Truth table of the fault tolerant KA gate 3

Inputs				Outputs			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	1
0	0	1	0	0	1	1	1
0	0	1	1	1	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	1	0	0	1
0	1	1	0	0	0	1	1
0	1	1	1	1	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	0	1	0	1
1	0	1	0	1	1	0	0
1	0	1	1	0	0	0	1
1	1	0	0	1	1	1	1
1	1	0	1	0	0	1	0
1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	0

d. KA gate 4

It perform the copying operation then this gate can be used as copying gate. It has 4×4 input (Iv) and output vectors (Ov).It can be represented as Iv=(A,B,C,D,)and Ov=(P,Q,R,S,). Block diagram of KA gate 4 is shown in Fig. 3. It has a quantum cost of fourteen. Its truth table shown in table 3.

Fig.9. Block diagram of KA gate 4

III. Proposed fault tolerant division method

A. Proposed method

In arithmetic operation division is one which is in various field in day to day life. In microprocessor floating point arithmetic is an essential feature. It is indispensable

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and achieve a high speed and low power consuming divider. This algorithm has low latency and time complexity. It deals with the implementation of low latency software for binary floating point division .It is used to provide correct rounding to its nearest even. The new algorithm is named as binary floating point division algorithm which can be used to perform the division operation efficiently.

Algorithm 1 will describes the operation of binary floating point division. The advantage of this algorithm is it reduces the

Table 4
Truth table of the fault tolerant KA gate 4

Inputs				Outputs			
A	**B**	**C**	**D**	**P**	**Q**	**R**	**S**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	1	0	1	1
1	1	0	0	1	1	1	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	0	1
1	1	1	1	1	1	0	0

number of operation required for binary division operation. It achieves maximum efficiency in reducing the number of addition and subtraction to a minimum.

In Algorithm1, the number of positions shifted may be one less than, equal to, one more than that require to normalize $D^{(s)}$.It occurs because simple normalization will not necessarily result in the best decomposition for Q. If we knew the best decomposition of Q (which as yet we do not), then each successive shift (from left to right) should stop with the binary point at the right of a position requiring an operation.

Algorithm1. Algorithm for Proposed binary floating point division operation

Division (D = YQ, Y is normalized)

1. set i =0
2. set s = 1
3. if (Y>D), form remainder, $D^s = D^{s-1} - Y$.
4. if (Y<D), form remainder, $D^S = D^{S-1} + Y$.
5. if (D^S<0), set Qi=0.
6. if ($D^S \geq 0$), set Qi = 1
7. normalize D^S .
8. calculate correct rounding from one sided approximations of D^S.
9. if (D^S<0), set Q0+α = 0 and the following bits are units.
10. if ($D^S \geq 0$), set Q0+α = 1 and the following bits are zeros.
11. increment s (for the next step).
12. set i = i+α.
13. if (i = number of bits),end the process.
14. go to Step3.

The procedure for algorithm1 is summarized as below, the process ends if i reaches the number of bits desired in the quotient. Then assume that the binary point is to the far left of each word, that the denominator Y is positive and normalized (its most significant bit a unit), that the numerator D is positive, and that D<Y, with D either normalized or with a single zero after the binary point.

The first step is to form the first remainder, D'= D-Y. Since, with our initial assumptions, D' is negative, the negative loop of Algorithm 1 is followed. If, D' has α zeros to the right of the binary point, then the quotient Q has atleast α-1 units to the right of the point. (In this initial step, Qi = 0 for i = 0 means merely that Q<1.) Now, D' is normalized and the second remainder, D" = D'+Y, is formed. If, D" is negative, then $Q_0+\alpha = 0$, and the following bits are units. If,

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D" is positive, then $Q_0+\alpha = 1$, and the following bits are zeros. The procedure continues in the way, differencing and normalizing each time, and determining Qi and Qi+1 through $Q_{(i+\alpha)+1}$ at each step.

B. Proposed design of division unit

The proposed design of reversible fault tolerant binary division circuit consists of reversible multiplexers(MUXs), registers, parallel-in–parallel-out (PIPO)left-shift registers, D-Latch, rounding and normalization registers and parallel adder. These circuits can be used to built a reversible fault tolerant division circuit.The proposed division circuit is compact compared to previous design.

a. Proposed reversible fault tolerant MUX

The reversible n-bit fault tolerant mux(fig.10.) can be designed using a KA gate 2 which has three inputs and three output but in mux one is select input S and other two inputs are A1A2A3…An and B1B2 B3…Bn and it has two unwanted ouput. The mux can be performed based on the condition. If s=0,then (Z1Z2Z3…Zn)=(A1A2A3…An) and if s=1,then (Z1Z2Z3…Zn)=(B1B2B3…Bn). It requires n KA gate 2, generates n garbage outputs and needs 10n quantum cost.

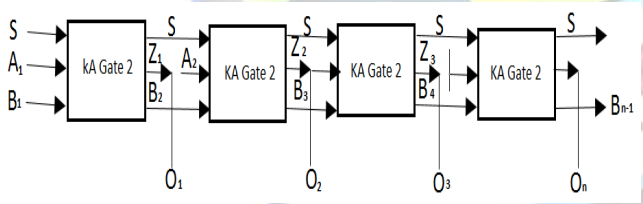

Fig.10. 2-Input n-bit reversible fault tolerant MUX

b. *Proposed reversible fault tolerant D-Latch*

This D latch is shown in fig.11. This D latch is constructed using a KA gate 3 which has four input and four output. In this circuit the third input and output are connected in a feedback path. It requires one KA gate 3, generates one garbage output and needs nine quantum cost.

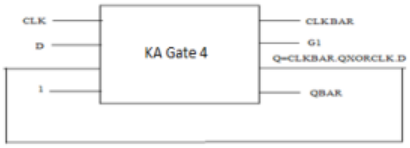

Fig.11.Reversible fault tolerant D latch using KA gate 4

c. Proposed reversible fault tolerant PIPO left shift register

Fault tolerant PIPO left shift register shown in fig.12. This PIPO left shift register is composed of KA gate 1, D latch and KA gate 4. This register work based on the condition shown in table 5.During clock pulse, If SV and E are 0 (low), left-shift is performed. If SV is 0 and E is1 (high), parallel load is performed. Then, input bits Ii are loaded into the left-shift register and outputs are taken from the Q output. When SVis1, the reversible fault tolerant PIPO left shift register saves its current value.

Qi can be obtained as

$$Q_i^+ = SV'.E.I_i + SV'.E.Q_{i-1} + SV.Q_i$$

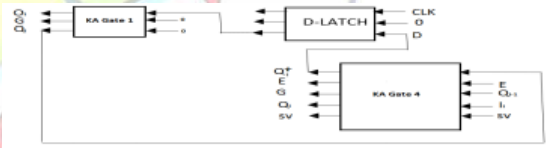

Fig.12. Reversible fault tolerant PIPO left sift register

Table 5
Control inputs of a fault tolerant D latch using KA gate3

SV	E	Output, Q_i
0	0	Q_{i-1} (left shift)
0	1	I_i (parallel load)
1	x	Q_i (no change)

It requires 3n reversible gates, (3n+1) garbage outputs with 43n quantum cost.

d. Proposed reversible fault divisor tolerant register

The divisor register is constructed using a reversible fault tolerant D latch which n gates, produces n garbage outputs and needs 9n quantum cost. It is shown in fig.13.

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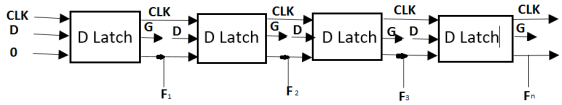

Fig.13.Reversible fault tolerant divisor register

e. Proposed reversible fault tolerant rounding register

This rounding register is composed of KA gate 1 and D latch gate. This performs the rounding operation nearest to the even. It register requires two reversible gates, two garbage outputs and nineteen quantum cost. It is shown in fig.14.

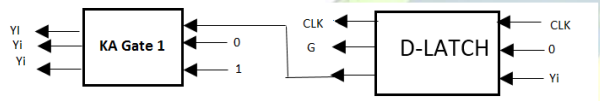

Fig.14.Reversible fault tolerant rounding register

f. Proposed reversible fault tolerant normalization register

This register is designed using the D latch which is used for normalize the divisor on each step. It requires one reversible gate, one garbage output with quantum cost of six. It is shown in fig.15.

Fig.15.Reversible fault tolerant normalization register

g. *Proposed reversible fault tolerant parallel adder*

In this paper a new reversible fault tolerant full adder gate is proposed. This gate is named as KA gate 5. This gate can be used to design a parallel adder. The truth table of this gate is construct and verify the input and output pattern according to the truth table 6. It is a parity preserving reversible gate. It has a quantum cost of twenty four. It is shown in fig.16.

Table 6

Truth table of the KA gate 5

Inputs					Outputs				
A	B	C	D	E	P	Q	R	S	T
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	1	0	1
0	1	0	0	1	0	1	1	0	0
0	1	0	0	1	0	1	1	0	0
0	1	0	1	1	0	1	1	1	0
0	1	1	0	0	0	1	0	1	0
0	1	1	0	1	0	1	0	1	1
0	1	1	1	0	0	1	0	0	0
0	1	1	1	1	0	1	0	0	1
1	0	0	0	0	1	1	1	0	0
1	0	0	0	1	1	1	1	0	1
1	0	0	1	0	1	1	1	1	0
1	0	0	1	1	1	1	1	1	1
1	0	1	0	0	1	0	0	1	0
1	0	1	0	1	1	0	0	1	1
1	0	1	1	0	1	0	0	0	0
1	0	1	1	1	1	0	0	0	1
1	1	0	0	0	1	1	0	1	1
1	1	0	0	1	1	1	0	1	0
1	1	0	1	0	1	1	0	0	1
1	1	0	1	1	1	1	0	0	0
1	1	1	0	0	1	0	1	1	0
1	1	1	0	1	1	0	1	1	1
1	1	1	1	0	1	0	1	0	0
1	1	1	1	1	1	0	1	0	1

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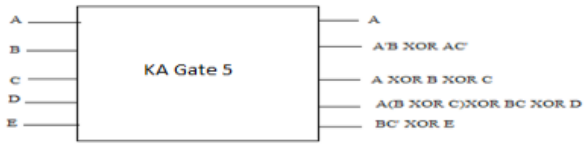

Fig.16. Reversible fault tolerant KA gate 5

KA gate 5 act as full adder shown in fig.17. The comparison between proposed and previous fault gates is shown in table 7.

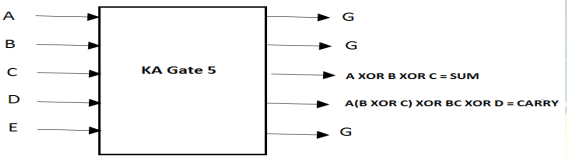

Fig.17. KA gate 5 as a reversible fault tolerant full adder

Table 7
Comparison between proposed and previous gates

KA Gates	Number of Cells used	Area	Simulation Time
Fredkin gate [13]	187	0.19µm^2	33sec
DKG gate [13]	752	1.24µm^2	16sec
MKMD GATE [13]	456	0.52µm^2	45sec
TR gate[13]	113	0.20µm^2	11sec
KA Gate 1	**169**	**0.19µm ^2**	**5sec**
KA Gate 2	**121**	**0.13µm ^2**	**3sec**
KA Gate 3	**116**	**0.19µm ^2**	**4sec**
KA Gate 4	**101**	**0.17 µm^2**	**4sec**
KA Gate 5	**244**	**0.42µm^2**	**7sec**

Using this proposed gate a (n+1)-bit reversible fault tolerant parallel adder is designed shown in fig.18. It can be

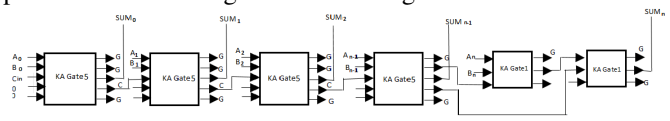

Fig.18. (n+1)-bit reversible fault tolerant parallel adder

implemented using (n+2) reversible gates, garbage outputs is 48, quantum cost 12 and constant input 8.

C. Proposed reversible division circuit

A New Reversible Fault Tolerant n-bit divider circuit where n is the number of bits of dividend and divisor. The division unit is designed with the proposed New Reversible Fault Tolerant gates, which are parity preserve.

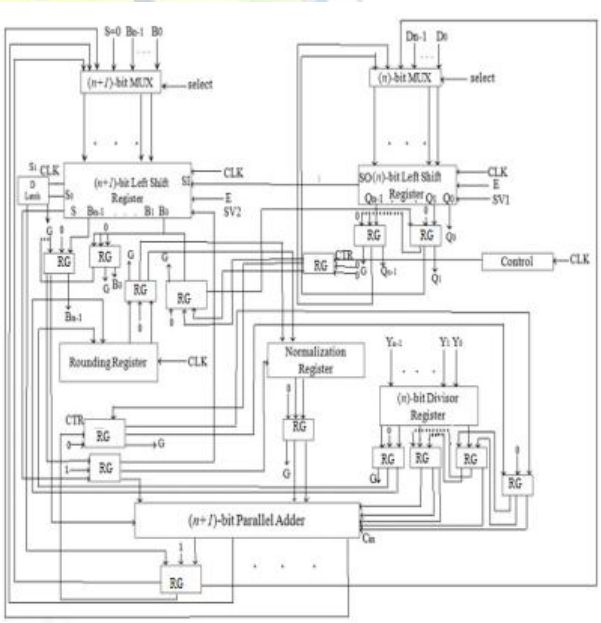

Fig .19. Block diagram of the n-bit reversible fault tolerant division circuit

An algorithm has been used to reduce the number of steps required for performing division operation.

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Division method consists of four steps:

- Considering Floating-Point Data and Rounding.
- Performing Rounded Division as per the Algorithm.
- Performing Rounding one sided Approximations.
- Calculating the Result of the Division operation.

A fault tolerant reversible divider is designed based on this algorithm. In this division circuit it consists of fault tolerant reversible components like reversible shift register, reversible parallel adder, D-latch, Multiplexer, Left shift register, rounding and normalization registers. Using these faults tolerant Reversible Gates the Quantum Cost, Garbage Outputs and Gate Counts of the design can be reduced.

Fig.19. shows the proposed design of the reversible fault tolerant n-bit division circuit. It has two PIPO reversible left-shift registers: one is (n+1)-bit named 'A' and another is n-bit named as Q. It also contains an n-bit reversible register to store the divisor, one D-Latch is used to maintain S1, one Reversible gate is used as a one bit, two-input MUX. The design also contains a rounding register to calculate the rounding to the nearest even and a normalization register for normalizing the divisor on each step. Initially, S = 0, B (B_{n-1}, B_{n-2}…B_0) = 0, D (Dn_{-1}, D_{n-2}…D_0) = dividend, Y (Yn-1, Yn-2…Y0) = divisor and CTR = 0. When the division operation is completed, register Q (Q_{n-1}, Q_{n-2}…Q_0) contains the quotient and B (Bn-1, Bn-2…B0) contains the remainder. If select = 1, then 2-input (n+1)-bit MUX selects S = 0 and B (B_{n-1}, B_{n-2}…B_0) = 0 and n-bit MUX selects dividend D (Dn-1, Dn-2…D0).

During the clock pulse when E = 1 and SV2 = 0, the input S1 = 1 and output data from (n+1)-bit MUX are loaded into (n+1)-bit left-shift register. When SV1 = 0, outputs from n-bit MUX are loaded into Q in parallel. When E = 0, both A and Q act as left-shift registers. Initially, the value of S1 is not important, it is important only after the left-shift of A.Q (A.Q means SO of register Q is connected to S1 of A), thus the value of S is shifted to S1 which is used to select the operation to be performed on A and Y. If S1 is 1, then A+Y is performed, otherwise AY is computed. Addition or subtraction is performed using (n+1)-bit reversible parallel adder. The complement of the Most Significant Bit (MSB) of the sum is loaded into Q_0 bit position of register Q and (n+1)-bit SUM is loaded into A during next clock pulse when select is 0. It requires 2n+1 clock pulses to store the value of quotient into register Q.

Algorithm 2. Algorithm Of Binary Floating Point Divider Circuit

Step 1 : Select =1

Step 2 : count =0

Step 3 : While (true), E=1

Step 4 : if(CLK is high and E=1),

Step5 : if(select=1), inputs are loaded into left shift registers

Step 6 : select=0

Step 7 : else, outputs from rounding registers are loaded into normalizing register

Step 8 : count=count+1

Step 9 : E=0

Step 10 : if(CLK is high), s1 gets the value of s_0

Step 11 : count=count+1

Step 12 : The values of divisor are the inputs of adder

Step 14 : else Q_0 will be 0 during next CLK.

Step 13 : if(the MSB of sum is 0), Q_0 will be 1 during the next CLK

The n-bit divisor is loaded into rounding register through reversible gate. During next clock pulse, the bits of the divisor Y (Y_{n-1}, Y_{n-2}…Y_0) is rounded and loaded into

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normalization register through another reversible gate. On each clock pulse, the remainder results from normalization register and loaded into (n+1)-bit Parallel adder. After 2n+1 clock pulses, control outputs a high signal. This signal is connected to SV1 input of Q register. Thus Q stores the quotient indefinitely. If S is 0, then remainder restoration is not required, SV2 will be high and B will store the Remainder indefinitely. If S is 1, then remainder restoration is necessary. During 2n+1 clock pulse as S1 is 1, restoration is performed by adding Y with A. During the next clock pulse, the correct value of remainder is loaded into A when E is 1. After remainder restoration, S must be 0. This result SV2 to be high and B will store the remainder indefinitely. The working principle of the proposed fault tolerant reversible design is described in Algorithms 1 and 2.

IV. COMPARATIVE ANALYSIS

The performance of the proposed gates with the existing gates can be analyzed. The comparison between the proposed and the existing reversible fault tolerant divider for n-bits is presented in Table 8. In this we achieve a correct high speed divider circuit using the proposed division algorithm.

Table 8
Comparison between the proposed and the existing reversible fault tolerant divider for n-bits

	Existing	**Proposed**
No. of Gates	13n+18	**13n+15**
Garbage outputs	12n+17	**12n+15**
Quantum Cost	67n+69	**74n+61**
Constant Input	10n+17	**9n+21**

IV. CONCLUSION

Divider circuits play a significant role in computational arithmetic operations which can be used in future quantum computers. In this paper a n-bit reversible fault tolerant binary division circuit is proposed where n is the number of bits of dividend and divisor. A new algorithm is proposed to design the compact n-bit divider circuit. This algorithm has been proposed to reduce the number of steps needed for division operation. The proposed circuit is compared with the previous circuit in terms of optimum number of gates, garbage outputs, constant inputs, quantum costs and delay.The comparision results of our proposed design shows that it is more scalable and perform better than existing one. The proposed division circuit was simulated using a tool QCA 2.3.0 to check the correctness of the circuit

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