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DESIGN,ANALYSIS AND IMPLEMENTATION OF VARIOUS FULL ADDER USING GDI AND MGDI TECHNIQUE

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***Abstract* — The design of 1-bit full adders having high performance has analyzed and declared by claiming interest on last few years, among the schemes of high performance, several adders constitute prime class. This paper bestows low power, low voltage and high speed 1-bit full adder circuits are designated. Our full adder approach is mainly based on Gate Diffusion Input and Modified Gate Diffusion Input technique. By weilding XOR style gate logic 28T, 14T, 10T and 8T are contrivanced, which enhances speed and reduces power dissipation at lower supply voltage. The annotation of alternate full adder topologies using GDI and MGDI techniques are reviewed here. The MGDI techniques permutates the circuit to consume less power, delay and to obtain optimized area of deserved circuits, thereby compromising the complexity of desired logic. By considering proposed 1-bit 8T MGDI full adder, the 8-bit ripple carry adder is implemented by using Cadence ORCAD tool. The various full adder styles concedes simulation results using Cadence Virtuoso Schematic Suite Design at 180nm technology, the count of full adders are remitted from 28T to 8T is constructed. By analyzing the comparison coated in this paper for 1-bit full adder, an efficient adder design can be picked up by the designer based on the prime criteria being wanted. As an outcome the proposed 8-bit ripple carry adder is efficient in terms of extent.**

***Index Terms*— Full adder, 8T based MGDI design, CADENCE suite design, Power, Delay.**

A. INTRODUCTION

In this paper we introduces a 1-bit full adder cell that shows faster operation and has less area and power than standard work of full adder. In most of the applications in VLSI, addition plays a major role on basic arithmetic functions such as subtraction, multiplication and division. The full adder cell is the building block of above operations. The main objective is to suppress the power consumption of adders used, for that some techniques has been proposed. The main alliteration of this paper grants the MGDI cell design. The design of MGDI cells are established and compared with CMOS and GDI logic. In CMOS logic style, static CMOS gates are slow since its input should operate both PMOS and NMOS. It has increased delay and area because it utilizes more number of transistors. The GDI cells are used to implement the logic circuits with high speed, low power and

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Provides the disadvantages that it requires twin-well CMOS or silicon on insulator thereby enhances the fabrication cost and complexity circuits. MGDI technique is adaptable for all types designed circuits and overcome the disadvantages of other two logic styles. Here 8-bit Ripple carry adder has been implemented using MGDI technique with reduced power.

The common prime performance parameters for upcoming VLSI systems are speed, area and power consumption. We establish various full adder topologies that includes 28T and 14T CMOS full adder cell, 10T GDI cell and 8T MGDI cell. The design objective becomes equal to the high performance system with portable system's popularity as well as fastest growth of IC's in terms of power density. Commonly RCA are utilized among all the adder cells. It makes the system designers to design the power efficient adders but it is a slow adder, it can be overcome by introducing various topologies of full adder.

Most of the ripple carry adder has been designed using distinguished full adder that achieve some design accents such as power, area, and PDP. By considering those designs with less transistor count have been used to minimize the area. The proposed ripple carry adder circuit with 8T is appliance using CADENCE EDA tool[]. The tool has the features of cadence virtuoso schematic editor that provides exact parameters in the circuit. Cadence virtuoso visualization and analysis gives efficient analysis of design performance, cadence virtuoso layout suite that enhances design layout.

B.CMOS BASED FULL ADDER DESIGN

A network of CMOS has pull down network and pull up network. The PMOS provides '0' weak logic and '1' strong logic whereas the NMOS provides weak '1' and good logic '0' to the rest of the levels. The output has full swing and non-

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degraded voltage levels. In the basic CMOS digital gate the average power dissipation will be the sum of static power, dynamic power and short circuit power. In some cases body effect will be increased because of the design.

a. Full adder cell and operation

The full adder may be shortly described as addition of two single-bit binary values by including input

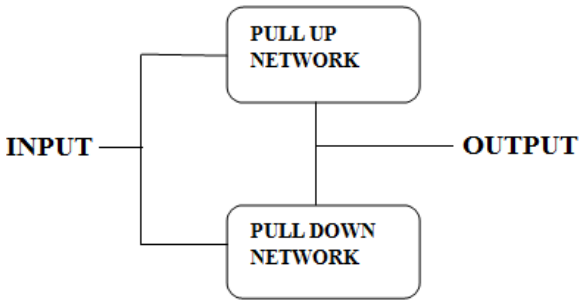

Fig 1: CMOS structure

Carry provides two outputs namely sum and carry. The relative expression between A, B, C, sum and carry are said as

SUM = A xor B xor Cin ……(!)

CARRY = (A and B) or (B and Cin) or (A and Cin)…..(!!)

The truth table of full adder as,

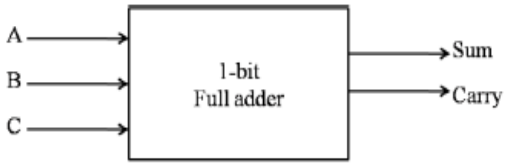

Fig 2: Block diagram of full adder

Table 1:Truth table of 1-bit Full adder				
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig 3: Truth table of full adder

From the different point of view, distinguished logic styles will be investigated. It has the proof that they heed to favor one performance perspective at the expense of others. In other words, the design constraints are different to impose the application that every logic style has its position in the library cell development. Even a suitable style appropriate for a specific function may not be suited for other one. For instance, static model provides robustness against noise effects, thereby provides reliable operation. The issue of easy design will not be reached normally. The design style of CMOS is not area efficient for complex gates with fan-ins. Hence care must be taken when a static logic style is picked up to realize a logic function.

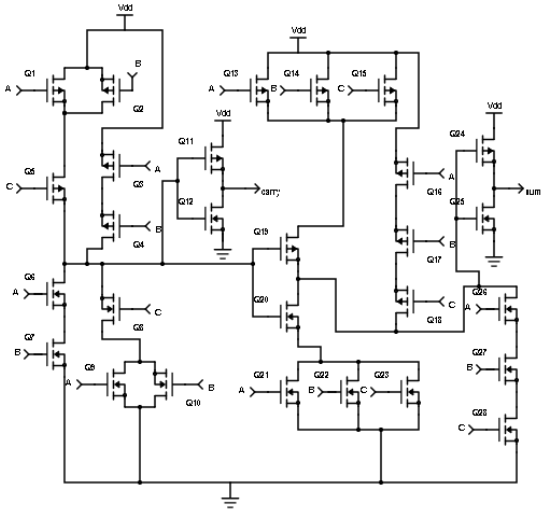

Fig 4: 28T CMOS full adder

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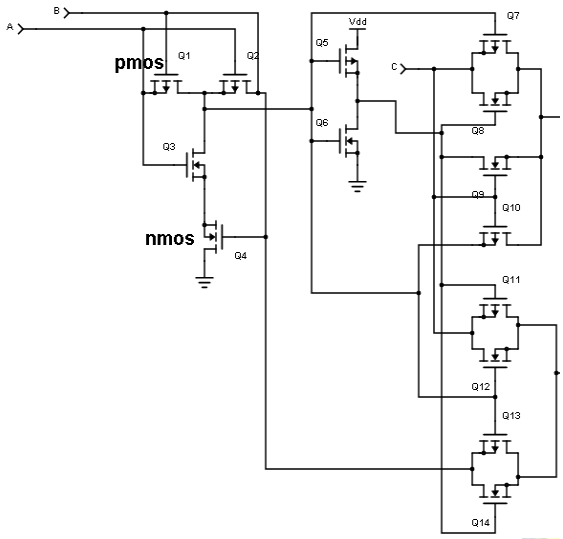

Fig 5: 14T CMOS full adder

The conventional full adder shown in fig 1 and fig 2 are a complementary CMOS ie. C-CMOS full adder with 28T[] and 14T[]. It will be the clubbing of PMOS and NMOS transistors[]. It is known for its scalability and robustness at low voltage supply. It has a benefit of regular layout and voltage scalability deserved for complementary transistor pairs and less number of connecting wires. In this type of full adder, interdependence between signals causes the delay imbalance.

C.GDI Design cell

The structure of GDI cell was first proposed by Morgenshtein []. This technique is used in digital combinational circuit cell

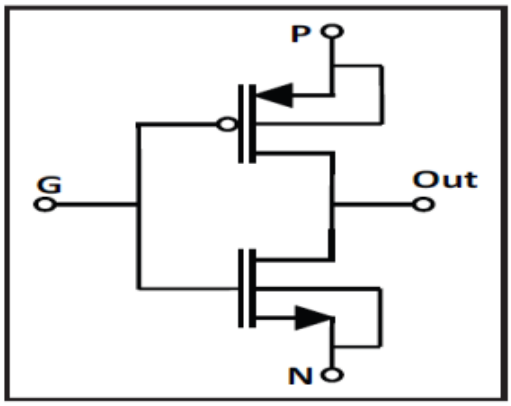

Fig: GDI STRUCTURE

Design for its low power and minimum area. By maintaining the low complexity of logic design, the GDI cell is established. The significant content of GDI based design is the source of PMOS in GDI cell is not wired with VDD and the source of NMOS is not wired with ground. Simple cell of GDI is shown in fig. as first sight GDI cell looks compatible with CMOS inverter but there are few resolvable differences.

GDI cell consists of three inputs (1) common gate input of NMOS and PMOS as G, (2) input to the drain/source of PMOS as P and (3) input to the drain/source of NMOS as N where as CMOS inverter has only single input and output.

Bulks of both PMOS and NMOS are wired to P or N respectively, so it will be self biased at contrast to CMOS inverter. It should be notable that all the functions are not possible in standard P-well CMOS process but can be constructed in Twin-well CMOS or SOI technologies [] in success.

Truth table of GDI cell:

N	P	G	Output	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

Fig: GDI cell truth table

Table exploits how a change of input configuration of the simple GDI cell resembles to a different boolean functions. Many logic functions are complex in CMOS as well as PTL functions, but simple in GDI cell design. Here 10T GDI is proposed with concepts of GDI operation as mentioned above.

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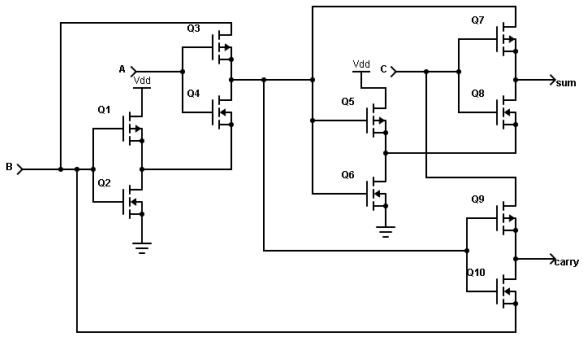

Fig: 10T GDI based adder cell

D. MGDI Design Cell

The state of MGDI cell is almost similar to that of GDI cell contains PMOS and NMOS with four terminals namely common gate input of NMOS and PMOS transistors as G, the outer diffusion node of PMOS transistor as P, the outer diffusion node of NMOS transistor as N and common diffusion node of both transistors as OUT. In modified state GDI cell substrate PMOS is wired to supply voltage VDD and NMOS body is wired to supply voltage ground. In GDI cell, the PMOS body is wired to the drain and NMOS body is wired to source. This initiate the GDI to constant body biasing in MGDI cell in turn raise the loading effect and circuit stability. The CMOS logic gates have been organized in 180nm CMOS technology and it is compared with existing GDI and CMOS logic.

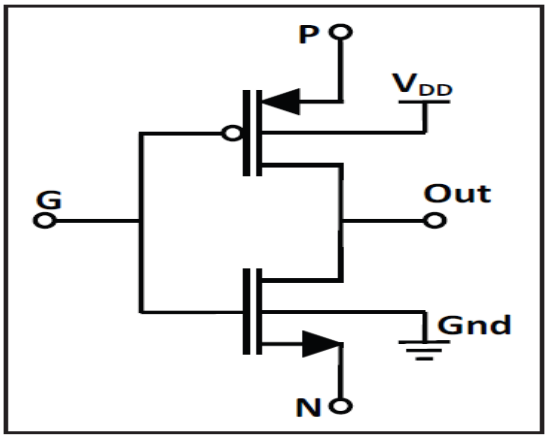

Fig: MGDI CELL STRUCTURE

Fig. shows the construction of modified GDI cell that contains the operation listed below as AND, OR, NOR, NAND, XOR XNOR and MUX. From that the operation of AND gate is elucidated as example. For AND gate, the PMOS drain is wired with A input and the NMOS source is wired with B input. The gate terminal G is wired with A when two of the inputs are zero the PMOS will operates in linear region whereas NMOS in cut off form. when A='1' and B='0' the PMOS will be in cutoff and NMOS is in linear. Similarly for A='0' and B='1' PMOS is in linear and NMOS will be in cut off. Hence for A='1' and B='1' PMOS and NMOS will be in linear thereby provides '1' as output.

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
A	B	A	A+B	OR
B	A	A	AB	AND
B	A'	A	A'B'	NAND
A'	B	A	(A+B)'	NOR
C	B	A	A'B+AC	MUX
0	1	A	A'	NOT
B	B'	A	A'B+AB'	XOR
B'	B	A	A'B'+AB	XNOR

Fig: Truth table of MGDI Cell

The logical level for different input combination will be,

For A ='0' and B = '0'
pMOS in linear : Vin-Vtp<Vout<Vdd
nMOS in cutoff: Vin<Vtn

For A ='1' and B ='0'
pMOS in cutoff: Vin>Vdd+Vtp
nMOS in linear: 0<Vout<Vin-Vtn

For A ='0' and B ='1'
pMOS in linear: Vin-Vtp<Vout<Vdd
nMOS in cutoff: Vin<Vtn

For A ='1' and B ='1'
pMOS in linear: Vin-Vtp<Vout<Vdd
nMOS in linear: 0<Vout<Vin-Vtn

The section of MGDI, GDI, and CMOS logic are evaluated and its comparison are done with switching delay, transistor count and average power consumed by MGDI, GDI and CMOS logic cells. By having this analysis it is observed that MGDI performance is good when compared to both CMOS

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and GDI function. In CMOS the transistor count is used to realize a function twice that of MGDI. The design of xor and xnor utilized only three transistors in MGDI whereas in CMOS logic it is eight. Hence consumption of power is slightly higher than MGDI.

E. Design of Modified GDI full adder

Full adder exhibits as a combinational circuits which performs arithmetic sum of three bits: A, B and C that produces corresponding SUM and COUT from previous addition.

The equations for SUM and CARRY are given below,

SUM = (A xor B xor Cin) ----------(1)

CARRY = A.B + B.C + A.C ----------(2)

SUM = $\overline{C}$ (A xor B) + C ($\overline{\text{A xor B}}$) -----(3)

COUT = A.B + Cin (A xor B) ----------(4)

COUT = B (A xor B) + (A xor B) C----(5)

The 8T MGDI full adder is used to implemented the ripple carry adder based, were it uses MGDI full adder with 8 transistor from equation (1) and (5) has been realized using 3-input xor and SUM expression and 2-to-1 MUX is used for carry expression as shown in figure.

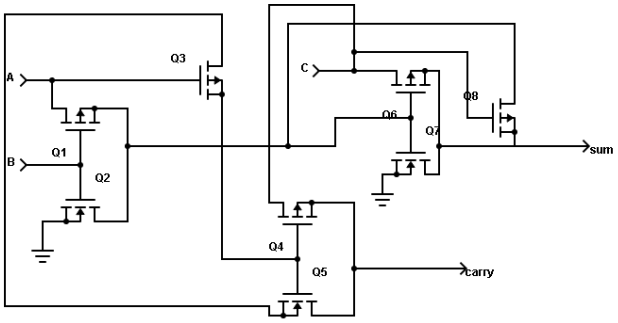

Fig: 8T MGDI cell adder

F. Implementation of RCA

A 8-Bit ripple carry adder is designed using 1-bit full adder cell. The RCA is having 8-bit input of A[i] and B[i] where i vary from {0….7} and the SUM output as SUM[k] where k = {0….7}.

SUM[k] = A[i] + B[i]

In the methodology of proposed design a 8-bit ripple carry adder will be constructed using MGDI technique. The ripple carry adder can be explained as a chain circuit where the carry output of one full adder will be the carry input of the successive adder cell circuit. The input carry ripples through every input to output. Hence the implementation of RCA has 8 adder cells. Full adder exhibits addition that are having multi

bits in each of its operand. It can be as,

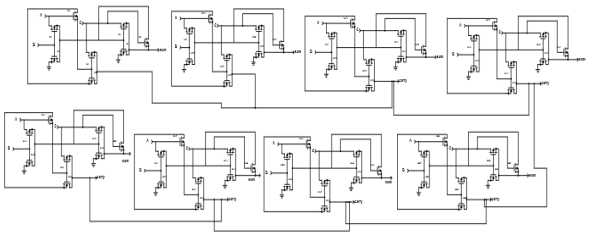

Fig. 8-bit Ripple carry adder

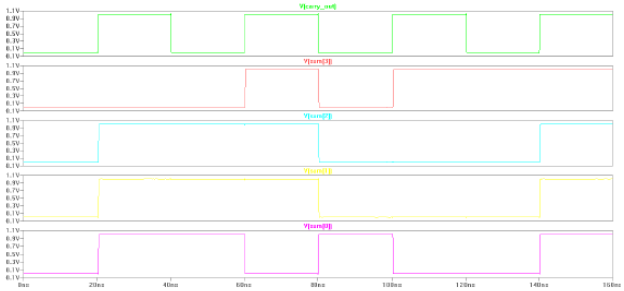

Fig: Output of 8-bit RCA

G. Simulations and Designs

The different full adders proposed are based on CMOS, GDI and MGDI technique simulated with 100MHz frequency and 27 degree Celsius and the supply voltages varies from 0.5V to 1.5V in 180nm CMOS technology and keep the threshold voltage of the transistor as 0.34V. The inputs to the full adder are A, B, and CIN, the test vectors are generated and fed into the corresponding adder cells.

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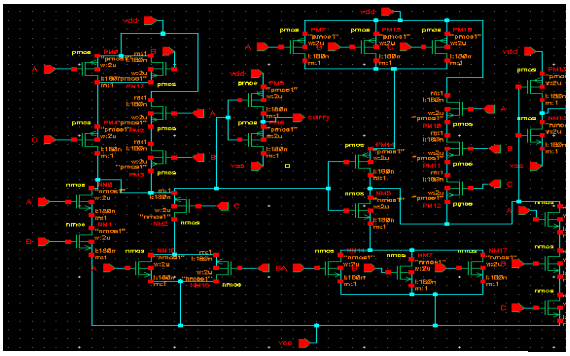

Fig. Schematic of 28T

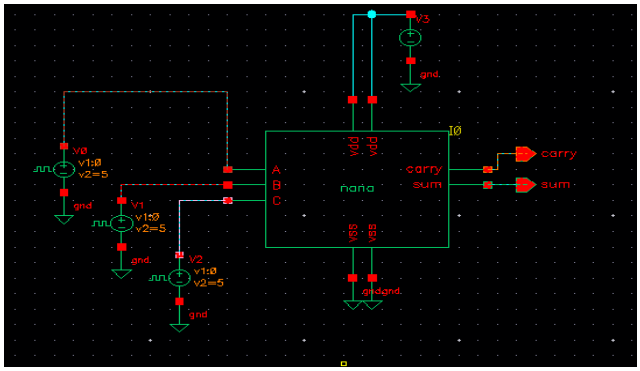

Fig. Symbol of 14T

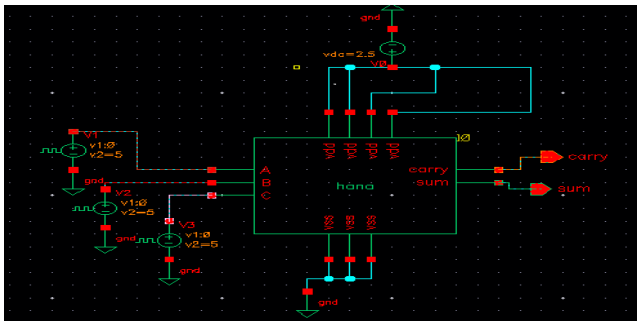

Fig. Symbol generation of 28T

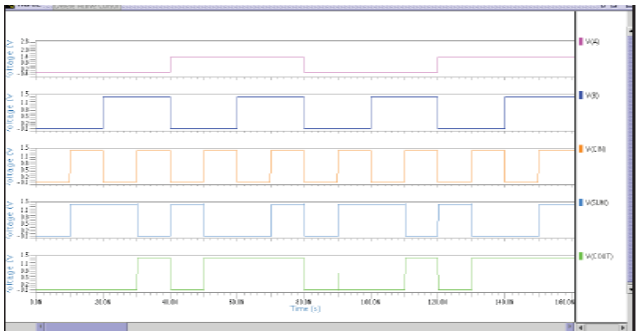

Fig. output of 14T

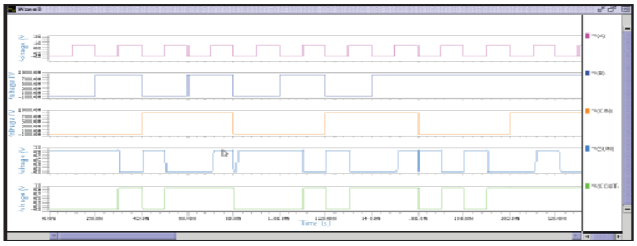

Fig. output of 28T

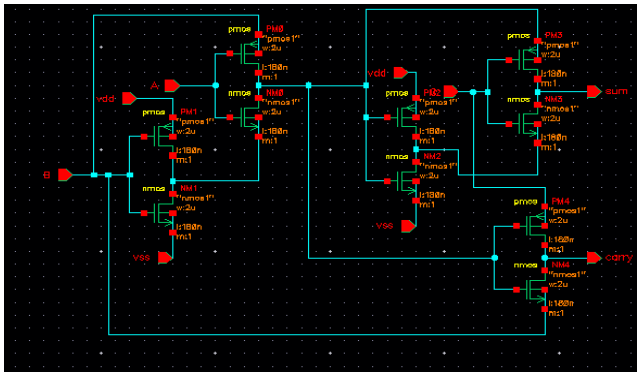

Fig. Schematic of 10T

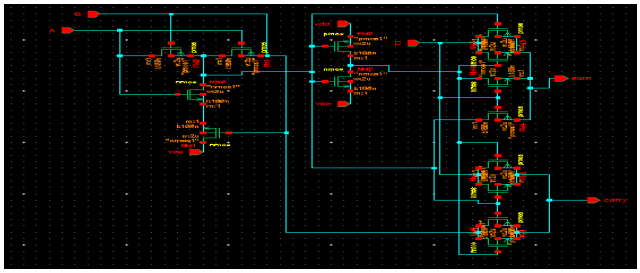

Fig. Schematic of 14T

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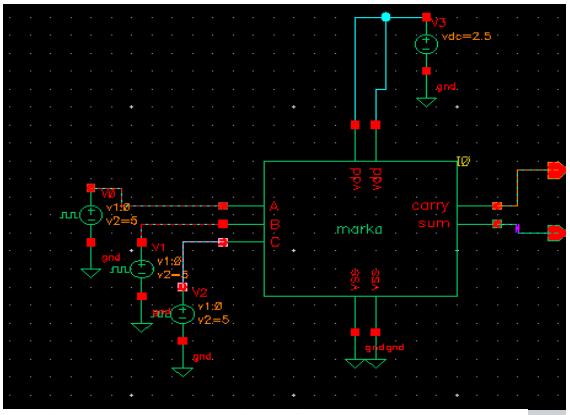

Fig. Symbol generation of 10T

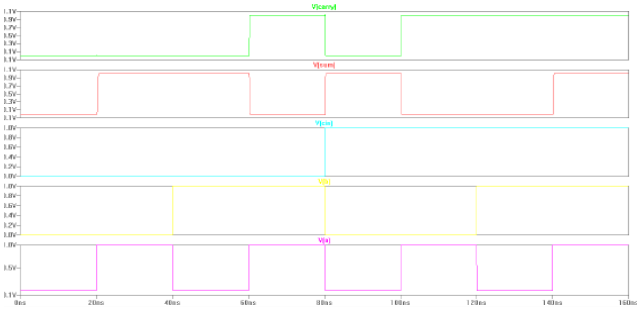

Fig. output of 8T

H. Results

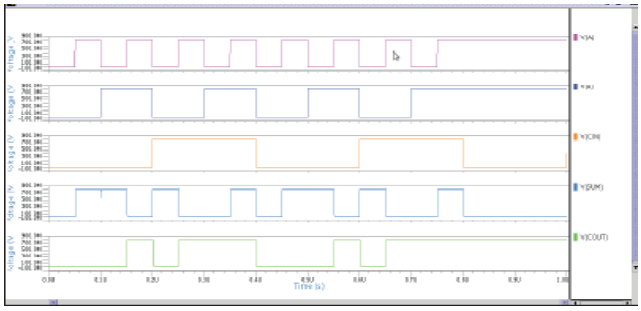

Fig. output of 10T

CIRCUITS	Leakage Power (nw)	Dynamic Power (nw)	Area (No of Transistors)	Delay
28T Full adder	13.4261	9157.10	28	11.73E-10
14T Full adder	9.84764	7311.54	14	9.981E-11
10T Full adder	5.38142	6761.33	10	7.862E-11
8T Full adder	3.54751	3999.14	8	6.176E-11
RCA	31.9324	27566.96	64	79.33E-10

Fig. Comparison of full adders and RCA

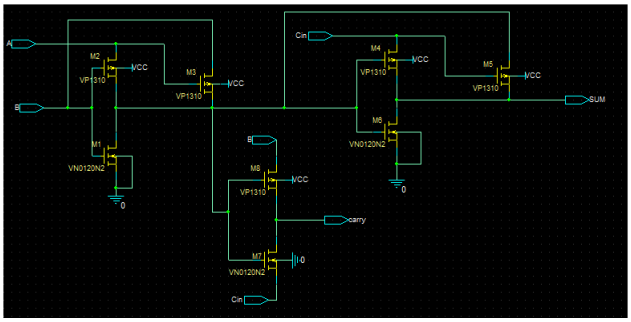

Fig. Schematic of 8T

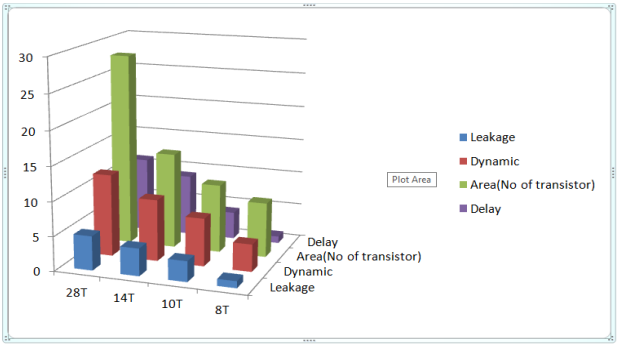

Fig. Graph of various full adders

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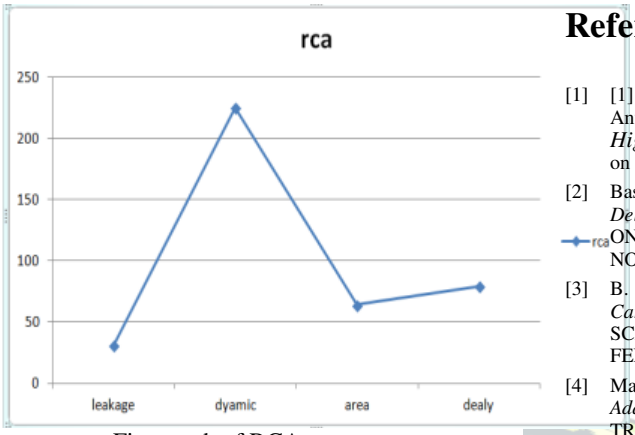

Fig. graph of RCA

I. Conclusion

The above circuits are designed in Cadence virtuoso and Cadence Orcad using 180nm GPDK technology, having voltage supply of 1.5V and Voltage of 0.9v and then compared with each other and tabulated as shown in the above figure.

The Future works that are to be done as follows. We can improve the works or performance of every designed 1-bit full adder blocks by varying their W/L ratios or by summing some of the passive elements like resistors, capacitors, etc. Using the designed 1-bit full adder blocks, we can design the from lower bit to higher bit (for example 64 bit extension). We can now design and compare the cells in all possible technologies from 180nm to 22nm and so on. We can replace the blocks of full adder of any application projects, with our designed full adder circuit blocks, which can perform the similar function as that is done by previous full adder, to enhance the performance factors like Area, Delay, or Power consumption, etc.

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