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Design and Analysis of Time-to-Digital Converter Based on Vernier Delay Line

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***Abstract*—This paper presents a low nonlinearity, missing code free, time-to-digital converter (TDC) with direct bin-width calibration. The vernier delay lines (VDLs) and a modified direct-histogram architecture are combined to correct the nonlinearity originated from carry chain, ad use a multiphase sampling structure to minimize the skews of clock routes. Also vernier delay lines are compared by tuned tapped delay lines (TDLs). Results of code density test shows that VDL has much better linearity performance and time resolution than TDL. Based on the direct-histogram architecture, a direct bin-width calibration method was implemented. For a single VDL, the differential nonlinearity (DNL) is within [-0.59,0.45]LSB with σDNL=0.07 LSB and the integral nonlinearity (INL) is within [-0.59,0.026] with σINL =0.59 LSB. The dead time for VDL is reduced as half of one clock cycle.. Thermal and power variations are also calculated for both vernier delay lines and tuned tapped delay lines.**

***Index Terms*— Carry chains, vernier delay line (VDL), tuned tapped delay line, code bin width, time-of-flight, time-to-digital converters (TDCs).**

I. INTRODUCTION

TIME-TO-DIGITAL converters (TDCs) are required in many time resolved applications due to their excellent performances in timing resolution: they have been widely applied in space sciences, medical diagnosis and imaging, nuclear physics, quantum communications and time-of-flight detections. TDCs are actually high-precision (several picoseconds) stop- watches that are capable of time-tagging fast events and generating corresponding digital codes. For example, TDCs in time-correlated single photon counting instruments generate picoseconds timestamps for photon events in fluorescence lifetime imaging microscopy (FLIM), fluorescence spectroscopy, or time-resolved luminescence experiments for characterizing solid-state materials.

With rapid advances in CMOS and digital technologies, TDCs can be implemented in application-specific integrated circuits (ASIC) or field programmable gate arrays (FPGA) to achieve a sub nanosecond resolution. Compared with the FPGA-based TDCs, ASIC-based solutions usually have better

precision and linearity. However, they are more expensive and time consuming, usually more suitable for large-scale commercial products. On the other hand, FPGA TDCs provide greater flexibility with a shorter developing cycle for prototyping and verifications. FPGAs are reprogrammable, easy to access (low cost), and promising for product developments. Furthermore, recent advances in FPGAs have allowed tapped delay line (TDL) TDCs to achieve a resolution less than 20 ps.

The simplest digital TDCs can be implemented by clock driven counters, but the time resolution of this type of TDCs is limited by the clock frequency. To achieve a better resolution, vernier delay line (VDL) and TDL methods have been widely used. Further-more, coarse and fine code methods and interpolation methods have been proposed to achieve a larger measurement range with higher precision. Besides, the cyclic pulse shrinking and dynamic re- configuration methods were proposed to explore the different FPGA–TDC architectures.

The measure of time interval between two events and represent that interval in the form of digital number is TDC. They are used in places where the time interval between two events needs to be determined. These two events may, for eg, be

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represented by rising edges of two signals. The delay line based TDC is a very primitive one and involves a delay line which is used to delay the reference signal. The other signal is used to sample the state of delay chain. Each stage of delay chain output to a flip-flop or a latch which is clocked by the sample signal. Thus the output of TDC forms a thermometer code as the stage will show a '1' if the reference signal has passed it, otherwise it will show a zero.

II. DESIGN AND ARCHITECTURE

There are different ways of building a TDC in that the major architectures are based on delay lines. In this project vernier delay lines are proposed and also compared with tuned tapped delay lines. Great care must be taken in the design phase, which includes trade-offs in resource utilization, stability and calibration difficulty amongst other concerns.

The architecture of the TDC is shown in Fig. 1. The 'start' port of a VDL is buffered by a hit signal driven

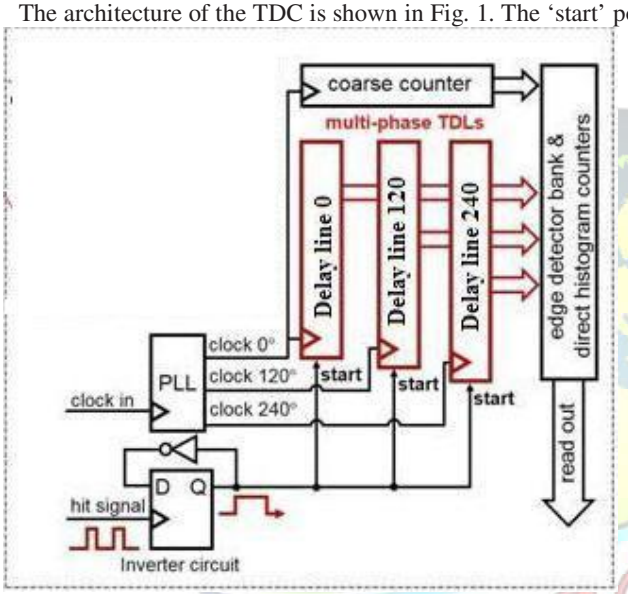

Fig. 1 Block diagram of TDC

inverter. The TDL is based on cascaded carry chain modules with modified outputs. The states along the TDL are registered by D-flip flops as thermometer codes (1 111 000... or 0 000 111.. .), to be converted to one- hot codes (0 001 000.. .) by the XOR-based edge detector to indicate the position of the transitions. We applied the direct- histogram architecture. But in order to apply the bin width calibration, each bit of the one-hot code drives a synchronous counter instead of a ripple counter used in Dutton's original design. The diagram that each synchronous counter has multiple count registers (according to the coarse code) to extend the measurement range. By this arrangement, these counters can be further employed for novel bin-width calibrations to be detailed in Section III. In order to cover the sampling clock period and reduce the length of the VDL simultaneously. The multiphase sampling architecture are proposed. This design is suitable for both VDL and TTDL, only the delay lines are replaced. [5] proposed a novel method for secure transportation of railway systems has been proposed in this project. In existing methods, most of the methods are manual resulting in a lot of human errors. This project proposes a system which can be controlled automatically without any outside help. This project has a model concerning two train sections and a gate section. The railway sections are used to show the movement of trains and a gate section is used to show the happenings in the railway crossings. The scope of this project is to monitor the train sections to prevent collisions between two trains or between humans and trains and to avoid accidents in the railway crossings. Also an additional approach towards effective power utilization has been discussed. Five topics are discussed in this project : 1) Detection of obstacles in front of the train;2) Detection of cracks and movements in the tracks;3) Detection of human presence inside the train and controlling the electrical devices accordingly 4) Updating the location of train and sharing it with other trains automatically 5) Controlling the gate section during railway crossing. This project can be used to avoid accidents in the railway tracks.

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A. Tuned tapped delay line

The tuned tapped delay lines are the existing method can be used to interface CMOS single-photon avalanche diodes (SPAD) for ranging, FLIM or positron emission tomography applications. The output signals of CMOS SPADs are compatible with the TTDL with very simple frontend circuitry converting the SPAD can range from several to tens of nanoseconds. Benefiting from a short dead time when compared with raw TDL. TDC can serve multichannel SPADs for high-speed time-resolved spectroscopy applications. The design of tuned-TDL is shown in Fig. 2. It consists of D-flip flops and delay inverters. In tuned-TDL, the delay inverter starts before the first flip flop. Only input D consists of delay and there is no delay for clock input. It is superior with respect to conversion rate, resourse usage and ease of encoding.

The delay in TTDL is N where N is the number of flip flop used. The dead time i.e. time difference between hit arrival time and rise time of clk will leads to one clock cycle. This type of TDL consists of frequency ranges from 160MHZ to 470MHZ. The tuned tapped delay line consisit of series of flipflops and inverter.

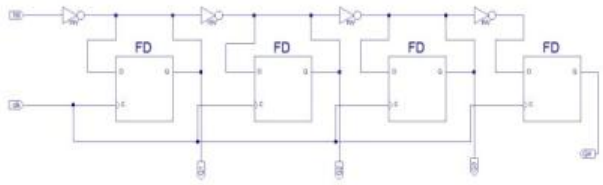

Fig.2 Block diagram of Tuned tapped delay line

B. Vernier Delay Line

The time to digital converters are also designed by Vernier delay lines. So in this paper vernier delay lines are proposed because it shows better performance than tuned tapped delay lines. The same CMOS SPAD output signals are compatible with VDL. There is even shortest dead time when compared with TTDL. It is based on cascaded d flip flop with delays for both d input and clk shown in Fig 3.

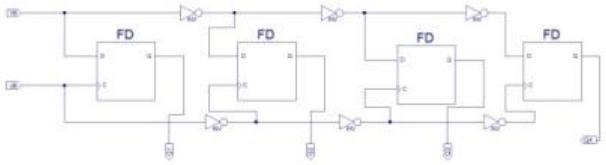

Fig.3 Block diagram of Vernier delay line

The delay in VDL is (N-1) where N is the number of flip-flops used. The frequency ranges are varied from 80 to 500 MHZ. The dead time for this type of delay lines are half of one clock cycle. By comparing VDL with TTDL, Vernier Delay Line has better time resolution with tuned tapped delay line.

C. Missing Codes and Modified Direct-Histogram Architecture

Due to the nonuniformity of carry chains in a Delay lines, “bubbles” (1110100... or 00010111...) are generated in ther-mometer codes after sampling. Traditional TDL-TDCs convert one-hot codes to binary codes, and bubbles must be removed by bubble-proof circuits. However, after the bubble removal, missing codes appear as the taps are not able to detect enough hit events. Some research groups proposed the bin realignment and delay lines are reduce to missing codes, but they are not able to remove missing codes completely.

The direct-histogram architecture is used in this paper which does not convert thermometer codes to binary codes, and the bubbles are counted into the histogram on purpose to remove the missing codes. When bubbles appear in ther- mometer codes, multihot codes (0011100) are generated by the XOR edge detector, and the missing codes are compensated and filled up by the multihot codes. Dutton’s direct- histogram design does not have missing codes, however, its linearity performances are not satisfactory. The proposed delay line combines the direct-histogram with the delay lines, not only removing the missing codes completely, but also greatly enhancing the linearity. Although bubbles introduce errors, they are static and can be corrected easily by bin-width calibrations according to our study.

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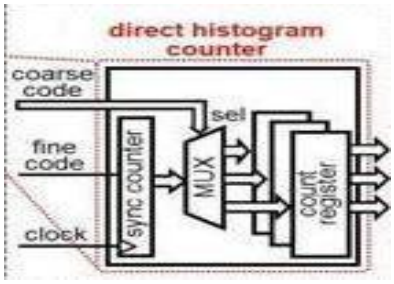

Fig 4. Architecture of direct histogram

The architecture of direct histogram is shown in Fig 4. Our study shows that missing codes have more dominating effects on the linearity performances of a TDC. In addition, benefiting from the direct-histogram architecture, multiple events can be recorded simultaneously by the same TDL, and the dead time is reduced. In time domain imaging a temporal histogram is conventionally created by incrementing a memory location determined by the TDC output code. The synchronous counter is directly connected to each XOR output. Each counter then forms one bin of the temporal histogram. Programmable protection logic is implemented to avoid counter overflow.

D. Clock Distribution

The direction of the TDL is vertical, and a large skew exists between two delay cells that are located at the boundary of two a TDL) should be able to cover at least one period of the sampling clock, LSB × N ≥ τ (where LSB is the average code bin width and τ is the period of the sampling clock), otherwise the TDC cannot capture events completely. The maximum clock frequency (of different speed grades) is from 80MHZ to 600 MHz Devices operating at higher clock frequencies are more prone to timing errors. On the other hand, TDLs have larger nonlinearity when they cross the boundaries of CRs. To avoid crossing CR boundaries, the length and the location of a TDL should be controlled properly. It is hard to achieve a short TDL and use a high-clock frequency simultaneously, if a single TDL is used. Won *et al.* proposed a dual-phase method which to reduce the length of the TDL and to allow the TDCs operating at a lower clock frequency. The dual-phase method used two parallel TDLs sampled by two clocks with 0° and 180° phases, respectively. The number of phases does not influence the linearity of the TDC directly.

A large number of phases reduce the clock frequency, but it also increases the system complexity. There is a trade-off, and the number of phases is selected according to the devices or system specifications. After performing full-length TDL tests (it confirms that using dual-phase sampling causes more timing errors), we used the multiphase architecture with three sampling phases. Three parallel TDLs are sampled by three clock signals with 0°, 120°, 240° phase shifts, respectively, and each TDL covers one-third of the clock period. The timing diagrams of the triple-phase architecture are shown in Fig. 5 and 6.

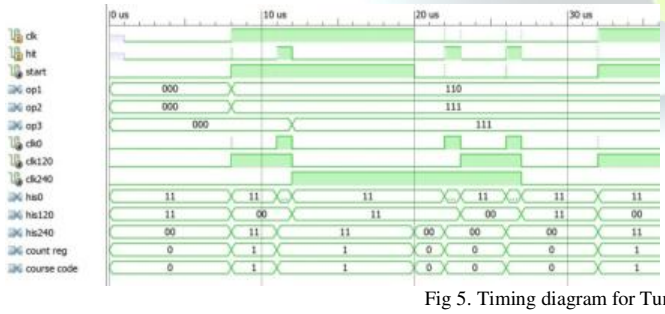

Fig 5. Timing diagram for Tuned Tapped Delay lines

The same clock frequency and same hit signals are used in the both delay lines. The outputs of these are also nearly same. The direct histogram architecture is applied for both delay line TDCs.

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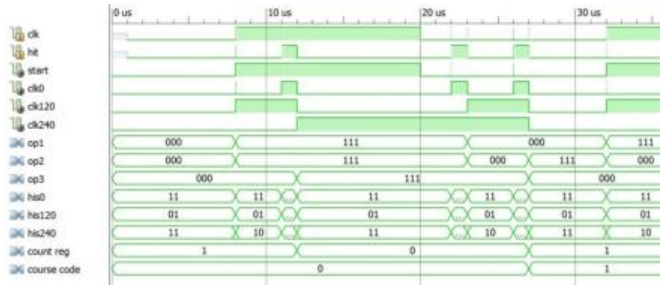

Fig 6. Timing diagram for Vernier Delay lines

III. PERFORMANCE ANALYSIS

To evaluate the proposed TDC, code density tests were performed. A tuned-TDL and vernier delay line were tested with the modified direct-histogram architectures, respectively (four combinations). The bin-width calibration method was tested and discussed as well. Two independent low jitter crystal oscillators (DSC1103) were used.

A. Bin-width calibration

The bin-by-bin calibration method was widely used to enhance the linearity of TDCs. This method can be summarized as, where the calibrated time of Bin n, t_n, can be derived as

$$t[n] = \frac{W[n]}{2} + \sum_{k=0}^{n-1} W[k] \qquad (1)$$

Where W[n], W[k] are the code bin width of the code bins n and k. The effect of applying (1) is equivalent to discarding all missing codes. However, removing missing codes also reduces the number of effective bins. The another simple calibration approach can be easily derived from the definition of the DNL. Different from the original design for the post calibration, we propose a new strategy to allow on-line calibration in this paper.

B. Differential Nonlinearity and Integral Nonlinearity

The length of TDL was tested with a full length of 2000 bins. The code density test, we measured the individual bin widths ω and T_{LSB} . The DNL was calculated as follows:

$$DNL_i = \frac{\omega_i - T_{LSB}}{T_{LSB}}$$

To characterize the INL, we used the end-point INL, which was calculated as follows:

$$INL_I = \sum_{k=0}^{i} DNL_k$$

This equation can be applied to both tuned and vernier delay lines. The bins at 200, 400, 600, 800, 1200, 1400, 1600, and 1800 are taken for the calculation. The clock frequency for Tuned TDL is between 150 and 470 MHZ. Similarly the clock frequency for VDL is between 80 and 400 MHZ. The DNL for TTDL is ranges from [-0.38, 0.87] and also for VDL is ranges from [-0.59, 0.45].

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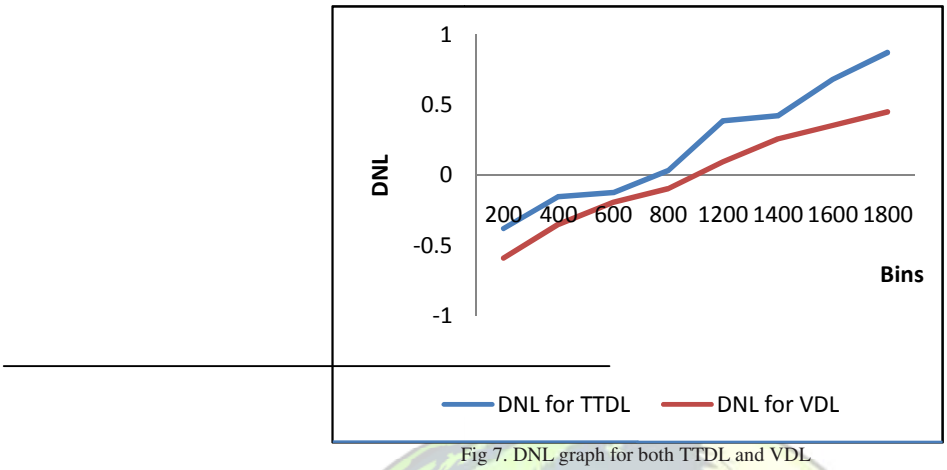

Fig 7. DNL graph for both TTDL and VDL

The INL for TTDL is ranges from [-1.23, 1.02] and also for VDL is ranges from [-1.22, 0.026]. The T_{LSB} for above bin widths are 3.1ns. The positive and negative DNL appear alternatively because of the unbalanced propagation delay primitive. This TDC architecture allows us to implement the VDL with minimizing the clock skew problem, and thus there was no high positive DNL or no continuous negative DNL. The fig 7 and shows the graph for DNL and INL variations for TTDL and VDL. Also Table 1 shows the variations of DNL, INL, σ_{DNL} and σ_{INL} for raw-TDL, tuned-TDL and VDL.

IV. CONCLUSION

We integrate, for the first time, the vernier delay line, the modified direct-histogram based on the multiphase architecture to implement a low nonlinearity, missing-code free TDC with the fast bin-width calibration. The unique advantages are that the synergistic effects brought by this combination are Significant in suppressing the nonuniformity according to the tested DNL and INL, measurement deviations, the equivalent bin widths and their standard deviations. Moreover, the missing codes are completely removed. The multiphase method provides extra design flexibility to minimize the nonlinearity from clock route skews and to lower the timing requirements for the clock frequency simultaneously. Based on the direct-histogram architecture and the missing-code-free feature, a novel bin-width calibration method can be applied, and the performance was presented and evaluated. The σDNL and σINL are reduced to 0.07 and 0.5. Thus the direct- histogram architecture can be widely applied in vernier delay line to achieve low nonlinearity, missing-code free with direct bin-width calibrations providing distinguished advantages over tuned tapped delay line.

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