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# REDUCTION OF COUPLING SIGNALS USING LATCH TYPE SENSE AMPLIFIER IN SRAM

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***Abstract*—with the developement of modern semiconductor fabrication technology, the channel length of the CMOS device and the device pitch continually shrink accompanied by more and more severe process variation and signal coupling effect respectively. The coupling effect of the sense amplifier with a memory element circuit reduced by using a different type of sense amplifier. In this paper, we explain the reduction of coupling effect in the circuit by classifying and suppressing different turn ON currents. This new type of sense amplifier circuit achieves obvious improvement and leads to better results for memory elements in our monte-carlo simulation. The power can be consumed over latch type sense amplifier.**

***Keywords—monte-carlo,sense amplifier,SRAM,coupling***

## I. INTRODUCTION

Sense amplifiers are one of the most critical circuits in the periphery of CMOS memories. This performance strongly affects both memory access time and overall memory power dissipation. Sense amplifier is a basic part of SRAM and is widely used in SRAM products which is the critical memory block for the SOC. In SRAM, sense amplifier is normally used for sensing small differential voltage generated from bit-cell [1].Sense amplifiers are used extensively in memories read operation to amplify the small signal bit-line voltage differential to digit level [3].Random variations causes yield loss due to several mechanisms such as read stability, write ability, retention and read sense margin, this mechanism that typically limits SRAM speed [2],[4].The latch type voltage sense amplifiers are favourable because of their simple structure and low power consumption. The memory chip will occupy 90% of chip area, Therefore the power dissipated within the on-chip latches will become a dominant part of the total power consumption of the chip [7]. The sense amplifier has the ability to quickly amplify a small differential signal from the bit-lines(BL) and data-lines to full CMOS logic level outputs without requiring large voltage swings [7],[8].

In this paper, as we can see, the coupling of signals to the sense amplifier circuit. In fig1 shows the traditional SA. MP1, MP2 are transfer gates of the bit-line differential voltage.

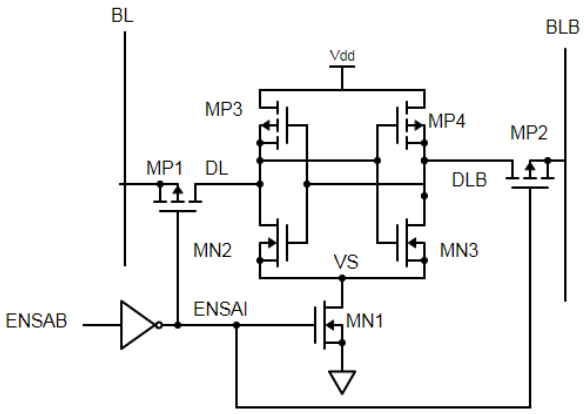


Fig 1: Traditional sense amplifier

The behavior of the SA as follows,

1. ENSAB goes low when enough differential voltage is generated from SRAM cell between DL and DLB.
2. MP1 and MP2 shut down.
3. MN1 turns on and sinks current, which make MN2 and MN3 turn on.
4. MN2 and MN3 both sink current and make MP3 and MP4 turn on. When PMOS current exceeds the NMOS current one node is pulled back while the other node falls to zero.

The rest of this brief is organized as follows, In section II the sensing dead zones of various latch type SA's are analyzed. In section III, the suitable proposed SA is compared with traditional SA and power consumption is analyzed. The performance criteria and results are analyzed in monte-carlo simulation in section IV.

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## II. SENSING DEAD ZONES OF LATCH TYPE SA'S

### A. *Simulation methodology and variability:*

T-SPICE is a complete circuit design and system analysis system that include; schematic editor S-EDIT, T-SPICE, circuit simulator, advanced model package, W-EDIT waveform viewer. The design cycle for the development of electronic circuits includes an important prefabricated verification phase. Because of the expense and time pressure associated with the fabrication step, accurate verification is crucial to an efficient design process. The roleof the T-SPICE is to help design and verify the circuit operation by numerically solving the differential equations describing the circuit.

Simulations were performed using a predictive model of a 65nm CMOS technology with a VDD of 1.1V. $V_{BL}$ is assumed to be larger than $V_{BLB}$ by $\Delta V_{BL}$. The SA input voltage is defined as $V_{BL}$ in this brief. Monte-carlo (MC) simulations were performed to analyzed the sensing dead zones of an SA. There are many sources of random and systematic variability that can induce transistor mismatch. As the process technology is scaled down, the effects of random variation increase. In particular, threshold voltage($V_{TH}$) variation which is induced by random dopant fluctuation(RMF) and is assumed to follow a Gaussian distribution becomes a dominant factor. Therefore $V_{TH}$ variation is the main contributor to $V_{OS}$. According to pelgrom's research the standard deviation of $V_{TH}$ variation($\sigma VT$) is expressed as,

$$\sigma_{VT} = \frac{A_{VT}}{\sqrt{W \times L}}$$

$$A_{VT} = \frac{\sqrt[4]{4q^3 \varepsilon_{Si} \Phi_F N}}{2} \cdot \frac{T_{OX}}{\varepsilon_{OX}}$$

Where AVT is a constant that depends on the process technology used. ΦF is the Fermi potential, Tox is the thickness of the gate oxide, N is the doping concentration of the substrate and ξsi and ξox are the permittiviy of silicon and gate oxide respectively. The transistor variability used in the monte carlo simulations was modeled as a $V_{TH}$ variation that follows a Gaussian distribution. However, RDF induced $V_{TH}$ variation comprises ˜60% of the total $V_{TH}$ variation in deep sub-micron technology because there are other variability sources such as line edge roughness, Tox, variation and interface roughness. When designing an SA yield is the most important design criterion. Because the industry design target of 3 σos is typically set to be 50-70 mv, the SA's in this brief are designed to have a σos of 20 mv. The simulation methodology for performing sening dead zone analysis as follows, wit a fixed value of $V_{BL}$ The correct sensing operation occurs when $\Delta V_{BL}$ is larger than Vos. Then $Y_{sa}$ can be estimated as

$$Y_{SA} = \frac{\text{number of correct sensing operations}}{\text{total MC simulation trials}}.$$

Because the SAs are designed to have a σos of 20 mv, sweeping $\Delta V_{BL}$ from -70 to 70 mv is sufficient to extract μos is close to 0 and thus can be ignored. The same procedures are performed while sweeping $V_{BL}$ from 0 Vto VDD. The Ysa is significantly reduced when the $V_{BL}$ is in the sensing dead zone. The degradation of Ysa can be modeled as an increase in σos.

## III. PROPOSED WORK

### A. *Coupling suppression in Latch type Sense amplifier:*

The bit line signal difference affects on the gate voltage of transistors MN1 and MN2. The drains of transistors MP1,MN5,MP2 and MN4 are output nodes.

There is no current flow from bit lines to output nodes. When sensing signal SE is at logic 0 (GND), the output node is isolated to GND and the precharge transistors are MP3 and MP4 charge output nodes to VDD. Because the output nodes out and outb are precharged to VDD. The transistors MP1 and MP2 are at cut off region and MN4 and MN5 are at saturation region. When the sensing signal SE changes to logic 1 (VDD). MN3 turned on and the node is pulled down to GND level. Under this condition, MN1 and MN2 are working as a common source differential amplifier.

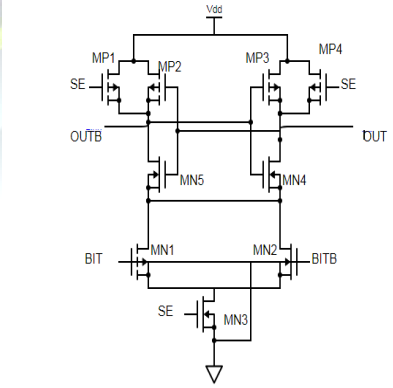


Fig 2: Schematic diagram of Latch type sense amplifier

The voltage difference between BIT and BITB is transferred to the output nodes out and outb by the common source differential amplifier After a small voltage difference between out and outb is generated the cross

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coupled amplifier which is constructed byMN4,MN5,MP1 and MP2 will finally amplify tha voltage difference between out and outb to a full swing voltage level.

Therefore, we can sense and amplify the bit line signal without any current drifting from bit line to output node. This result shows that the bit line voltages will not be amplified, so the sensing and precharging power dissipation will be reduces. Thus, the coupling signals of an circuit is suppressed.

## IV. IMPLEMENTATION

### A. *Implementation of sense amplifier in SRAM:*

Static Random Access Memory, or SRAM, is a type of volatile memory with a non-destructive read cycle. Figure 2.3 shows an example of an SRAM cell in standard 6T configuration. The SRAM cell contains two access transistors (NAX1, NAX2), and two cross coupled inverters (N1, P1 and N2, P2) comprised of a PMOS load transistor, and an NMOS driver transistor. The cross coupled inverters constantly reinforce which value is stored on each side of the cell. Node Q holds the cells value and node Q holds its complement.

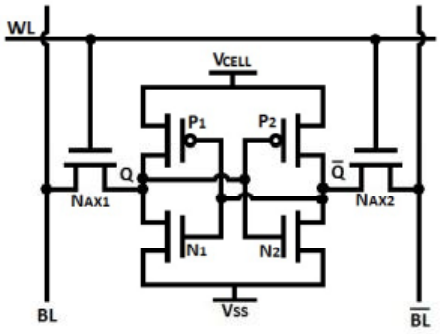


Fig 3 : SRAM cell

The cell is powered by the voltage applied at VCELL. As long as power is supplied to VCELL, the SRAM cell can hold its value inde_nitely. The wordline (WL) selects the cell and allows values to be read from or written to the cell. When the wordline is not selected, the cell is in standby mode. Selecting an address brings a wordline to a logic high, selecting all of the cells in that word. This brings the cells out of standby by enabling the access transistors, which allows the cells to be read from or written to. The cell also has two bitlines which control both the input and output of the data from the cell. The bitline (BL), known as bitline, holds the same value that is stored in the cell. The second bitline BL, known as bitline bar, or bitline, or bitline not, holds the inverse of the value that is stored in the cell.

The SRAM write circuitry connects directly to the bitlines and is used to write a value to the SRAM cell. The value stored in the SRAM cell is stored at node Q, while the inverse of the value is stored at node Q. The cell can be seen above in Figure 3.Instead of writing either a logic 1 or a logic 0 to side Q, a 0 is written to either Q or Q depending on which value should be stored in the cell. To write a value to the cell, one bitline is held at VDD while the other is held at VSS. Holding the bitline at VSS will cause the inverter to be pulled past its trip point, which will cause the cell to latch and hold the new value [6].

The precharge circuitry brings the bitline and bitline to be the same voltage before a read cycle. The simplest version of precharge circuitry consists of three transistors that can be either NMOS or PMOS devices. Two of the transistors are used to connect the bitlines to VCC, and the third transistor is connected between the two bitlines to ensure that the lines end up being the same voltage.

The memory circuit is said to be static if the stored data can be retained indefinitely, as long as the power supply is on, without any need for periodic refresh operation. The data storage cell, i.e., the one-bit memory cell in the static RAM arrays, invariably consists of a simple latch circuit with two stable operating points. Depending on the preserved state of the two inverter latch circuit, the data being held in the memory cell will be interpreted either as logic '0' or as logic '1'. To access the data contained in the memory cell via a bit line, we need atleast one switch, which is controlled by the corresponding word line

Embedded Static random access memory (SRAM) has become increasingly prevalent in modern system on chip(SoC) designs to support multiple processors running numerous software applications. This demand is driven by a new generation of medical devices, wearable electronics, Hand held devices, communication systems, all driven by the Internet of Things (IoT). Even though SRAM have many attractive features, low power consumption with high speed and variation induced failures are the most difficult challenges faced by the designers. Lowering supply voltage down to sub threshold region is an effective method for SRAM power reduction and widely adopted in practical applications. SRAM power consumption is often limited by sense amplifier (SA) offset voltage (*VOS*). Therefore, Sense Amplifier is a vital component of the SRAM. Resolution time, power/energy consumption, die area, and resolution are the decisive metrics of the SA. The SA resolution for correct sensing is determined by the SA offset voltage. For high resolutions, it is important to minimize the SA's input-referred offset voltage, which is largely determined by the threshold mismatches of the sensing and cross coupled transistors. Therefore, higher the higher the offset, higher is the power. This brings us to the typical trade-off between memory yield and power delay product. SA's *VOS*, mainly arises from mismatches in the gain factor, the drain current, the threshold voltage (*VTH*), and the layout of

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the devices used in the SA. Among these contributors, *VTH* mismatch has been identified as the dominant contributing factor to large *VOS*. Due to this offset, SRAMs suffer from slow read speed or high read failure probability. Thus, developing an SA with greater offset tolerance is a prerequisite to achieving high-yield. Various approaches like data line isolated differential CSA increasing device size, slower transition of sense enable (SEN) signal, post silicon tuning using digitally controlled offset compensation, *VOS* compensation by storing the *VTH* of the sensing transistors current-sampling-based SA (CSB-SA) to suppress the offset and offset cancellation scheme through equalizing the *gm* of the devices, have been proposed to mitigate the above issues associated with SA offset.

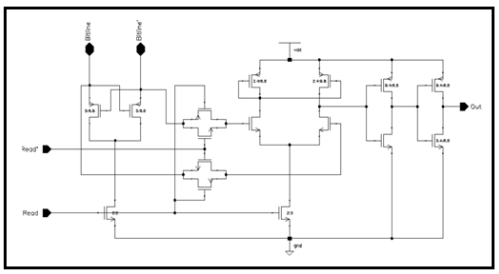

Fig 4 SRAM with Sense amplifier

The solution added a Schmitt Trigger (ST) to the pull down network in SA. The STn-SA achieves higher level of tolerance to *VTH* variation by increasing switching threshold of the inverter. This was also achieved by weakening the pull down network using stacked NMOS devices called stacked SA (STk-SA). Unfortunately, the attempt to reduce the input offset voltage of SA often leads to increase in SA area and power consumption or prolonged resolution time. Hence, the trade-off between SA input offset voltage, area and power-delay is a major design challenge, especially for nano scale CMOS technology. [5] proposed a novel method for secure transportation of railway systems has been proposed in this project. In existing methods, most of the methods are manual resulting in a lot of human errors. This project proposes a system which can be controlled automatically without any outside help. This project has a model concerning two train sections and a gate section. The railway sections are used to show the movement of trains and a gate section is used to show the happenings in the railway crossings. The scope of this project is to monitor the train sections to prevent collisions between two trains or between humans and trains and to avoid accidents in the railway crossings. Also an additional approach towards effective power utilization has been discussed. Five topics are discussed in this project : 1) Detection of obstacles in front of the train;2) Detection of cracks and movements in the tracks;3) Detection of human presence inside the train and controlling the electrical devices accordingly 4) Updating the location of train and sharing it with other trains automatically 5) Controlling the gate section during railway crossing. This project can be used to avoid accidents in the railway tracks.

### *B. Implementation of sense amplifier in flip flop:*

In general, flip flop consists of two stages, a pulse generator (PG) and a slave latch (SL). The sense amplifier flip flop (SAFF) consists of SA in the first stage and slave reset latch in the second stage. Sense amplifier based flip flop is a flip flop where the SA provides a negative pulse on one of the inputs to the slave latch, depending whether the output is to be set or reset. It senses the true and complementary differential inputs. The SA stage produces monotonic transitions from one to zero logic level on one of the outputs, following the leading clock edge. Any subsequent change of the data during the active clock interval will not affect the output of SA. After the clock returns to inactive state, both outputs of the SA stage assume logic one value. Therefore whole structure act as a flip flop.

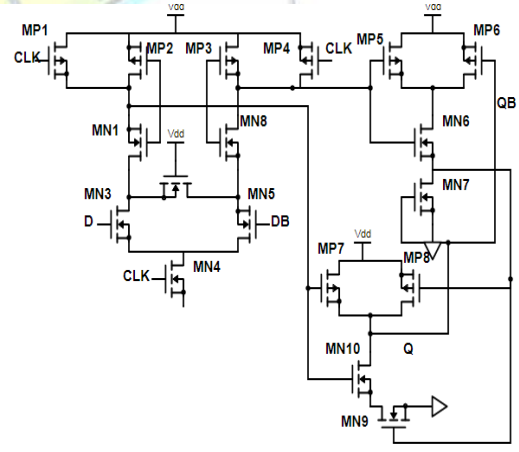


Fig 5: Implementation of sense amplifier in flip flop circuit

## V. RESULTS AND ANALYSIS

In the design of latch type sense amplifier, we try to make every coupling happen when the turn on MOS drive the nodes of DL and DLB. By thie design, the effects of coupling are suppressed. A smaller differential voltage can be applied to new SA. The basic characterization is shown. Robustness is

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analyzed through the monte carlo simulation. Improvement ratio and power are also presented.

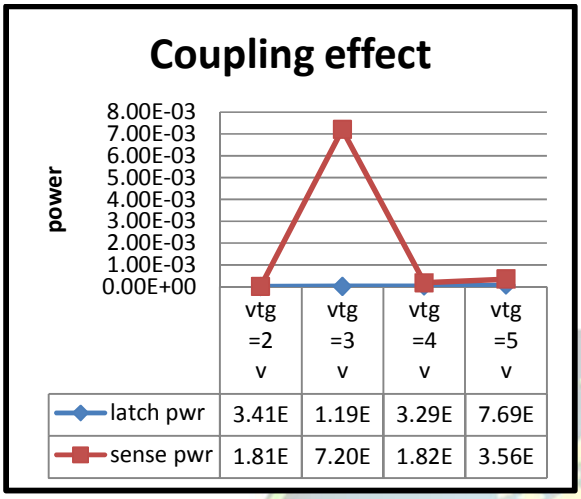


Fig 4: coupling effect reduction analysis; due to coupling effect sense amplifier achieves unstable state

Process variation is critical in the submicron CMOS circuit design, SA is a duplicate block in the memory and its small sensing feature makes it especially vulnerable. The monte carlo method is introduced for considering the process variation. It is a tool and is widely used in engineering, meterology, finance and so on. The monte carlo device models are supplied by foundaries and are already verified by their processes. In the simulation, the pseudorandom samples of SA are generated and applied. The simulation results are collected and analyzed. These statistical results are used for discussing the circuit robustness.

All samples will sense correct and we cannot get a fair standard for the difference in architecture. Of course, this case may only happen when we just read a very weak bit cell and yield is the only concern. A better SA can successfully sense a smaller differential voltage and avoid mistake. Fori is the number of failed samples of the original design. Fnew is the number of field samples of the new design. The improvement ratio is defined as

$$P_{\text{adv}} = \frac{F_{\text{ori}} - F_{\text{new}}}{F_{\text{ori}}}.$$

A normal differential voltage is applied. In this case all the samples can successfully work. A better SA means more stable read speed under a small supply voltages. In table 1 the power consumption of various supply voltage simulations are shown. The speed for new design is slightly faster than the old design as a larger valid differential voltage is obtained. The coupling effect is reduced and also the power reduces.

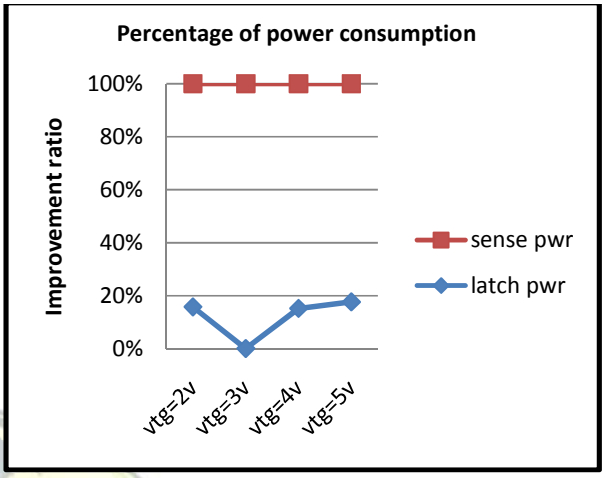


Fig 5: Improvement ratio analysis

| VOLTAGE (V) | SENSE AMPLIFIER | LATCH TYPE SENSE AMPLIFIER |
|---|---|---|
| 1.5 | 1.36e-005 | 1.81e-006 |
| 2 | 1.81e-005 | 3.14e-006 |
| 3 | 7.20e-003 | 1.19e-005 |
| 4 | 1.82e-004 | 3.29e-005 |
| 5 | 3.56e-004 | 7.69e-005 |

Table 1: Coupling reduction in terms of power using monte carlo method

## VI. CONCLUSION

In this paper, the coupling effect of the latch type decouple voltage SA is introduced. The coupling effects are serious and could not be omitted. When the process scales down. A new design is presented for reducing the harmful coupling. It can be seen that the robustness can be improved by the new designs against the harmful coupling with little power under different voltage, the new design can offer improvement steadily. It can be expected that, when entering 16nm or a smaller size era, the new design can play a more efficient role for an even smaller pitch.

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