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EFFICIENT POWER REDUCTION OF STATIC RANDOM ACCESS MEMORY

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Abstract— **Static random access memories are designed to provide high speed and low power consumption to the memory system. Due to aggressive scaling of devices low power design is important to meet the required constraints. This paper presents a bit interleaving 12T SRAM and 14T SRAM for high performance. In the existing method 10T SRAM having single ended decoupled read-bitline with a 4T read port was proposed. The power consumption of 12T SRAM is minimized by using power gating and clock gating techniques. 14T SRAM contains the sleep transistors to reduce the energy requirement of the cell. The proposed design achieves significant improvement in power, delay and noise. Finally the low power 12T and 14T SRAM cells are implemented in the 4×4 SRAM architecture.**

Keywords— Low power, SRAM, Power Gating, Clock Gating, 4×4 SRAM array, Transmission Gate.

I. INTRODUCTION

Random access memory allows data items to be read and written in approximately the same amount of time regardless of the order in which the data items are accessed. RAM is normally associated with voltaic types of memory (such as DRAM memory modules) where the stored information is lost if power is removed. Single ended Schmitt trigger based SRAM cell uses Schmitt trigger based inverter pair but its power consumption is high due to the degraded inverter characteristics [2]. The SRAM with capacitive charge share transient voltage collapse write access circuit reduces write energy by eliminating bias currents [4]. Trip point bitline precharge sensing scheme for single ended SRAM maintains the sensing margin but it consumes more power [6]. 9T SRAM with 1K bitline enhances write and read operation but it increases the area [7]. The 9T sub threshold SRAM reduces multi bit upset and enhance the soft error immunity but it requires additional negative BL and timing tracing circuit [9].

In section II we review existing 10T SRAM design. In section III we review proposed 12T SRAM design. In section IV we show the 10T and 12T SRAM designs with low power techniques. In section V we review proposed 14T SRAM design. In section VI we show implementation of 12T and 14T SRAM in 4×4 SRAM array.

II.EXISTING 10T SRAM

10T SRAM cell with single ended read bitline (RBL) is shown in fig1. The 4T read port is added to the conventional 6T SRAM cell. The 4T read port is used to decouple the internal nodes during the read operation. 4T read port consist of an inverter driven by the output node QB and transmission gate (P2-N2). The output node Z of the inverter is connected to the RBL during read operation through TG and controlled by read control signals.

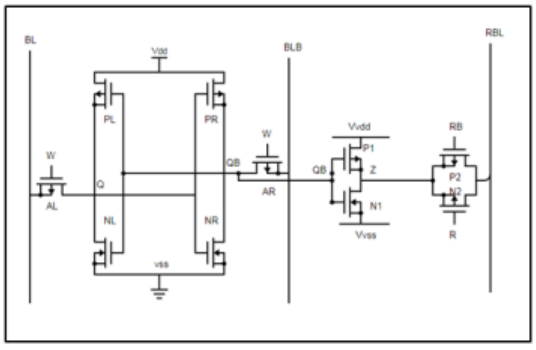

Fig1: Schematic diagram of 10T SRAM

Read port is powered by the virtual power rails (Vvdd and Vvss). In this design dynamically controlled power rails are used for read port. The RBL is charged or discharged from Vdd/2. For every read cycle the RBL will exhibit some changes from its precharged value.

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A. Precharge and Read Operation

The 10T SRAM is precharged by the value which is half of the supply voltage. For the read operation R goes high and RB goes low. The transmission gate is activated to connect RBL to the node Z. If QB is 0 N1 if OFF and P1 connect node Z to the Vvdd. The read current flows from Vvdd to RBL through TG. Then RBL voltage increases towards Vdd. For read 0 QB is 1, P1 turned off and N1 connects node Z to Vvss. The read current flow from RBL to the ground through the TG then RBL voltage decreases to 0v.

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III.12T SRAM DESIGN

The 12T SRAM cell uses extra word line for bit interleaving aware design and a feedback circuit for stable space applications. In the read operation the extra p type transistors are active according to stored bits and charge the storing nodes using bitline voltages. The fig.2 shows the 12T SRAM design.

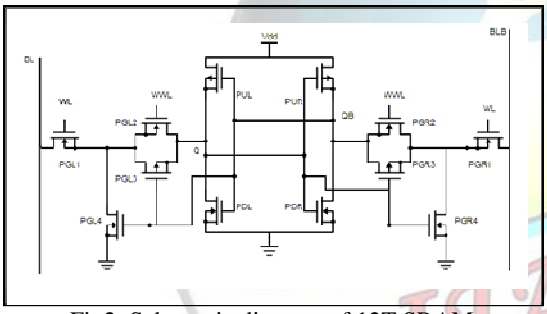

Fig2: Schematic diagram of 12T SRAM

PGL3 and PGR3 are feedback transistors. These are activated according to the stored data and refresh the storing node during the read operation. PGL2 and PGR2 are active in the write mode of operation along with the PGL1 and PGR1 access transistors PUL, PUR, PDL and PDR from the latch. PGL4 and PGR4 are the read transistors. PGL4 and PGR4 activate according to the stored data in the SRAM cell. WL, WWL and VGND are the major control signals for the SRAM and enables for the different mode of operation.

A. Read, Write and Hold Operation

PGL3, PGR3 play a major role in improving stability in the read operation. During the read operation bitlines BL and BLB are kept at VDD and the word line WL is enabled to turn on PGL1 and PGR1. Without loss of generality we assume Q and QB is 1 and 0 respectively. The read operation is performed by discharging the BLB through the read access transistor PGL4. Due to the voltage division between the QB and BLB it increases the Δv between the BL and BLB for read.

If read QB is more than the trip point voltage (Vtrip) of PUR and PDR, the value of the cell flips and a read failure occurs. Therefore to enhance the read stability of cell, we need to increase or decrease read Vtrip. In order to increase read Vtrip PUL needs to be stronger. Moreover reducing the leakage current of PDL increases read Vtrip value, and improves the read stability. To reduce the leakage current absolute value of the VT of PDL needs to be high. On the other hand PDR and PGR2 should be stronger than PUR to decrease Vtrip. Therefore for stable read operation desired transistor sizing is required.

B. Write Stability and Feedback Circuit

To write Q=0 into the cell the voltage of BL is set to 0, BLB set to Vdd and WL, WWL are activated. The right storage node QB charges through PGR1, PGR2 and is determined by the voltage division between PUR and PGR1, PGR2. If node voltage at QB becomes high than the Vtrip of PUL and PDL, the write operation is successful. To increase the write margin PGR1 and PGR2 should be stronger than PDR and trip voltage of PUL , PDL should be low enough. To do this PUL and PGL1-PGL2 should be stronger than the PUL. In addition increasing leakage current of PDR helps to charge QB and enhances the write margin. To minimize the leakage current the VT of PUR needs to be low. [5] proposed a system which contributes the complex parallelism mechanism to protect the information by using Advanced Encryption Standard (AES) Technique. AES is an encryption algorithm which uses 128 bit as a data and generates a secured data. In Encryption, when cipher key is inserted, the plain text is converted into cipher text by using complex parallelism. Similarly, in decryption, the cipher text is converted into original one by removing a cipher key. The complex parallelism technique involves the process of Substitution Byte, Shift Row, Mix Column and Add Round Key. The above four techniques are used to involve the process of shuffling the message. The complex parallelism is highly secured and the information is not broken by any other intruder.

C. Hold State

In the hold state bitlines are precharged to Vdd and the WL and WLL are kept at ground. PGL1, PGL2, PUL and PDL are in the sub threshold region and so their sub threshold currents should be low for low static power dissipation. As a result to reduce the leakage the desired transistor sizing should be 1 and 3 for PGL1, PGL2 and PUL1 respectively.

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IV.LOW POWER TECHNIQUES

A. Power Gating

The fig.3 and 4 shows the 10T SRAM and 12T SRAM with power gating respectively. Power gating is a technique used in integrated circuit design to reduce power consumption by shutting off the current to blocks which are not in use. In addition to reducing stand by or leakage power gating has the benefit of enabling Iddq testing. Power gating has additional consideration for time closure implementation. It is less sensitive to PVT variation introduces less IR-drop variation and imposes a smaller area overhead than the cell or cluster based implementation. In this design the power gating transistor is a part of the power distribution network rather than the standard cell.

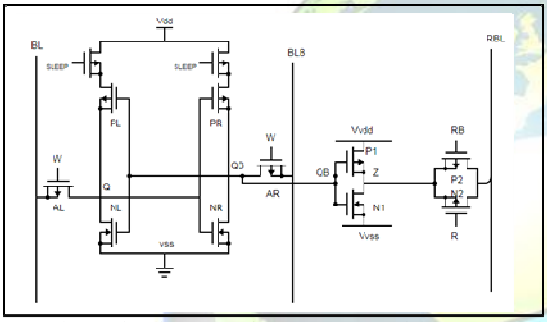

Fig3: Schematic diagram of 10T SRAM with power gating

Adding sleep transistor to every cell that imposes large area penalty and individually gating the power of cluster of cells creates timing issues introduced by inter-cluster voltage variation that are difficult to resolve. The sleep transistor technique is load here. Sleep transistors are turned on during the active mode in such a way that the normal operation is not affected as there exist the path between the supply and ground rails. They are turned off in stand b mode there by shutting down the power supply to the circuit creating the virtual supply and ground rails. This technique is popularly known as power gating.

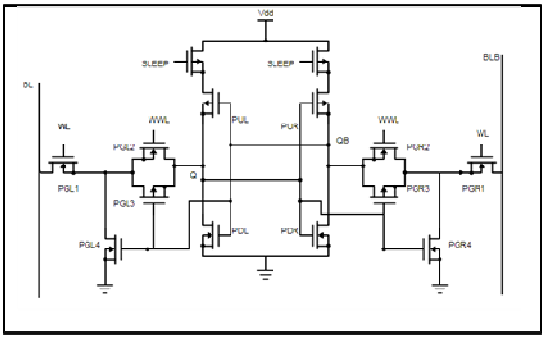

Fig4: Schematic diagram of 12T SRAM with power gating

The read and write operation for 10T, 12T SRAM with power gating is same as the normal 10T, 12T SRAM designs. But only difference is the sleep transistors for the power reduction by shutting off the current to the unused blocks.

B. Clock Gating

Clock gating is a popular technique used in many synchronous circuits reducing dynamic power dissipation. Fig.5 and 6 shows that the 10T SRAM, 12T SRAM with clock gating. Clock gating saves power by adding extra circuitry to reduce the clock tree. Reducing clock tree disables the portions of the circuitry so that flip flops in them do not have to switch states. Switching states consumes power when not being switched the switching power consumption goes to zero and leakage currents are incurred.

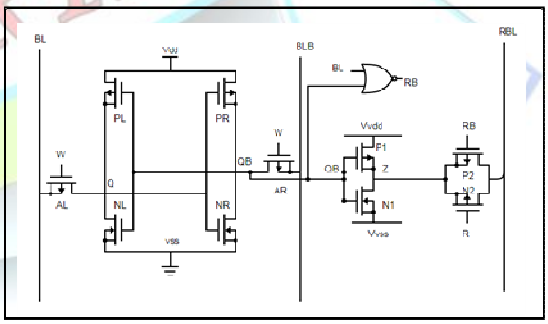

Fig5: Schematic diagram of 10T SRAM with clock gating

Clock gating works by taking the enable conditions attached to the registers and uses them to gate the clocks. Therefore it is imperative that a design must contain those enable conditions in order to use and benefit from clock gating. This clock gating process can also save significant die area as well as power since it removes large number of mux's and replaces them with clock gating.

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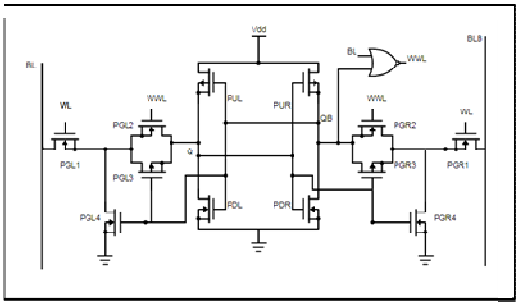

Fig6: Schematic diagram of 12T SRAM with clock gating

Clock gating logic can be added into a design in a variety of ways

1. Coded into the RTL code.
2. Inserted into the design manually by the RTL designers.
3. By instantiating library specific ICG cell.

In asynchronous circuits by definition do not have clock the term perfect clock gating is used to illustrate how various clock gating techniques are simply approximately of the data dependent behavior exhibited by asynchronous circuitry. In clock gating degradation is calculated is more while using either NOR or NAND output stage. Typically the tool will use a single kind of ICG for all clock gates NAND type of ICG cell. Yet if some of the clock gates neither were NOR based and some were AND based.

V.14T SRAM

14T SRAM cell is used to improve the write delay and power consumption of the cell. Fig.7 shows the schematic diagram of 14T SRAM. In this design transmission gate is an analog switch which can pass the signal in either direction. It removes the problem of passing both 0 and 1 by the PMOS and NMOS transistors. Transmission gate contains the both NMOS and PMOS so it can solve the above problem. The transmission gate also reduces the parasitic capacitance and resistance of the circuit.

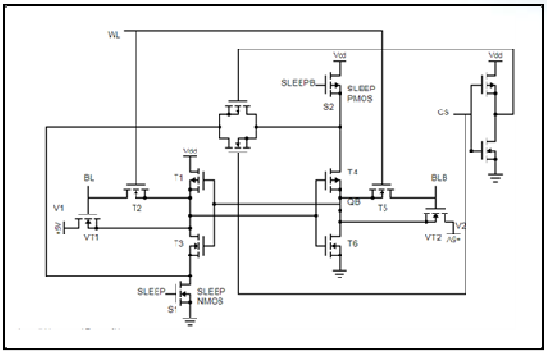

Fig7: Schematic diagram of 14T SRAM

A. *Sleep Transistors*

When the sleep signal is low then it turns on both the sleep NMOS and sleep PMOS transistors. Then it connects the virtual ground to the actual ground. Similarly the virtual supply is connected to the actual supply by the use of sleep transistor signals. During active period both transistor are work in the linear region. The voltages at the nodes of both transistors are at the 0 and Vdd respectively. For writing 1 into the cell the sleep transistors are turned off. They allow very low sub threshold leakage currents. Hence the power consumption also reduced.

B. *Voltage Swing*

As the transistors are switched from high to low and low to high at the bitlines, there is the need of swing voltage. It will leads to the dynamic power dissipation. This dynamic power dissipation should be reduced. In the 14T SRAM design two voltage source V1 and V2 are used with the bit and bitbar lines to reduce the dynamic power dissipation.

While writing 0 to the cell BL is low and BLB is high. Hence VT1 NMOS will turn off and VT2 NMOS is turned on to decrease the voltage swing of the BLB. For writing 1 BL is high and BLB is low. Then the VT1 will be turned on and VT2 will be turned off which decreases the swing voltage of the bit lines. The small area overhead of the cell can be overruled by the reduced 14T SRAM power consumption and delay of the cell.

C. *Charge Recycling*

When the circuit switches between the active and sleep mode, it leads to static power dissipation which is not commended for high speed operation. To reduce this static power dissipation a charge recycling technique is employed b the transmission gate connects the virtual power supply and virtual ground in the circuit. Charge recycling transmission gate is activated before turning on the sleep transistors i.e. from sleep to active mode and after turning off the sleep transistors i.e. from active mode to sleep mode to share the charge between the virtual ground and virtual supply nodes. It reduces the mode transition energy.

VI.IMPLEMENTATION OF SRAM

Implementation of SRAM contains four important blocks such as precharging, data write circuitry, 4×4 SRAM Array and

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sense amplifier. The block diagram of SRAM memory system is shown in fig.8.

A. *Precharging*

One precharging circuit is connected to the every column of the circuit. Precharging is not intended to deal with the ability to source drive current into a bit line. Precharge is intended to minimize propagation delay time.If there is no precharge, the maximum voltage swing in a readout is from a "0) to "1" (or vice versa), which happens in T01.

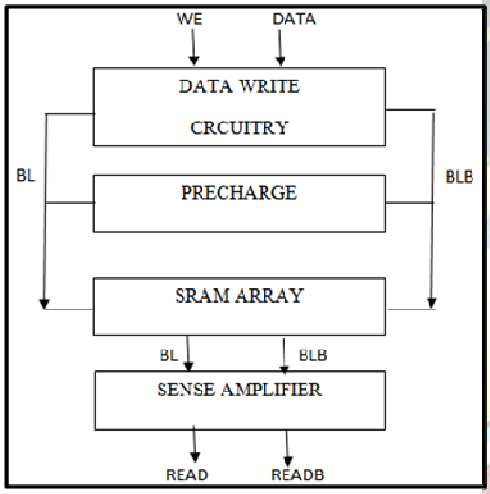

Fig8: Schematic diagram of 4×4 SRAM memory system

Pre charging ensures that the bit line is driven to voltage midway between "0" and "1", so that when the actual cell is read out, the line need only be driven from the midway voltage to either "0" or "1". This results in about one half the transition time (1/2*T01), and results in a faster memory. The main reason they charge the bitlines HIGH (in the circuit he is showing) and let them discharge is because the pass transistors are NMOS. This means they pass a very solid '0' but they pass a degraded '1'.So rather than start the bitlines low and let them pull up through the NMOS (slower and weaker, can only pull to VSUPPLY-VTH), they will start the bitlines high and let them pull down through the NMOS (which can pull down more strongly, to a solid '0'). Fig.9 shows the pre charging circuit.

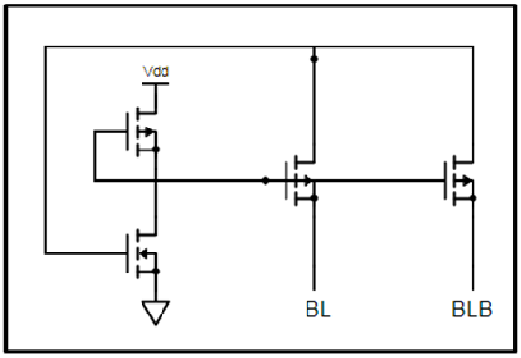

Fig9: Schematic diagram of precharging circuit

B. *Data Write Circuitry*

Each column of the memory array has one data circuit as shown in fig.10. The data write circuit consist of two invertors and an AND gate implemented by pass transistors. The data write circuitry writes data and its complement onto the bitlines when activated by write enable signal. The data and its complement are written onto the individual nodes Q and QB of the selected word through the access transistors of the sram cell.

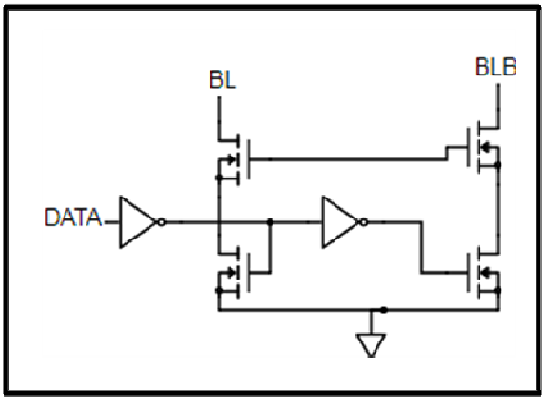

Fig10: Schematic diagram of data write circuit

C. *Sense Amplifier*

A sense amplifier shown in fig.11 is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a bitline that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly.

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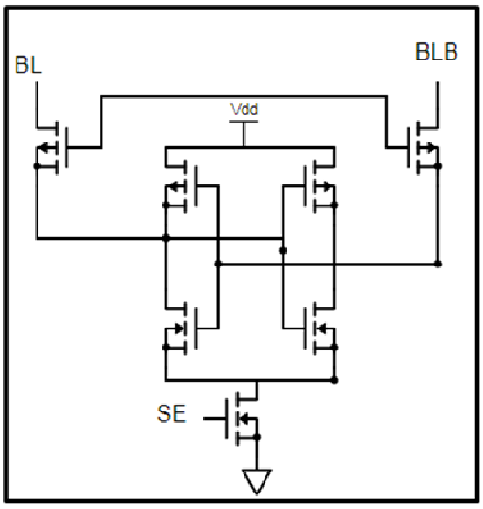

Fig11: Schematic diagram of sense amplifier

Fig.12 shows that the implementation of the 12T in memory system consist of precharging, data write circuitry and sense amplifier for a single bit.

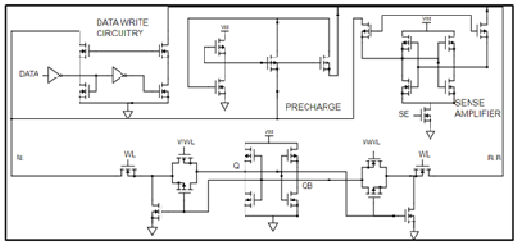

Fig12: Schematic diagram of implementation of 12T SRAM for single bit

Fig.13 shows that the implementation of the 14T in memory system consist of precharging, data write circuitry and sense amplifier for a single bit.

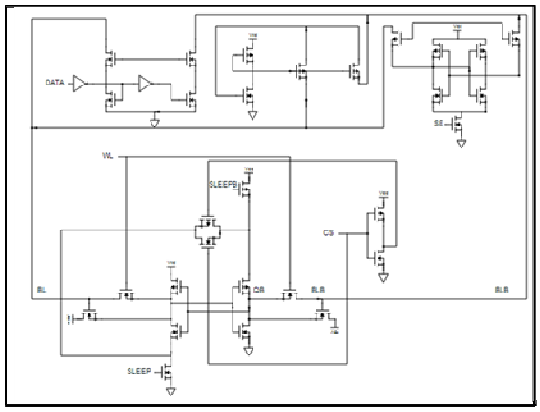

Fig13: Schematic diagram of implementation of 14T SRAM for single bit

VII.IMPLEMENTATION RESULTS

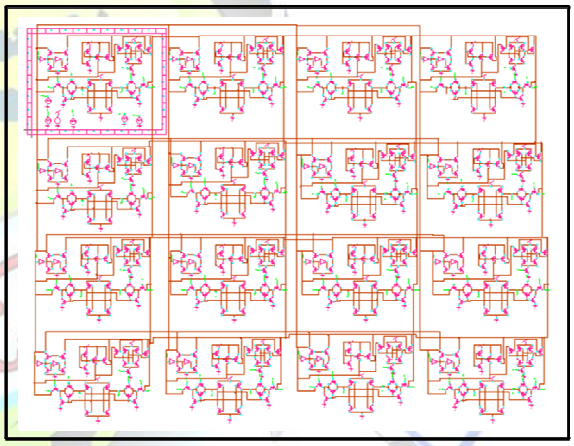

Fig14: Implementation of 12T SRAM in 4×4 Array

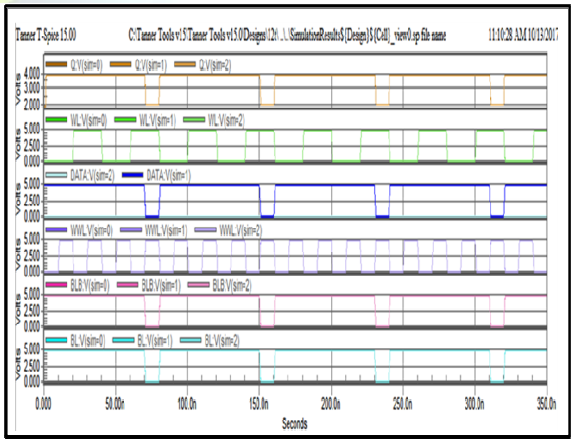

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Fig15: Simulation output of 12T SRAM in 4×4 Array

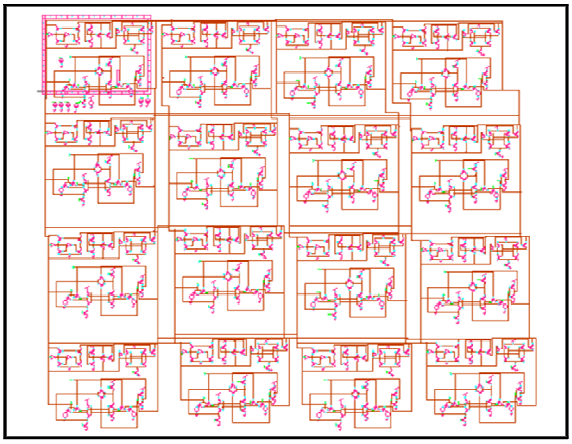

Fig16: Implementation of 14T SRAM in 4×4 Array

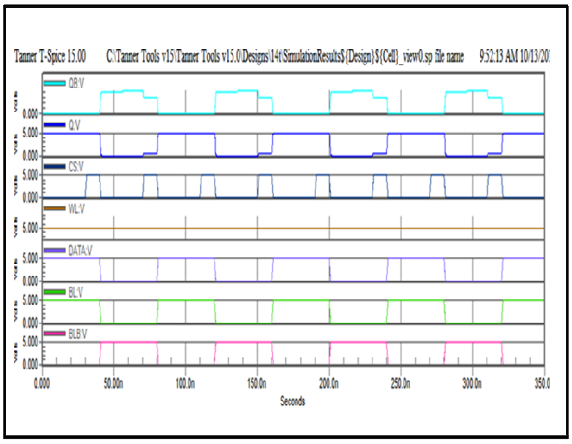

Fig17: Simulation output of 14T SRAM in 4×4 Array

Fig.14 and 16 shows the schematic diagram of implementation of 12T and 14T SRAM in 4×4 SRAM array. It contains the 4 rows and four columns of SRAM interconnected with the sense amplifier, data write circuitry and precharge circuitry. Fig.15 and 17 shows the one bit output of implemented 12T and 14T SRAM.

VIII.COMPARATIVE ANALYSIS

In 10T SRAM design static and dynamic power dissipation is reduced by the power gating and clock gating technique. 12T SRAM produces the bit interleaving architecture and power consumption is reduced by the low power techniques. The 14T SRAM contains the in build sleep NMOS and PMOS for the power reduction and the leakage is reduced by the transmission gate. The power consumption of different SRAM designs is shown in table 1.

IX.CONCLUSION

The proposed design aims at the lower power consumption. From the results it is clear that the power consumption of bit interleaving 12T SRAM is reduced by the low power techniques such as clock and power gating.

Design	Power in µw
10T SRAM	1602.186
12T SRAM	759.889
Design	Power in µw
10T SRAM with power and clock gating	501.2943
12T SRAM with power and clock gating	1.510633
14T SRAM	0.000071

Table1: comparative analysis of power consumption

The 14T SRAM contains the in build sleep transistors for power reduction and transmission gate for the parasitic resistance and capacitance reduction. The designs of both 12T and 14T SRAM is implemented in 4×4 SRAM architecture.

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