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Design, Analysis and Implementation of PNAND Cell Using Sense Amplifier Energy Recovery Flip-Flop

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***Abstract*— This paper demonstrates an unconventional approach to compute logic function in ASIC's, and a fully automated approach for technology mapping in standard cell ASIC's using a novel cell. In this approach based on a design of Threshold Logic Gates (TLG's) and their seamless integration with conventional standard cell design. The novel cell provides a reduction in dynamic power, leakage, wire length and area without sacrificing performance of the design. To achieve the threshold function first describes a new robust, standard cell library of configurable circuits. The threshold gate behaves as a multi input, single output, edge triggered flip-flop, which computes a threshold function of the inputs on the clock edge. In this paper presents a method of signal assignments for the inputs of a threshold gate to realize a given threshold functions. The mapping algorithm is based on logic decompositions into specific threshold function. The sense amplifier energy recovery flip-flop are implemented on standard cell ASIC's. The SAER flip-flop reduces the CLK-Q delay and improving the timing performance of the flip flop. The flip-flop is used to operate with an energy recovery clock. The simulation results are obtained from the simulation of standard cell ASIC's using Cadence Virtuoso 180nm process technology.**

Keywords*—Threshold logic, Tehnology mapping, low power technology, Sense Amplifier Energy Recovery (SAER) flip-flop.

I. INTRODUCTION

Efforts to reduce power consumption of digital CMOS circuits have been in progress for nearly three decades [4]. The static power dissipation can be reduced by using stack transistors, using dual voltage supply and dual threshold voltages. The new standard cell ASIC aims at high volume consumer computing and communication markets which are driven by end user requirements for low power and cost. The methods to minimize the static and dynamic power level have been explored thoroughly since most of the techniques are used and implemented in the logic/circuit level. Consequently, the focus has shifted to the higher levels of design, including power efficient micro architectures, memory, compilers and OS and system level control, including thermal aware dynamic frequency and voltage control.

A CMOS Application Specified Integrated circuit using static logic is a multilevel network of AND/OR logic gates. A proper subset of unate Boolean function called threshold function, which can be computed by several mechanisms, the possibility of further improvements in power consumption, performance and area, which has not been sufficiently explored.

Let X= $(x_1, x_2,.....,x_n)$, $x_i \in \{0, 1\}$, **w** = (w_1, $w_2,....,w_n$), $w_i \in R$, and $T \in R$. An unate Boolean function F(X) is called a threshold function.

$$F(X) = \begin{cases} 1 & \text{if } w'X \geq T \\ 0 & \text{otherwise} \end{cases}$$

Without the loss of generality, the weights W and threshold T can be assumed to be positive integers. The example of threshold functions:

$$F(a, b, c) = ab \vee bc \vee ac$$
$$= [w_a= 1, w_b= 1, w_c= 1; T=2]$$
$$= [1, 1, 1; 2].$$

A threshold function can be implemented as any logic function, as a network of logic primitives or a pull up network and pull down network of p FETs and n FETs. In this paper a design of ASIC using

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Sense Amplifier Energy Recovery flip-flop is described. The energy recovery clocking results in substantial reduction in clock power there still remains some energy loss due to resistances of the clock network and loss of energy in the oscillator due to uncontrolled switching. The sense amplifier energy recovery flip-flop is based on the sense amplifier flip-flop, is a dynamic flip-flop with precharge and evaluates phases of operation. This flip-flop is used to operate with an energy recovery clock. [5] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm .By this design, the power dissipation, delay and noise can be reduced.

In this paper, a methodology for ASIC design with SAER flip-flop s described [1]. It includes the robust architecture of Threshold Logic Gates (section 1), Design of Sense Amplifier Energy Recovery (SAER) flip-flop (section 2), standard cell ASICs using SAER (section 3), Experimental results (section 4), and conclusion (section 5).

II. ARCHITECTURE OF THRESHOLD LOGIC GATE

A. Threshold gate

A differential threshold circuit called as a "PNAND" fig. 1 shows the schematic of the threshold gate with k-inputs referred to as PNAND-k. It consists of three components: (1) left input network (LIN) and a right input network (RIN), each with n-inputs driving PMOS transistor, (2)a sense amplifier (SA) (pair of cross coupled NAND gate) and (3)a set-reset(SR) latch. The effective conductance of each input network depends on the number of ON transistors. Note that an NMOS input network would requires a NOR type sense amplifier, which would be less robust and have more delay than a PNAND. A circuit implementation of threshold function is called threshold gate.

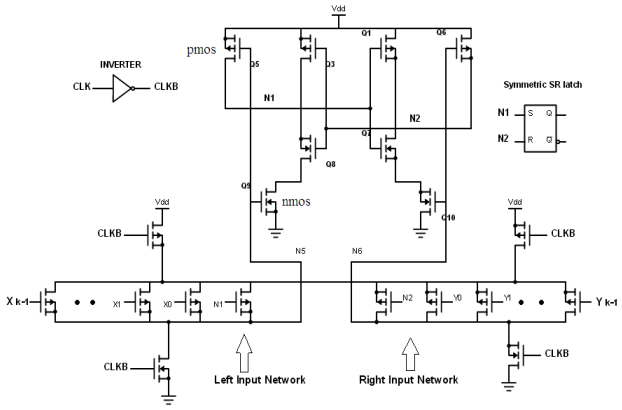

Fig. 1: PNAND cell architecture

B. Cell operation

The cell is operated in two phases: reset(CLK=0) and evaluation (CLK 0 1). In the reset phase CLK=0, the two discharge devices M18 and M19 pull nodes N5 and N6 low, which turn off M5 and M6. The nodes N1 and N2 are 1 and SR latch maintains the last state. Without loss of generality, assume that the LIN has more ON transistors than the RIN and therefore has a higher conductivity. In the evaluation phase when clock rises from 0 to 1, node N5 and N6 both rise to 1 at different states. Due to the higher conductivity of the LIN, node N5 will start to rise first, which turns on M5. The output node N1 is 0 and N1 is 1. As the circuit and its operation are symmetric, if l < r, l active devices in the LIN and r active devices in the RIN, then the evaluation will result in N1=1 and N2=0.

The active low SR latch stores the signals N1 and N2. During reset, when (N1, N2) =1, the SR retains its state. After evaluation, if (N1, N2) = (1, 0), Q=1, providing a dual rail output for the threshold function being computed.

C. Threshold functon realization

The threshold function variables are connected to the inputs of a PNAND-k cell such that output of PNAND is 1. The threshold function evaluates to 1. The actual function implemented by a PNAND –k depends on the inputs signal assignment (SA). The procedure always ensures that LIN and RIN never have the same number of ON transistors. For a PNAND-k, an L/R refers to l and r active transistors in the LIN and RIN. For example PNAND-5 can implement eight threshold functions to be computed. SA = (a, b, c, d, e | a, b, c, d, e) implements abc + abd + abe + cad + ace + ade + bcd + bce + bde + cde.

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Note that the optimal signal assignment (OSA) is used to optimize the cell.

The generic PNAND library consists of 7 basic cells depending on fan-in: PNAND-1, 3, 5, 7, 9, 11 and 13. For each cell, the set of threshold functions that can be realized by that cell under OSA, are enumerated. All the functions within such a group can be realized by the same physical PNAND-k cell without any impact on performance power or area. Using process variation statistics provided by the foundry, no failures were found in 100k Monte Carlo simulation accounting for global variations and local mismatch, ensuring the robustness of the PNAND cells. The Fig.2 shows the simulation results of Standard Cell ASIC.

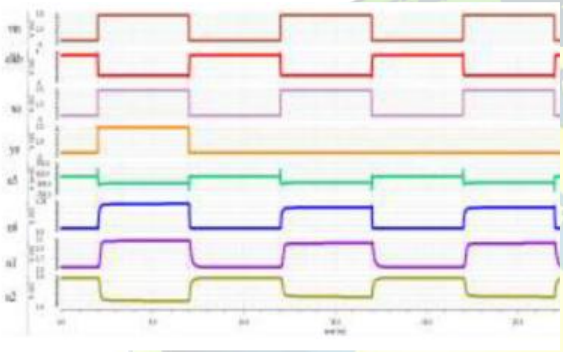

Fig.2 Simulation results of Standard Cell ASIC

D. Scan implementation

If PNAND cells are to replace flip-flops and logic cones feeding them, scan capability is necessary. There exist several
ways to implement scan for a PNAND cell. The simplest way to make a D-FF scannable is to use a mux that selects between the input D and the test input (TI), depends on whether or not the test mode is enabled (TE). This is not practical for a multi input flip-flop, such as PNAND cell. The scan implementation has negligible performance and robustness during normal operation. Fig.3. shows the PNAND design with scan. The additional transistors for scan are labeled as *S*1through S6. In the normal mode, the signals TE and TI are both 0, which disables the scan related transistors (s1-s4), and reduces the circuit function to the one shown in Fig.1.in the scan mode, the TE signal acts as a clock. The Signal global TI (GTI) is the entry point for the scan data input to the PNAND chain.

1) Set CLK = 0 and TE = 0.

2) Set GTI = *i* th bit of the input (*i* = 0 initially).

3) Set TE = 1. Each PNAND registers its TI input.

4) Set TE = 0.

5) Increment *i* and repeat until the end of stream.

The pull-up transistors *S*5 and *S*6 are included to eliminate a dc path during testing. In the absence of these transistors, when TE is asserted (0 1), while CLK=0, M7 is active, and there is a dc path VDD M7 S1 S2 GND.

III. SENSE AMPLIFIER ENERGY RECOVERY FLIPFLOP

The clock distribution network consumes about 70% of the total power of modern microprocessor. Clock power dissipation will increase as the complexity of the VLSI systems increase [6, 7]. Some energy recovery flip-flops are Sense Amplifier Energy Recovery flip-flop (SAER), Static Differential Energy Recovery flip-flop (SDER), Differential Ended Conditional Capturing Energy Recovery flip-flop (DCCER).

In this section discuss about the Sense Amplifier Energy Recovery flip-flop which is having the characteristics like reduced dynamic power dissipation due to reduction in number of transistors. It avoids charge sharing and charge leakage and it exhibits negative setup time. The clock signal consumes more power; a relevant solution for this issue is using a resonant clock. Power clock signal having sinusoidal or trapezoidal shape having inherent circuit characteristics to recover all the energy used in the charging the nodes.

This flip-flop is used to operate with an energy recovery clock. When the clock voltage exceeds the threshold voltage of the clock transistor (MN1), evaluation occurs. It was seen that, at the onset of evaluation, the difference between the differential data inputs (D and DB) resulted in an initial small voltage difference between SET and RESET nodes. This initial small voltage difference is then amplified by the cross coupled inverter, resulting in either SET or RESET switches to low.

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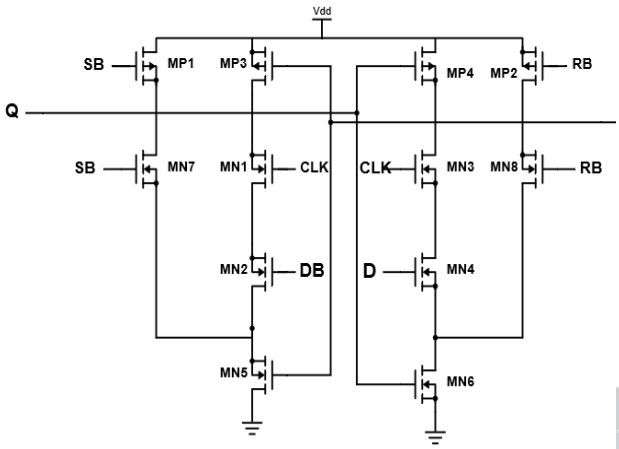

Fig.3. Sense Amplifier Energy Recovery flip-flop (SAER)

This state transition is captured by the set/reset latch (cross coupled NAND gates) and retained for the rest of the cycle time until next evaluation occurs. The SET and RESET nodes are precharge high when the clock voltage falls below V_{dd}- V_{tp}, where V_{tp} is the threshold voltage of the precharging transistors (MP1 and MP2). Even though the SAER flip-flop is fast and consumes low power at high data switching activities, its main drawback is that either the SET or RESET node is always charged and discharged in every cycle, regardless of the data activity. This leads to considerable power consumption at low data switching activities where the data is not changing frequently. Fig.4. shows the simulation results of SAER flip-flop.

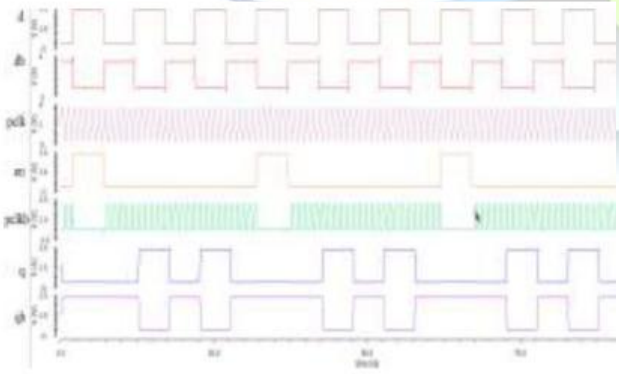

Fig.4. Simulation results of SAER flip-flop

IV. STANDARD CELL ASIC USING SAER FLIP FLOP

The design of the Standard Cell ASIC using the SAER can be implemented by replacing the Set-Reset Latch in the architecture by using the SAER [10]. As the number of transistors decreases, the power consumption will be reduced. Also the SAER is a D flip-flop hence the problem of not allowed state of SR latch can be eliminated. The D flip-flop passes what we are giving at the input. Fig.5. shows the standard cell ASIC using SAER flip-flop.

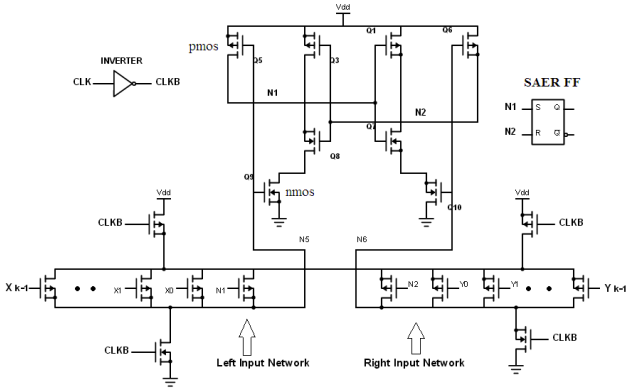

Fig.4. standard cell ASIC using SAER flip-flop

This SAER is designed to reduce CLK-Q delay and power consumption of the flip-flop. The circuit operation is as follows: at CLK= "0", both outputs S and R of sense amplifier are pre-charged to V_{dd}. During the pre-charge, the transistors MN7 and MN8 and cross coupled inverters composed of keeper transistors MP3, MP4, MN5 and MN6 in slave latch holds the flip-flop states and makes the SAER flip-flop static. Now, let us examine the flip-flop operation: assume that D is "1" at the rising edge of the clock then sense amplifier drives
$\overline{S}$ = "0" and $\overline{R}$ = "1". The transistor MP1 associated to input
$\overline{S}$ ="0" gives output Q="$\overline{1}$". Including one stage delay caused by the sense amplifier, the SAER flip-flop presents three stage delays for high to low output transition [4].

The pull down transistors avoid the simultaneous conduction of pull up and pull down transistors of inverters which results in lower leakage power loss. Let us assume that at time t = 0, outputs Q = "1" and QB = "0". Now if D is changed to "0" with rising clock CLK then R switched to "0" and S to "1".

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Consequently QB changed to "1" through strong MP2 and therefore output Q switched to "0". Thus three stage delays occurred to pull down the output in SAER flip-flop. The transistor MN5 in SAER will have to wait for the time taken by the sense amplifier in charge of the output node S through minimum sized PMOS transistor MP3. The SAER flip-flop the high to low output delay at Q is caused by the pull down stacked transistors MN1, MN2 and MN5 associated with signals CLK, D and QB respectively. Fig.5.shows the simulation results of standard cell ASIC using SAER flip-flop.

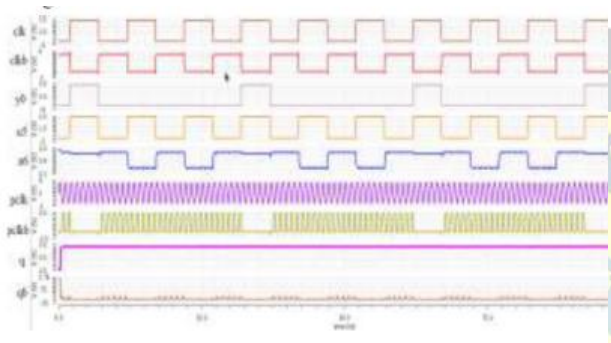

Fig.5.simulation results of standard cell ASIC using SAER flip-flop

Table.1. Comparison of Standard Cell ASIC's using SR latch and SAER

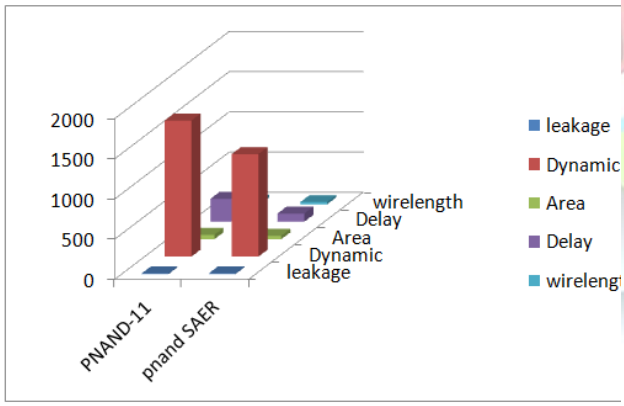

Fig.6. Comparison graph of PNAND cell and PNAND cell with SAER flip-flop

The Table.1 shows the performance comparison of standard cell ASIC using SR latch and SAER.

TABLE-I

Circuit	Dynamic Power (nw)	Leakage Power(nw)	Delay (ps)	Area	Wire length
Standard Cell ASIC using SR Latch	1693	8.9	286	54 μm^2	35
Standard Cell using SAER	1275	7.53	102	42 μm^2	28

V. CONCLUSION

In this paper, we have proposed the design of a Standard Cell ASIC's using Sense Amplifier Energy Recovery Flip Flop. The circuit is implemented using cadence 180nm technology. The proposed design achieves lower power consumption as compared to the already existing Standard Cell ASIC's design. The Dynamic and leakage power consumed by the Standard Cell ASIC's using SAER is 1275n Watt and 7.53nWatt and its delay is only 102ps which is much lesser than that of the ordinary standard cell. Hence, by implementing the proposed design of standard cell ASIC and inserting it into the standard cell library it's possible to design a number of energy efficient as well as fast systems.

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