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DESIGN OF ASYNCHRONOUS LOGIC QDI CELL TEMPLATE USING CURRENT CONTROLLED LATCH

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***Abstract*— An asynchronous logic quasi delay insensitive sense amplifier half buffer cell design using current controlled latch, with emphases on high operational robustness, high speed and low power dissipation. In a SAHB design there are five key features are there. First, the SAHB cell is designed using the asynchronous QDI 4-phase (4ω) signaling protocol to accommodate process voltage temperature variations. Second, the sense amplifier block in a SAHB cells are designed using the current controlled latch to a lower input capacitance. Third, the evaluation block in the SAHB comprises both nMOS pull-up and pull-down networks with minimum transistor sizing to reduce the parasitic capacitance. Forth, both the evaluation block and SA block are tightly coupled to reduce redundant internal switching nodes. Fifth, the SAHB cell is designed in CMOS static logic. In this sense amplifier half buffer there are six library cells are designed**.

***Keywords*— 4-phase (4ω) protocol, asynchronous logic circuits, dual-rail encoding, process-voltage-temperature variations, quasi-delay-insensitive (QDI) circuits**.

I. INTRODUCTION

As the feature size continues to shrink and the corresponding transistor density increases, power dissipation has become an important concern in nanoscale CMOS VLSI design [2]. Power dissipation in CMOS circuits can be categorized into dynamic dissipation and static dissipation. Dynamic power is the power dissipated when the device is active, and static power is the power dissipated when the device is powered up but no signals are changing their values [3]. In the highest classification, there are the synchronous and asynchronous digital logic design philosophies. As the synchronous digital logic design philosophy requires timing assumptions associated with the clocks, realizing operationally robust circuits under large PVT variations is challenging, where large timing margins are required to accommodate the worst case conditions. In the asynchronous digital logic design philosophy, particularly the quasi-delay-insensitive (QDI) approach, is an alternative approach to mitigate the timing assumptions [1]. There are three types of the asynchronous digital logic design. These are [4]: 1) Delay insensitive (DI); 2) Bundled data (BD); 3) Quasi delay insensitive/ Timed pipeline(TP)/ Single track(ST). The DI circuits, they are largely impractical because they make no assumption on the gate/wire delays. In BD circuits, they are similar to synchronous circuits, requiring delay assumptions for circuit realization [6], [7]. QDI circuits operate error free for arbitrary wire delays and assume isochronic forks [8]. The QDI circuits, there are two pipeline structures are available. 1) data control decomposition (DCD) 2) Integrated latch pipelines [9]. The DCD pipeline separates asynchronous controller and data paths. Such pipelines are simple but less speed efficient. The QDI cell design approaches with the DCD pipeline include three types. These are the 1) Delay insensitive minterm synthesis 2) Null conversion logic and 3) Precharged static logic. The IL pipeline in more speed efficient, it incorporates a pair of asynchronous controller and logic cell to form a microcell pipeline stage. The resulting is shorter critical path. The asynchronous QDI cell design approaches with the IL pipeline. There are many cell approaches in the IL pipeline. These are the PS0, LP2/1, SAPTL, PCHB STAPL STFB and SAHB [10].

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In this paper, we propose the SAHB- a novel QDI cell using the current controlled latch design approach with emphases on high operational robustness (i.e. error free) high speed and low energy dissipation. There are many features in the SAHB. 1) The SAHB cell incorporates an evaluation block and sense amplifier block. To perform an asynchronous 4-phase QDI logic operation [8], in the presence of PVT variations. 2) The SA block used in current controlled latch with positive feedback mechanism to speed up and latch the output.3) The evaluation block only used both nmos pull up and pull down network to reduce the parasitic capacitance and reduce the power dissipation in the circuit.4) The evaluation block and the sense amplifier block are tightly coupled to reduce the switching nodes and hence short cycle time and low power dissipation.5) The SAHB cell is designed using the cmos static logic. This paper is organized as follows. Section 2) presents the SAHB cell design approach and its attributes are benchmarked against reported competing async cell design approaches. Section 3) describes the modified SAHB approach. Section 4) implementation of 4-bit SAHB pipeline adder and the sync counterparts. Finally, conclusions are drawn in Section 5.

II. SAHB APPROACH

A. *Standardization of Interface Signals*

Fig. 1 shows the data inputs are Data and nData and the data outputs are QT/QF and nQT/nQF. The left-channel handshake outputs are La and nLa, and the right-channel handshake inputs are Ra and nRa. nDatain, nQT, nQF, nLa, and nRa are logical complementary signals to the primary input/output signals of Data, QT, QF, La, and Ra, respectively.

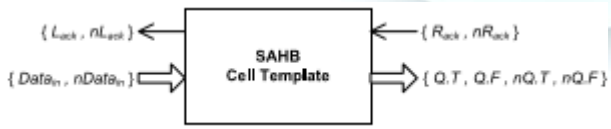

Fig.1. SAHB QDI Cell

For the sake of brevity, we will only use the primary input/output signals to delineate the operations of an SAHB cell. The SAHB cell strictly abides by the asynchronous 4-phase (4φ) handshake protocol—having two alternate operation sequences, evaluation and reset. Initially, La and Ra are reset to 0 and both Datain and QT/QF are empty, i.e., both of the rails in each signal are 0. During the evaluation sequence, when Datain is valid (i.e., one of the rails in each signal is 1) and Rack is 0, QT/QF is evaluated and latched and La is asserted to 1 to indicate the validity of the output. During the reset sequence, when Datain is empty and Ra is 1, QT/QF will then be empty and La is deasserted to 0. Subsequently, the SAHB cell is ready for the next operation. The evaluation and SA blocks are powered, by VDD. The nMOS transistor in green with RST is optional for cell initialization.

Fig. 2 shows the evaluation block comprises an nMOS pull-up network and an nMOS pull-down network to, respectively, evaluate and reset the dual-rail output QT/QF. Of particular interest, the nMOS pull-up network features low parasitic capacitance (lower than the usual pMOS pull-up network whose transistor sizing is often 2× larger than that of the nMOS). Consider first the nMOS pull-up network where QT/QF is evaluated based on the data input (i.e., AT/AF), and nRa serves as an evaluation flow control signal. The nMOS pull-up network realizes the buffer logic function as expressed in (1). To reduce the short-circuit current, nQT/nQF will disconnect the evaluation function when QT/QF is evaluated

QT = AT; QF = AF ---------- (1)

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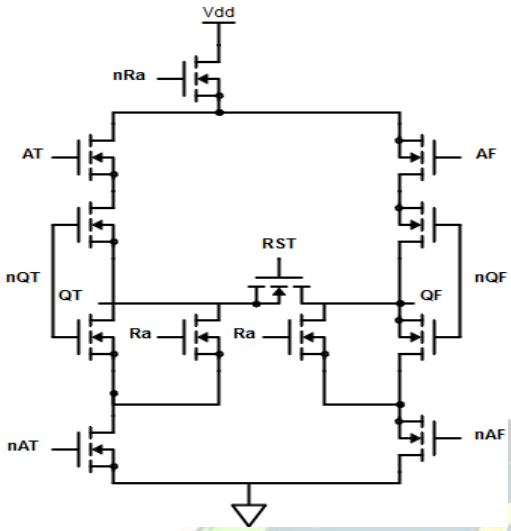
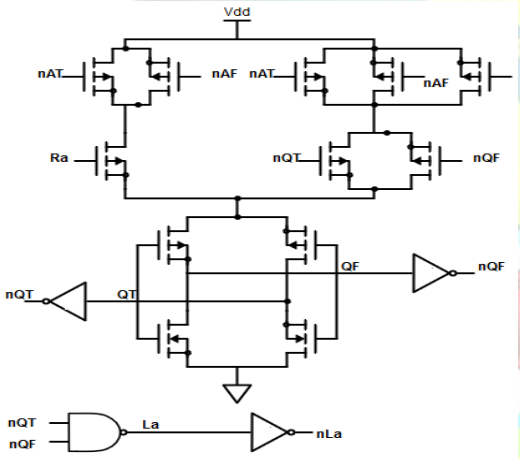


Fig. 2. Evaluation block



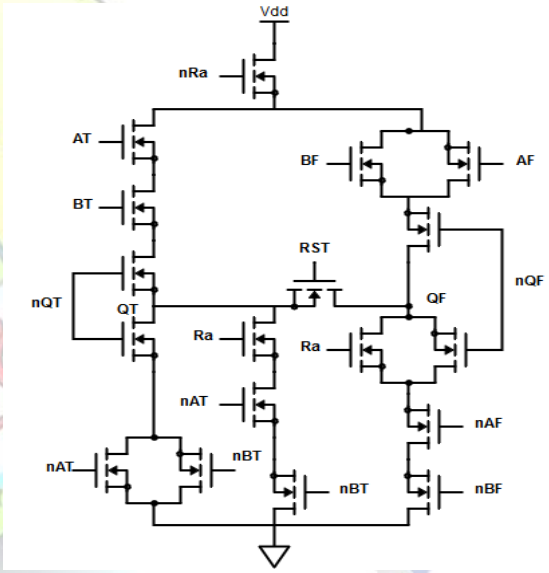


Fig.3. Sense Amplifier block

Consider now the nMOS pull-down network where QT/QF is reset depending on the data input. The transistor configuration of AT/AF in the pull-up network is a series–parallel topology to the transistor configuration of nAT/nAF in the pull-down network. For examples of two-input and three-input cells, Fig. 4 Depicts two-input AND/NAND. Ra serves as the reset flow-control signal, connecting in series the data input for input completeness. Fig. 3 the SA block comprises an SA cross-coupled latch, complementary buffers, and a completion circuit. The SA cross-coupled latch amplifies and latches QT/QF. The complementary buffers and completion circuit, respectively, generate the complementary output signals (nQT/nQF) and the left-channel handshake signals (La/nLa).

The cross-coupled inverters serve as an amplifier where in the reset phase, both QT and QF are 0. During the evaluation phase, the cross-coupled inverters will amplify (in a positive feedback mechanism) the voltage difference between QT and QF.

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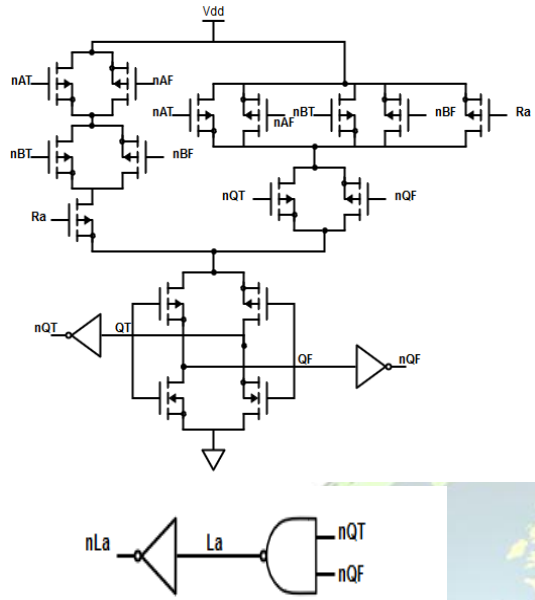

Fig. 4. Library cell 2 input AND/NAND cell

To realize the input completeness feature, the top left branch in the SA cross-coupled latch detects if all inputs (i.e., nAT and nAF) are ready and Ra =0. For bistable operation, the top-right branch (within the dotted oblong circle) in the SA cross-coupled latch holds the output until all inputs are empty and Ra =1.

B. Operations of SAHB

Initially, AT, AF, Ra, and La are 0 and nAT, nAF, nRa and nLa are 1. During the evaluation phase, for example, when AF = 1(nAF = 0), the voltage at node QF is partially charged to VDD by the nMOS pull-up network in the evaluation block and QT remains as 0 (via the nMOS pull-down network). As the input is now valid, the SA cross-coupled latch is turned ON by connecting the virtual supply VDD and amplifies QF to 1. QF is thereafter latched (together with the pMOS bistable transistors and the cross-coupled inverters) and nQF becomes 0. La is asserted to 1 (nLa = 0) to indicate the validity of the dual-rail output. During the reset phase, the input is empty (nAT and nAF are 1) and Ra = 1, the dual-rail output becomes empty and La is deasserted to 0. At this juncture, the SA block is ready for a new operation. Note that both the evaluation block and SA block are tightly coupled to reduce the number of switching nodes, thereby enhancing the speed and reducing the power dissipation. Furthermore, as both the evaluation and SA blocks operate in static logic style, their transistor sizings are not critical. [5] proposed a novel method for secure transportation of railway systems has been proposed in this project. In existing methods, most of the methods are manual resulting in a lot of human errors. This project proposes a system which can be controlled automatically without any outside help. This project has a model concerning two train sections and a gate section. The railway sections are used to show the movement of trains and a gate section is used to show the happenings in the railway crossings. The scope of this project is to monitor the train sections to prevent collisions between two trains or between humans and trains and to avoid accidents in the railway crossings. Also an additional approach towards effective power utilization has been discussed. Five topics are discussed in this project : 1) Detection of obstacles in front of the train;2) Detection of cracks and movements in the tracks;3) Detection of human presence inside the train and controlling the electrical devices accordingly 4) Updating the location of train and sharing it with other trains automatically 5) Controlling the gate section during railway crossing. This project can be used to avoid accidents in the railway tracks.

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C. *Library Cells*

Depicts the circuit schematic of three basic SAHB library cells: 1) two-input AND/NAND cells. The logic functions of the pull-up network for AND/NAND, XOR/XNOR, and AO/AOI cells are, respectively, expressed in (2). Similar to the buffer cell, the structure of the evaluation block and SA blockof these cells are constructed based on their logic functions and input signals. Table II tabulates the various power analysis of library cells.

$$QT = AT \cdot BT$$

$$QF = AF \cdot BF \qquad \text{----------} \qquad (2)$$

III. MODIFIED SAHB APPROACH

The current sense amplifier circuit operation is two fold: To detect and to amplify differential currents between its input. Current sense amplifiers have an advantage over voltage based sense amplifiers because they have a lower input capacitance. This is useful in increasing the sense speed of the sense amplifier circuits.

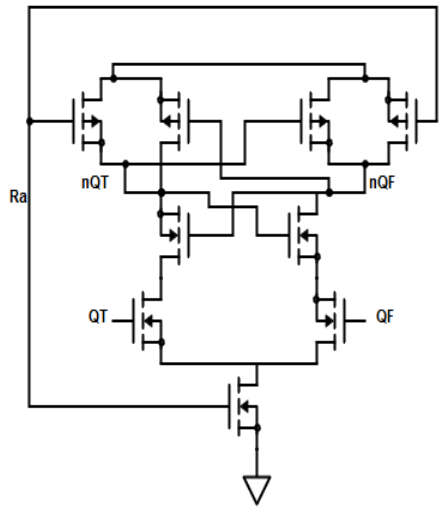

Fig. 5. Currernt controlled latch

IV. IMPLEMENTATION OF 4-BIT KOGGE STONE ADDER

Demonstrate the advantages of SAHB approach by constructing an adder circuit. Fig. depicts the pipeline architecture of 4-bit Kogge-Stone tree adder (i.e. 4-bit pipeline adder). The 4-bit pipeline adder consists of 15 BUFFER cells, 6 AND/NAND cells, 8 XOR/XNOR cells, and 5 AO/AOI cells. Based on our proposed TCIP approach, we apply WCHB BUFFER, SAHB AND/NAND, ASVHB XOR/XNOR and SAHB AO/AOI to form the 4-bit adder (i.e. proposed SAHB adder).

The realization of the SAHB pipeline blocks in group propagate–generate (PG) logic in terms of symbol view, cell view, and SAHB design view. The primary input operands of the adder are A= A3···A0, B= B3···B0, and carry-in Cin. The primary output operands are S = S3···S0

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and carry-out Cout. For the sake of illustration, the async handshake signals (and their complementary signals) are not shown. The SAHB adder (consisting of a bitwise PG logic, a group PG logic, and a sum logic) is constructed in a multiple carry look-ahead tree level so that the carry propagation time is shortened, thereby increasing speed. The handshake signal to the preceding pipeline stage (Ackn−1) is asserted when the SAHB pipeline cells have evaluated their outputs or deasserted when the SAHB pipeline cells have reset the outputs to empty. The handshake signal from the succeeding pipeline stage (Ackn) indicates whether the outputs G(i:k)n and/or P(i:k)n are accepted by the next connecting SAHB pipeline cells.

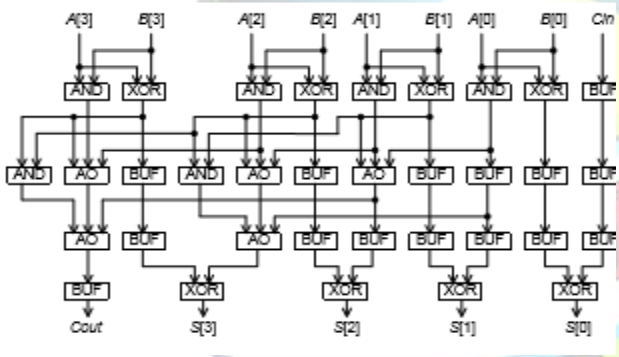

Fig. 6. 4-bit kogge stone adder

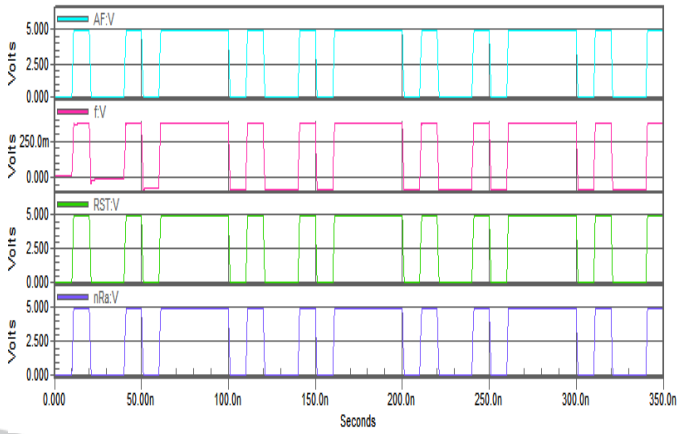

Fig. 7. Simulation results of SAHB approach

TABLE I

S.No	Library cells	Power(µw)	Area
1.	1-input buffer	3.75	36
2.	2-input AND/NAND	3.95	46
3.	Current controlled latch	5.42	29

Characteristics	SAHB
Logic family	Static
Classification	Asynchronous
Timing approach	QDI(Quasi-delay-insensitive)
Handshake	4-phase
PVT variations	Accommodating
Pipeline structure	Fine grain gate level
ICD(Input completion detection)	Not required
OCD(Output completion detection)	Required
Input buffer	Required
Static slack(%)	50

V . CONCLUSION

A novel SAHB realization approach with emphases on high operational robustness, high speed, and low energy dissipation. These attributes are collectively achieved by several circuit designs or operations, including QDI-compliant operation, cross-coupled latch with a positive feedback mechanism in the SA block, reduced switching nodes in the evaluation and SA blocks, minimum sizing of

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the NMOS pull-up network in the evaluation block, and static operation. The basic library cells embodying SAHB have been higher speed, low energy dissipation, and lower transistor count (and smaller IC area). The 4-bit SAHB adder has been implemented for power management application.

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