ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 23, December 2017

Fault Tolerance Technique Using MSR Logic For Combinational Circuits

Ms.Kodieswari.P[(1)] ,Ms.Geeta.R[(2)],Dr.Ramasamy.K[(3)]
PG Student[(1)], Assistant Professor[(2)],Principal[(3)]
Department of ECE[(1),(2),(3)]
P.S.R.Rengasamy College of Engineering for Women[(1),(2),(3)]
Sivakasi, India
E-mail:kodieswaripomman@gmail.com[(1)],rgeetaece@gmail.com[(2)]

***Abstract* - Performance changeability in an integrated circuit can basically affect parametric output in nanometer technology. As a result, variant tolerance is essential requirement for design. The efficient fault tolerance technique is implemented for improving the reliability of a circuit. In this paper, the fault can be tolerate for the combinational circuits by using MUX based self repair (MSR) logic. The Error Detection and Correction (EDC) circuit is modified by logic. The simultaneous error detection and correction done using multiplexer and inverter with reduction in cost, area and power. MSR logic aims to accomblish high accuracy in the output.**

Keywords: Error detection and correction, fault tolerance, MUX, MSR logic.

I. INTRODUCTION

Reliability with respect to soft errors has become a critical issue in digital circuits. Reliability of a circuit can be defined as its ability to function properly despite the existence of such errors. The selective transistor scaling method that protects individual sensitive transistors of a circuit. A sensitive transistor is a transistor whose soft error detection probability is relatively high. Gate level soft error reliability evaluation technique for combinational circuits is proposed that produces similar results as produced by transistor level simulation (using SPICE), but with orders of magnitude reduction in CPU time [1]. If a soft error occurs in the combinational logic, it will result in a Single Event Transient (SET). On the other hand, if it occurs in the memory cell itself, it will result in a Single Event Upset (SEU). Both SET and SEU have a major impact on circuit operation, and they should be treated properly. To reduce the simulation time, reliability evaluation techniques based on probabilistic gate models and stochastic computation have been proposed [2]. The number of injected fault is small. The number of iterations is T.

Quadded logic (QL) cannot correct the last one or two layer of the circuit. In contrast to QL, Quadded transistor (QT) corrects errors while performing the function of a circuit. QLQT has a better reliability than other fault tolerant techniques. The number of transistors in QT is half of QL and so is the area, whereas the delay in QLQT is slightly smaller than in QL. QLQT does not require additional transistors. The probability of having single errors in a short path is high. QL and QLQT are more reliable than Triple Modular Redundancy (TMR) technique. The fault-tolerant QT circuits correct faults that occur in the last two logic layers, hence leading to a better reliability [3].The reliability-driven software transformations targeting unreliable hardware. The goal is to lower the application's susceptibility toward failures. Compared to performance-optimized compilation, our method incurs 60% lower application failures, averaged over various fault injection scenarios and fault rates. To enhance the reliability of a fault susceptible system through software transformations that target reducing the critical instruction executions along with the spatial and temporal vulnerabilities [4].

A generalized modular redundancy scheme to enhance the reliability of combinational circuits is proposed. This method can achieve reliability figures higher than that of triple modular redundancy (TMR). Reliability estimation of combinational circuits can be achieved by measuring their failure rates. Failure rate is the percentage of which a circuit will produce faulty output when a fault is injected in the logic. This way, reliability of a circuit is reciprocally proportional to its failure rate [5]. The finite state machine (FSM) based fault tolerance technique for sequential circuits. This technique is based on adding redundant equivalent states to protect few states with high probability of occurrence. Triple Modular Redundancy (TMR) is one of the well known techniques to reduce the impact of soft errors in combinational logic. 90% state probability coverage protection achieves the lowest failure rates for most of the circuits among all compared techniques. The increase in the number of faults injected has exponential relation with the increase in the failure rate. A new static fault tolerant method called quad-gate-transistor,

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 23, December 2017

which uses quadded-transistor output logic with gate level quad implementation of the given circuitry to make the system
defect tolerant. Such combination of gate and transistor level redundancy provides significantly higher reliability over classical triple modular redundancy. If any fault occurs at the last or last but one level, the system fails. However, when outputs from last level gates of QL is connected to inputs of QT, any single error occurring at last level of QL is absorbed in the QT structure [7].

Categorizing state-of-the-art techniques at the hardware-level, software-level and application-level. It focused towards higher levels of abstraction to increase and optimize for reliability. The device through Hardware Architecture, System Software, Compiler and Application should be covered since all layers can potentially contribute to increase the reliability. The first part of the paper gave an overview of the currently most prominent reliability concerns like variability, aging, temperature effects and soft errors. The second part provided (a certainly not comprehensive) state-of-the-art of techniques at hardware-level, software-level and application level. The third part provided our perspectives obtained through larger-scale ongoing projects on reliability where the authors from industry and academia are involved in. Our perspectives reach from already practiced techniques like exploiting cross-layer techniques to visionary ones like future on-chip systems will evolve into complex Cyber-physical Systems-on-Chip [8]. The investigates limitations of conventional sizing methods and introduces new techniques for mitigating soft errors in nanometer circuits. Our techniques employ two algorithms. The first algorithm is called soft error rate saturation consideration algorithm. This algorithm prevents a gate from being oversized and thus, it limits the soft error rate of the circuit. The second algorithm, called weighted area distribution algorithm, can fairly distribute area overhead to the most sensitive gates [9]. Conventional memory structures such as caches and main memories are well protected using the Error Correcting Code (ECC). The first technique, upsizing parallel networks based on fault-sensitivity without weighted area overhead, equally distributes the additional area to parallel networks in sensitive gates. This method offers up to 20% reduction of soft error rate [10]. The sizing technique featuring upsizing all transistors either in a circuit or in selected sensitive gates may not be a good choice for handling soft errors in nanometer circuits.

II.QUADDED LOGIC WITH QUADDED TRANSISTOR

Fault-tolerant techniques using hardware redundancy have been extensively investigated for improving reliability. Quadded logic (QL) is an interwoven redundant logic technique that corrects errors by switching them from critical to subcritical status; however, QL cannot correct errors in the last one or two layers of a circuit. In contrast to QL, quadded transistor (QT) corrects errors while performing the function of a circuit. In this brief, a technique that combines QL with QT is proposed to take advantage of both techniques. The proposed quadded logic with quadded transistor (QLQT) technique is evaluated and compared with other fault-tolerant techniques, such as triple modular redundancy and triple interwoven redundancy, using stochastic computational models. Simulation results show that QLQT has a better reliability than the other fault-tolerant techniques (except in the very restrictive case of small circuits with low gate error rates and very short paths from primary inputs to primary outputs). These results provide a new insight for implementing efficient fault-tolerant techniques in the design of reliable circuits and systems.

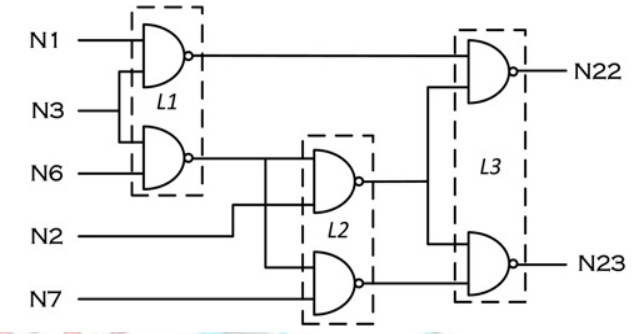

Fig.1.Logic diagram of QLQT

The measures for QLQT are similar, but slightly less than for QL due to the use of QTs in the last layer of the circuit. The number of transistors in QT is half of QL and so is the area (if transistor sizing is constant). Since circuit delay is dominated by the load capacitance, the delay in QL is at least twice as large as in the original circuit due to the fan-out of signals into two different gates, whereas the delay in QLQT is slightly smaller than in QL. This is due to the similar delays that the QTs incur as the original logic gates would have in the last layer. However, QLQT does not require additional transistors for the voters or arbiters that would be needed in a QL circuit. QL and QLQT are not very effective. Since the probability of having single errors in a short path is high, TMR and TIR could be viable. At a higher gate error rate, however, QL and QLQT are more reliable than TMR and TIR due to their better ability in handling multiple errors.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 23, December 2017

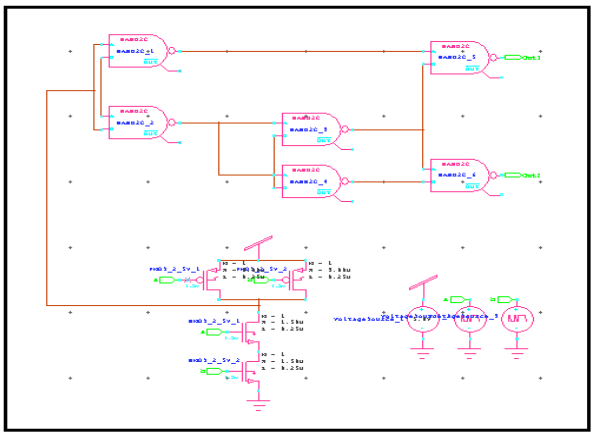

Fig.2.Implementation of QLQT in combinational circuit

In a large circuit with a high gate error rate, multiple faults are significantly better handled by QLQT than any of the other techniques, thus QLQT achieves the best reliability overall. Note that in QL, a single error in the four outputs is considered to be tolerable and is masked by the majority voting at the output. If all of the signals are required to be error-free to produce a correct output, the advantage of QLQT over QL becomes very significant.

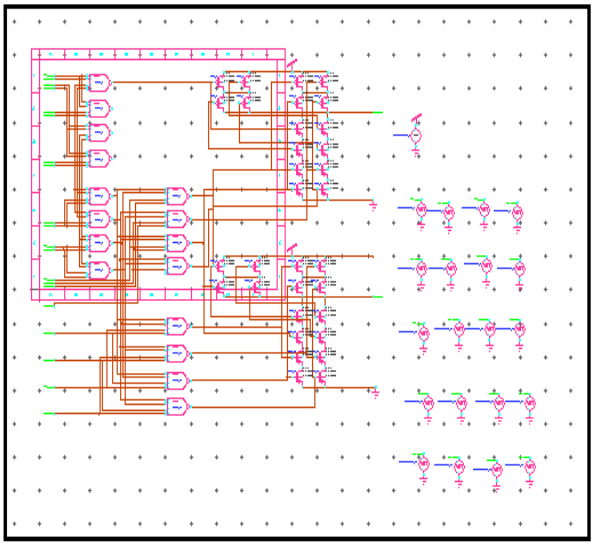

Fig.3.Schematic diagram of complex QLQT

III. PROPOSED WORK

The combinational circuit is a circuit in which we combine the different gates in the circuit, for example encoder, decoder, multiplexer and demultiplexer. The output of combinational circuit at any instant of time, depends only on the levels present at input terminals. The combinational circuit do not use any memory. The previous state of input does not have any effect on the present state of the circuit. A combinational circuit can have an n number of inputs and m number of outputs.

The XOR gate is acting as a comparator that produce a true output (1/HIGH) results when the input and the output were same, otherwise comparator (0/LOW). XOR express the equality and inequality function. XOR operation can be similar to an addition modulo 2 operation. Other uses of XOR operators are subtractions, comparators, and controlled inverters. XOR gate algebraic operations ($A.\bar{B}+\bar{A}.B$) where A and B are Inputs

In this project we present a new error detection and correction circuit that delivers fast response times with the use of a MUX and inverter. A multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. It has 2^n inputs and n select lines, which are used to select which input line to send to the output. MUX are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. MUX is also called a data selector. It can also be used to implement Boolean functions of multiple variables. MUX is a combinational logic circuit designed to switch one of several input lines through to a single common output line by the application of a control signal.

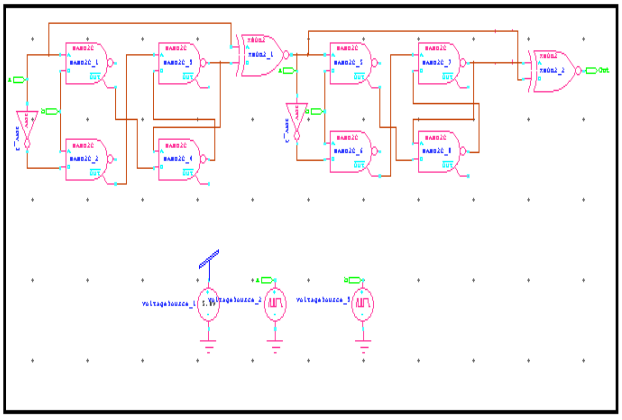

Fig.4.Logic diagram of MSR technique

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 23, December 2017

MUX is based on selection line. The XOR output is considered as the selected line of MUX and the MUX getting enable or disable. An inverter or NOT gate is a logic gate which implements logical negation. If the XOR output is high means the MUX get enable and send the inversion of flip flop output to the final output as CORRECT. If the XOR output is considered as the low means the MUX sends the main flip flop output to the final as CORRECT.

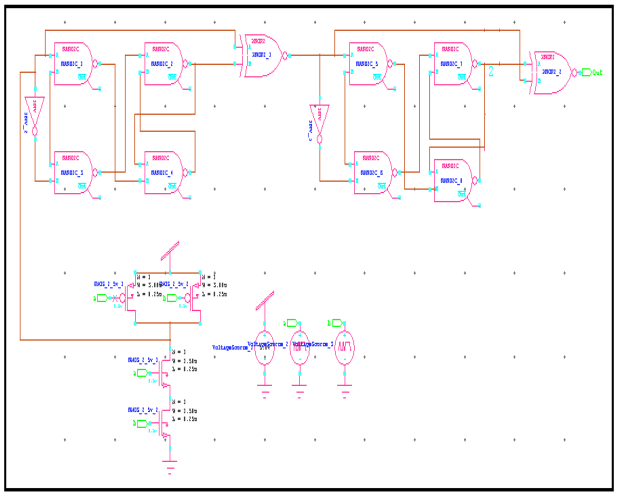

Fig.5.Implementation of MSR in combinational circuit

Fig 5 shows the implementation of MUX based Self Repair (MSR) logic in combinational circuit as a NAND gate. The faulty NAND gate is considered. In a PMOS input the fault is occurred, whereas the no connection is include. Hence the fault occurs at the NAND gate. This fault can be tolerate by using the error detection and correction circuit modified as MSR logic. The output of the combinational circuit is given as a input of the EDC circuit that provides the fault free combinational output.

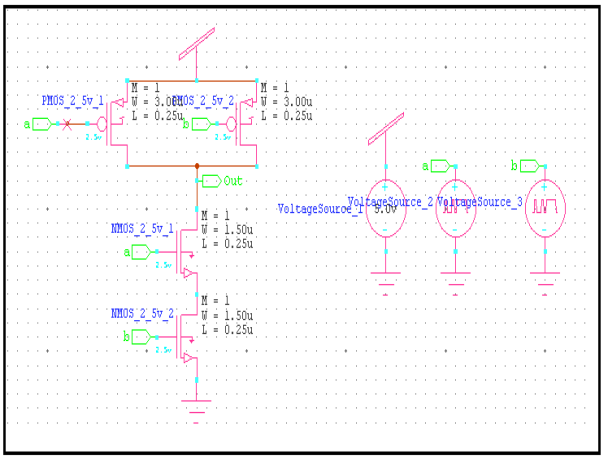

Fig.6.Schematic diagram of combinational circuit as a faulty NAND gate

IV.APPLICATION OF EDC

Error Detection and Correction circuit were implemented in the router circuit. A router is a device that forwards data packets in between two different networks. Routing is performed for public switched telephone network, electronic data networks and transportation networks. A data packet is typically forwarded from one router to another through the networks that constitute the internetwork until it reaches its destination node. When a node on one network needs to send a message to a node on another network, this packet will be picked up by the router and passed on to the other network. Many nodes are programmed with a so-called 'default gateway', which is the address of the router that is to take care of all packets not for other nodes on the same network. Home and small office networking are becoming popular by day by the use of IP wired and wireless router.

The routing was simulated, control the errors during the transmission in between the source to the destination. After the error correction the output was transmitted into the output as the CORRECT output. Wired and wireless router are able to maintain routing and configuration information in their routing table. They also provide the service of filtering traffic of incoming and outgoing packets based on IP address.

V.SIMULATION RESULTS AND ANALYSIS

The AND gate, XOR gate, latch is used. We have used the faster gate implementation using the library files. This requires a number of inputs and n number of outputs.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 23, December 2017

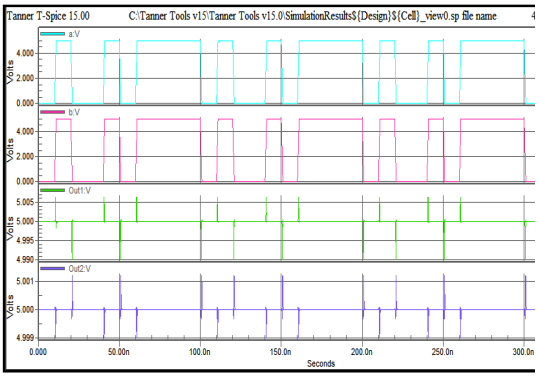

Fig.7.Simulation output of QLQT technique with combinational circuit

Fig.7 shows the simulation output of QLQT technique with combinational circuit. Which have the low accuracy output. The power consumption is high when compared to MSR logic.

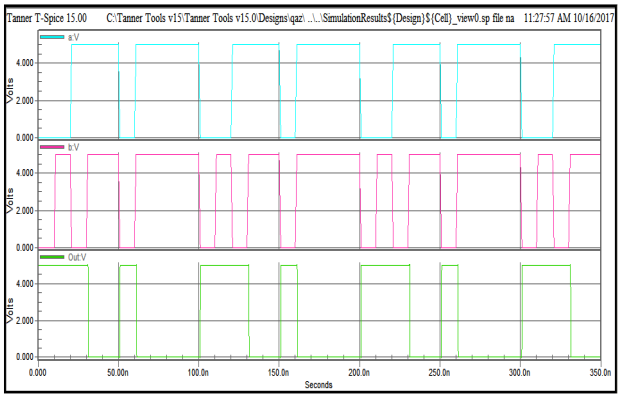

Fig.8.Simulation output of MSR logic with combinational circuit

Fig.8 shows the Simulation output of MSR logic with combinational circuit. Which has the high accuracy output. The power consumption is low. MSR uses the Error Detection and Correction(EDC) circuit were implemented in the router circuit. A router is a device that forwards data packets in between two different networks. Routing is performed for public switched telephone network, electronic data networks and transportation networks.

The error was detected by the comparator, comparator output was acting as a selection line for enabling/ disabling the latch. XOR express the equality and inequality function. XOR operation can be similar to an addition modulo 2 operation. Other uses of XOR operators are subtractions, comparators, and controlled inverters. XOR gate algebraic operations ($A.\bar{B}+\bar{A}.B$) where A and B are Inputs. A Second comparator compares and produce the final output as a corrective. Control line is used to control the error occurrence during the transmission.

DESIGN	POWER (kw)
QLQT technique	1.058757e^-003
QLQT technique with NAND gate	4.602692e^-003
MSR technique	1.749108e^-003
Faulty NAND gate	4.07438e^-003
MSR technique with NAND gate	1.772534e^-003

Table.1.Power comparison of existing and proposed method

The error detection and correction of multiplexer based self repair logic. This requires n number of inputs and n number of outputs. The error was detected by the comparator, comparator output was acting as a selection line for enabling/ disabling the MUX. A multiplexer 2*n* inputs have *n* select lines and send selected inputs into the output. If an error is occurring means MUX get enable and transmit the input to output after the inversion. [6] proposed a novel method for secure transportation of railway systems has been proposed in this project. In existing methods, most of the methods are manual resulting in a lot of human errors. This project proposes a system which can be controlled automatically without any outside help. This project has a model concerning two train sections and a gate section. The railway sections are used to show the movement of trains and a gate section is used to show the happenings in the railway crossings. The scope of this project is to monitor the train sections to prevent collisions between two trains or between humans and trains and to avoid accidents in the railway crossings. Also an additional approach towards effective power utilization has been discussed. Five topics are discussed in this project : 1) Detection of obstacles in front of the train;2) Detection of cracks and movements in the tracks;3) Detection of human presence inside the train and controlling the electrical devices accordingly 4) Updating the location of train and sharing it with other trains automatically 5) Controlling the gate section

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 23, December 2017

during railway crossing. This project can be used to avoid accidents in the railway tracks.

The delay occurrence during the transmission from the source or input to the destination or output. The delay is indicated by XOR. Some delay were occurred during the transmission that was said to be as error. The control output is used to detect the errors, correct output is used to correct the error and produce the output by using the modified technique MSR (Multiplexer Based Self Repair) logic. After the error correction the output was transmitted into the output as the correct output.

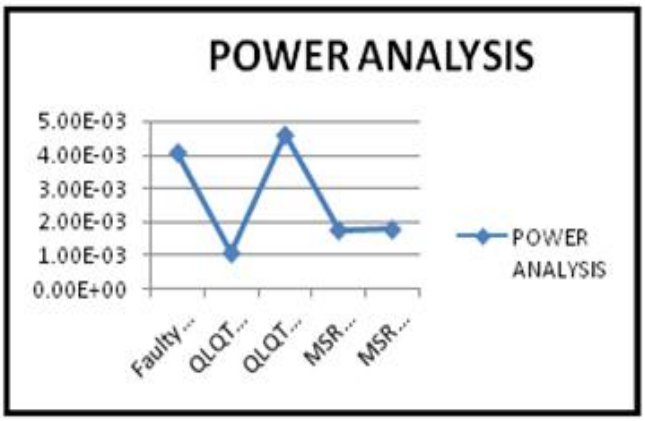

Fig.9.Power comparison graph

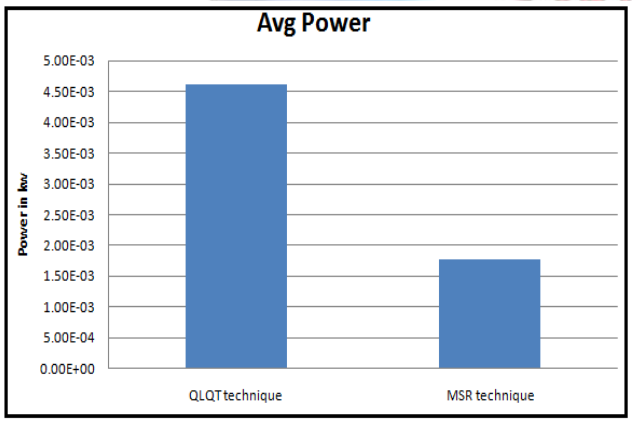

Fig.10.Comparison of average power consumption

VI.CONCLUSION

In this paper, a detecting and correcting concurrent fault and soft errors are presented. It uses minimum hardware overhead logic circuits to detect the erroneous responses at the outputs of the functional circuit being monitored. The earlier error detection and correction method provides error correction as non accurate. The adopted MSR approach can deliver very fast detection times compared to the techniques presented earlier in the literature. It exploits a new MSR logic which provides the ability to detect and correct multiple errors during the communication or transmission of information. The EDC circuit will be implemented in the router application. The MSR logic import accurate output with reduction in component and time consuming.

VII.REFERENCE

[1] Ahmad T.Sheikh, Aiman H.El-Maleh, Muhammad E.S.Elrabaa, and Sadiq M.Sait,"A Fault Tolerance Technique for Combinational Circuits Based on Selective-Transistor Redundancy" IEEE transactions on very large scale integration (vlsi) systems 1063-8210 © 2016 IEEE.

[2] A.H.El-Maleh and K.A.K.Daud, "Simulation-based method for synthesizing soft error tolerant combinational circuits," *IEEE Trans. Rel.*,vol. 64, no. 3, pp. 935–948, Sep. 2015.

[3] J. Han, E. Leung, L. Liu, and F. Lombardi, "A fault-tolerant technique using quadded logic and quadded transistors," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 8, pp. 1562–1566, Aug. 2015.

[4] S. Rehman, F. Kriebel, M. Shafique, and J. Henkel, "Reliabilitydriven software transformations for unreliable hardware," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 33, no. 11,pp. 1597–1610, Nov.2014.

[5] A.H.El-Maleh and F.C.Oughali, "A generalized modular redundancy scheme for enhancing fault tolerance of combinational circuits," *Microelectron. Rel.*, vol. 54, no. 1, pp. 316–326, 2014.

[6] Christo Ananth, K.Nagarajan, Vinod Kumar.V., "A SMART APPROACH FOR SECURE CONTROL OF RAILWAY TRANSPORTATION SYSTEMS", International Journal of Pure and Applied Mathematics, Volume 117, Issue 15, 2017, (1215-1221).

[7] A.Mukherjee and A.S.Dhar, "Fault tolerant architecture design using quad-gate-transistor redundancy," *IET Circuits, Devices Syst.*, vol. 9, pp. 152–160, May 2015.

[8] J. Henkel *et al.*, "Reliable on-chip systems in the nano-era: Lessons learnt and future trends," in *Proc. 50th ACM/EDAC/IEEE Annu. Design Autom. Conf. (DAC)*, May/Jun. 2013, pp. 1–10.

[9] W. Sootkaneung and K. K. Saluja, "Soft error reduction through gate input dependent weighted sizing in combinational circuits," in *Proc. 12th Int. Symp. Quality Electron. Design (ISQED)*, Mar. 2011, pp. 1–8.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 23, December 2017

[10] W. Sootkaneung and K. K. Saluja, "On techniques for handling soft errors in digital circuits," in *Proc. IEEE Int. Test Conf. (ITC)*, Nov. 2010, pp. 1–9.