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Analysis of Low Power CMOS Dual Edge Triggered Flip-Flops Using Multiple C-Elements

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Abstract - **Flip-Flops are the important elements in all digital design but, consume much power due to the dynamic and static power dissipation. This paper presents a low power Conditional Discharge Flip Flop, Static Pulsed Latch Flip Flop with comparison of existing DET FF using Multiple C-Elements. The FFs are used to reduce the power consumption and delay. In order to reduce power consumption C-Element technique is introduced. The CD_CFF and SPL_CFF are designed to implement in a 2to1 MUX and the simulation has been performed on the Tanner EDA Tool. Novel CMOS DET Flip-flops are compared to existing DET flip-flop using simulation in a high performance CMOS technology and are shown to have superior characteristics such as power and power delay product(PDP) for a range of switching activities.**

Keywords: Low power, Dual Edge Triggered Flip flop, CMOS, CD_CFF, SPL_CFF.

I. INTRODUCTION

Power dissipation and consumption is a serious problem in an IC. The four important components involve of power dissipation in integrated circuits.

$P_{Total}=\alpha C_L V_{DD}^2 f_{olk} + V_{DD} (Isc_+ I_{st} + I_{leakage})$.

P_{Total} is the total power dissipation. $\alpha C_L V_{DD}^2 f_{clk}$ refers to the power dissipation due to switching activities. Where C_L is the load capacitance, f_{clk} is the clock frequency and α denotes the node transition factor. $V_{DD}*I_{sc}$ Refers to the short circuit power and $V_{DD}*I_{st}$ refers to the Static power dissipation. So while designing an IC, delay, area and transistor count has comes under the primary design goal. In VLSI most of the power is dissipated by Flip Flops (FF's). Flip Flops are used as the memory elements which are the basic building blocks of an IC. They are used in many applications such as data storage, counters, frequency division and shift registers etc. The purpose of this paper is to reduce delay, power consumption, and noise.

CMOS DUAL EDGE triggered (DET) flip-flops achieve the same data rate as single edge triggered (SET) flip-flop at half the clock frequency, It is lead to reduced power dissipation of synchronous logic circuits[1], To avoid clock overlap hazards DET flip-flop (DET-FF) with a true-single phase clock. Reduce the leakage power consumption. More logic circuits are failure inside the circuits [2]. To reduced delay Design of Domino Logic Gates. It is high performance. Circuit is more critical [3]. Static timing analysis will provide more accurate the Timing Characteristics of Flip-Flops. It is high-performance, reliable and economically feasible circuits. It is improved power consumption. [4] To determine the optimal size of the flip-flop transistors. Statistical design of the flip-flops circuits is achieve a high yield, time efficiency [5]. The designed to understanding the Effect of process variations on the delay. Designs are Static and Domino logic gates. [6] The design nanometer flip-flops in the energy-delay space. Design nanometer flip-flops are reduced the size of the design space. It is efficiently reduces the number of clocked transistors [8]. The cost of this reduction is higher circuit complexity of DET flip-flops which usually have more transistors and more internal nodes than SET [9].The design of reduce circuit size compared to SET FF [10]. The cost is reduction is higher circuit complexity of DET flip-flops which usually have more transistors and more internal nodes than SET flip-flops [11].In

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section II we review basic operation of C-Element. In section III we review existing low power DET FF's. In section IV we review proposed low power CMOS DET FF's. In section V the power and performance characteristics are shown compared to other FF's. In section VI Implementations results in MUX. Finally Section VII concludes this paper.

II.BASIC OPERATION OF C-ELEMENT

A C-element is normally a three-terminal device with two inputs and one output. When all of its inputs are same the output switches to the value of the inputs; when the inputs are not same, the previous output value is preserved. Although both inverting and non-inverting C-elements can be used for the proposed DET flip-flop, only the inverting topology shown in Fig. 1 is used due to the transistor-level implementations being faster in the inverting configuration. Other implementations have been considered but have not been found to improve on performance, power, or circuit size when compared to the implementations. C-elements can be used in Finite state machines (FSMs) and in the designing of the Flip-flops and Latches. The C-element has different structures which gives the same operation, in this paper we use weak feedback of the C-elements as

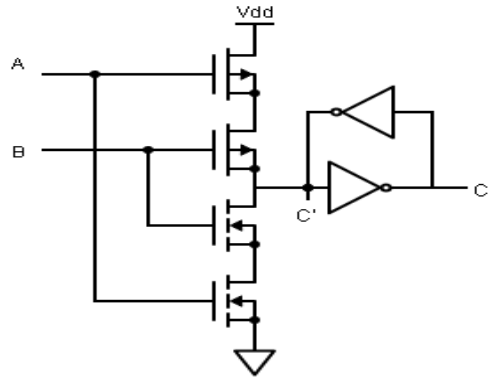

Fig.1.Schematic of Weak feedback C-element

III.EXISTING WORK

In this section we analyze the problems of previously described Flip Flops.

A. Low glitch-power DET LG_C Flip-Flop

Fig.2 shows a typical circuit of low glitch power LG-C DET Flip-Flop. This FF consists of three C- Elements. LG_C FF can be designed using both inverting and non-inverting configuration of C-elements can be used for the proposed DET flip-flop, the inverting topology is of C-element as it is having less delay compared to non-inverting topology of C-element. In this flip-flop D and CK are two inputs, A and B are the two internal nodes and Q is the output. C-elements are used to reduce switching activity. The value of D only determines which signal level latches A and B switch to at the next clock transition. LG_C's internal state only changes once with the first signal change at the input. This FF designs are much low power dissipation in the presence of glitches at the flip-flop inputs. In which results the output C-element switching Q to D.

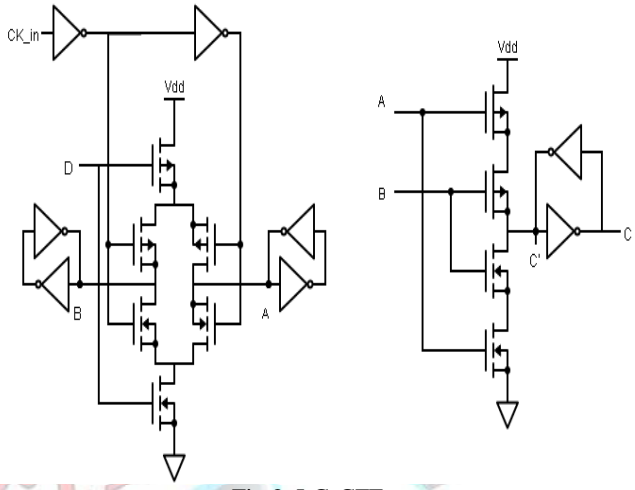

Fig.2. LG-CFF

B. Implicit Pulsed DET IP_C Flip-Flop

Fig.2 shows Implicit-Pulsed IP_C Flip-Flop is two additional weak C-elements are merged with the two input C-elements by sharing clocked transistors.

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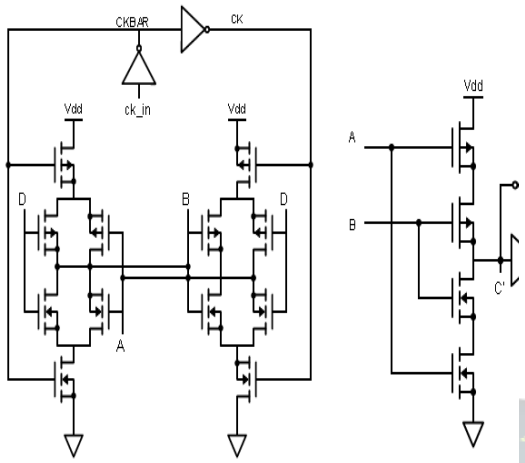

Fig.3. IP-CFF

LG_C can be modified to reduce the total dynamic power dissipation due to the latches that are present at the node A and B. (Latches mean the back to back connection of inverters).The IP_C design over the LG_C design is reduced delays and reduced switching power dissipation. This flip-flop design has no weak feedback to overpower. The output Q switches to D after every clock transition when both A and B are equal to Qbar.

C. Floating Node DET FN_C Flip-Flop

Fig.4 shows Floating Node FN_C flip flop (FN_CFF). It is simulated signal levels for one clock transition. Initially in the simulation, Q is "0," CK is "1," and D is "0," Since D is equal to CK bar, B is kept at "1" with a result, node A is floating. Due to the switching of parasitic capacitances, the voltage level at node A is slightly higher than the *V*DD voltage of 0.85 V. Before the next clock edge, input D switches to "1." Node A is floating again and B is kept at "0," which ensures that Q stays at "1" in the new cycle. [7] proposed a novel method for secure transportation of railway systems has been proposed in this project. In existing methods, most of the methods are manual resulting in a lot of human errors. This project proposes a system which can be controlled automatically without any outside help. This project has a model concerning two train sections and a gate section. The railway sections are used to show the movement of trains and a gate section is used to show the happenings in the railway crossings. The scope of this project is to monitor the train sections to prevent collisions between two trains or between humans and trains and to avoid accidents in the railway crossings. Also an additional approach towards effective power utilization has been discussed. Five topics are discussed in this project : 1) Detection of obstacles in front of the train;2) Detection of cracks and movements in the tracks;3) Detection of human presence inside the train and controlling the electrical devices accordingly 4) Updating the location of train and sharing it with other trains automatically 5) Controlling the gate section during railway crossing. This project can be used to avoid accidents in the railway tracks.

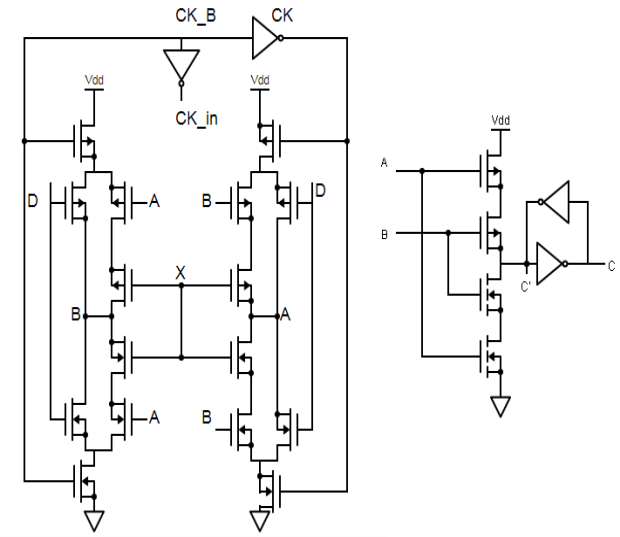

Fig.4.FN_CFF

In this example, the combinations of D and CK are such that only node A is seen floating. If either D or CK were inverted, node B is a floating node. Because of the switching of parasitic capacitances before floating node events, floating voltage levels at A and B can stay above the *V*DD voltage of 0.85 V or below 0 V. Analog simulations indicate that the increase above *V*DD and the decrease below 0 V do not exceed 10% of the nominal *V*DD and that no significant dynamic current is flowing through the transistors' channels during this time. Thus, floating node events do not affect circuit reliability. In this circuit, is only surveyed flip _flops that have both low power and delay is high. The FN_C's glitch energies are lower than that of LG_C due to the absence of static latches at nodes A and B. FN_C is high due to switching at one of A or B, yet the energies of subsequent glitches in the same cycle are considerably lower due to the flip-flops' internal states staying unchanged.

D. Conditional-Toggle CT_C And CTF_C Flip-Flop

Fig.5 and 6 shows Conditional-Toggle CT_C and CTF_C FF circuit uses only 20 transistors for input, output and clock buffering. The number of transistors in the FN_C flip-flop are more , if we reduce the transistor count and obtain the same operation of the DET Flip flop, High performance can achieved. The FN-C flip-flop is modified to CT_CFF. The flip

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flop inputs D the signal that mirrors and the Q in between the clock transitions. When D and output Q are equal, the signal level at X is kept at Qbar by weak C-element, when D and Q are not equal to X 1 kept at Qbar by using the latch.

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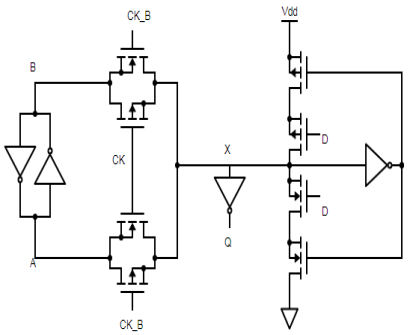

Fig.4.CT_CFF

The back to back connection of inverters and 2to1 MUX with its output connected to X at a latch part. But this latch part consumes high power so CT_CFF is modified to CTF_C flip flop. The transistor level implementation of CTF_C is as shown in the fig.5

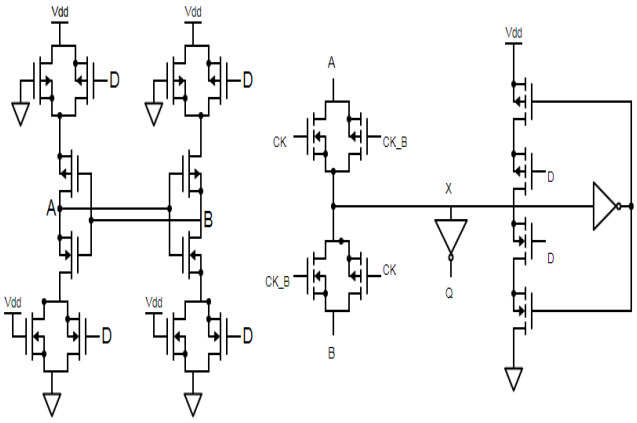

Fig.5.CTF_CFF

CTF_ CFF Operations are same as CT_C flip-flop. This flip flop is having high performance in term of switching speed and power consumption when compared to the CT_C flip flop.

IV. PROPOSED WORK

A. CONDITIONAL DISCHARGE FLIP-FLOP

Fig.7 shows a new flip-flop is introduced: the conditional discharge flip-flop (CD_CFF). It is based on a new technology, known as the conditional discharge technology.
This CD_CFF not only reduces the internal switching activities, but also generates less glitch at the output, while maintaining the negative setup time and small D-to-Q delay characteristics. The Conditional discharge scheme is employed in the CD_C Flip-flips reduce the redundant switch power.
CD_CFF consists of two stages. The first stage captures LOW to HIGH transition. The second stage captures HIGH to LOW transition. If the input D is high in the sampling window, the internal node X is discharged assuming that were initially (LOW, HIGH) for the discharge path to be enabled. Then the output node will be charged to HIGH. Control of discharge path is achieved by inserting an NMOS transistor in the discharge path of high switching activity stage.

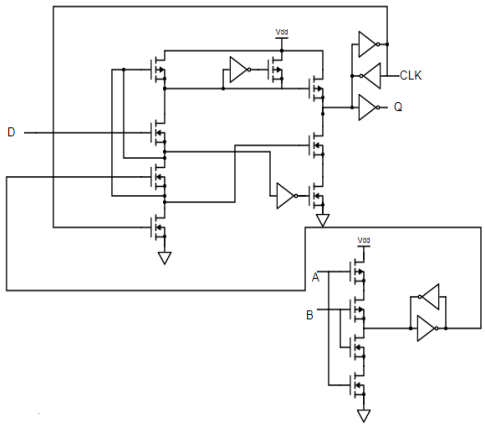

Fig.7.CD-CFF

The output is Q become HIGH and Qb become LOW. The input makes a low to high transition. This output transition switches off the first stage discharge path and thus, preventing it from discharge or further evaluating the next clock cycles as long as the input is 1.

B.STATIC PULSED LATCH-C FLIP-FLOP:

Fig.8 shows a new flip-flop is introduced: the static pulsed latch flip-flop (SPL_CFF). It is based on a new technology, known as the Static pulsed latch _C Flip-flop technology.
The SPL exhibits the lowest average delay and the minimum D-Q delay variation1. Such advantage of the SPL FF is mainly due to the simplicity of its data-to-output path, as occurs in all Explicit Pulsed (EP) flip-flops. This greater simplicity translates into compact layout that reduces both the wire capacitance and hence the transistor sizes for a given performance.

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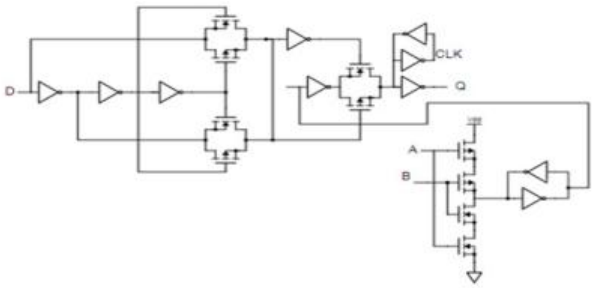

Fig.8.SPL-CFF

SPL are very close to TGLM in terms of both average delay and variations, and their differences are much smaller than for the CK-Q delay. This design is the low energy targets. SPL becomes as fast as TGLM, although with slightly lower average delay and wider variations.

V.SIMULATION RESULTS AND COMPARISON OF CMOS DET FLIP-FLOPS

The flip-flops presented in this paper were simulated and power and delay of these flip-flops were calculated in 45 CMOS technology with the help of tanner tool. The CD_CFF and SPL_CFF are the previously exiting designs which are compared with designs presented in this paper.

Simulation results of extensive Monte Carlo, glitch energy, and leakage simulations. All flip-flops operated correctly in all Monte Carlo simulation points. The figure of merit in this comparison is the power-delay product at 50% switching activity. For this metric and also for the new glitch energy metrics, results of the best performing flip-flops are highlighted. The two best DET flip-flops are the novel CD_CFF and SPL_C flip-flops. This design has the lowest glitch energies, and the lowest leakage of all the surveyed flip-flops. The design achieves the lowest PDP values at high switching activities compared to the common LM flip-flop.

VI.IMPLEMENTATION RESULTS

Implementation of CMOS DET Flip-Flop contains five important blocks such as Data input, clock signal, transistor block, C-elements and 2to1mux. The block diagram of Conditional Discharge Flip-Flop is shown in fig.9.

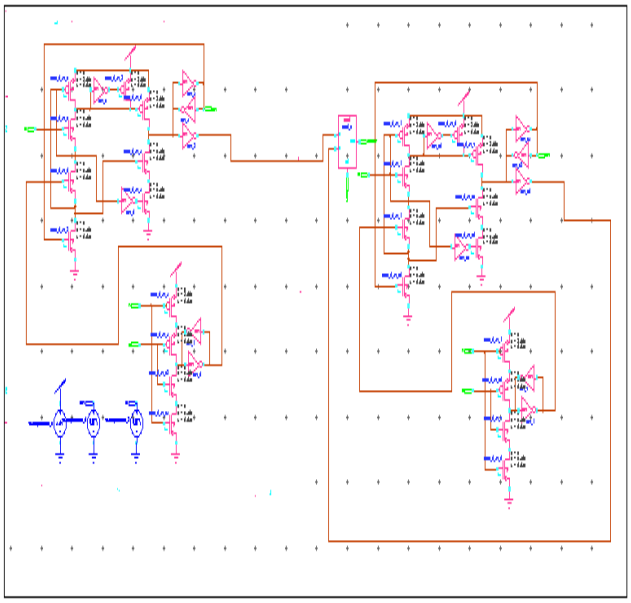

Fig 9: Implementation of Conditional Discharge FF in 2to1 Mux.

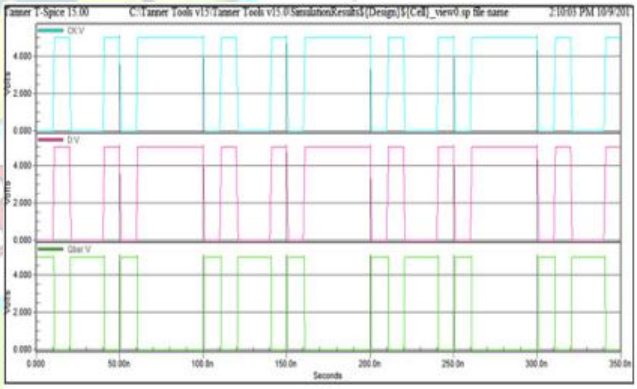

Fig10: Simulation output of Conditional Discharge FF in 2to1 Mux.

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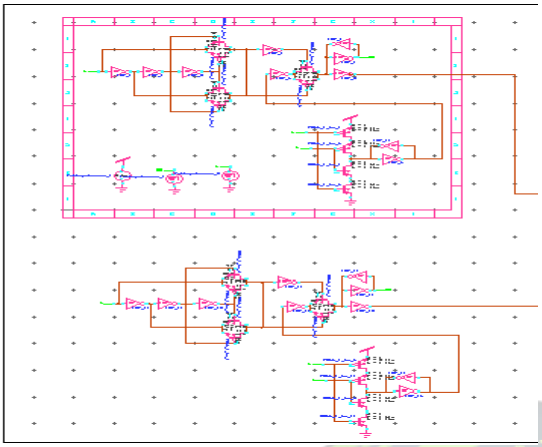

Fig 11: Implementation of Static Pulsed Latch FF in 2to1 Mux.

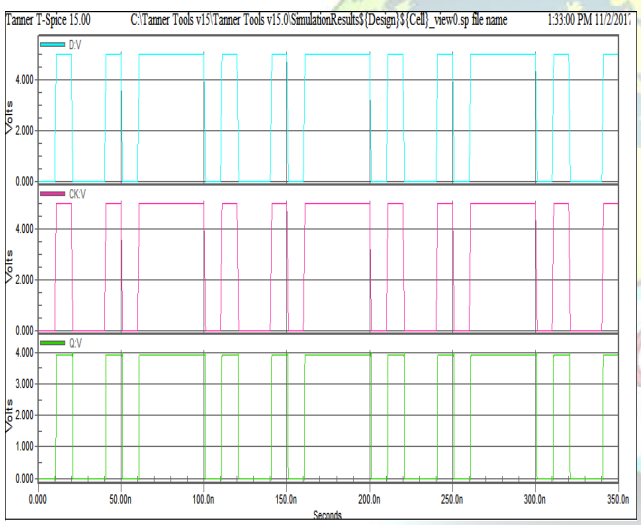

Fig12: Simulation output of Static Pulsed Latch FF in 2to1 Mux.

POWER ANALYSIS OF VARIOUS FLIP-FLOPS

DET FLIP-FLOPS	POWER(kw)
LG_C DET FF	0.003847
IP_C DET FF	0.004166
FN_C DET FF	0.004598
CT_C DET FF	0.008628
CTF_C DET FF	0.001468
CD_C DET FF	0.000961
SPL_C DET FF	0.000797

Table1: comparative analysis of power consumption

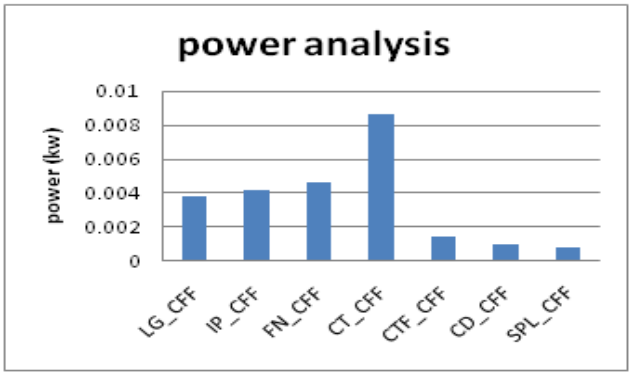

Fig.9.Plot of the power analysis for novel CMOS DET FF

VII.CONCLUSION

An extremely low-power FF, CD_CFF and SPL_CFF based CMOS DET FF is proposed. The new designs were compared to previous DET Flip-flop using simulation in the 40 nm CMOS technology. The novel CD_C and SPL_C designs can be used in high performance as they were found to have superior power and power delay products during periods of high switching activity. This flip-flop has the lowest Power dissipation in almost all range of the data activity Compared with other low-power FF's. C-Element based FF has the power reduction up to 70%. Extensive Monte Carlo simulations were carried out to demonstrate that the novel flip-flops are robust under process variations. The power reduction of CD_C and SPL_C based FF almost equal. Finally the designs are implemented in MUX.

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