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DESIGN OF T LATCHES BASED ON REVERSIBLE QUANTUM DOT CELLULAR AUTOMATA

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***Abstract*— — In this paper, sequential circuits have been designed which are based on reversible quantum dot cellular automata. The proposed designs have property of quantum dot cellular automata with essence of reversible logic. Each reversible logic gate is of computational complexity and distinctive type, so it will have a dissimilar delay and quantum cost. Computational complexity of reversible gate can be represented by its delay, quantum cost. Thus, primary objective of this article is design efficient latches in term of garbage outputs, quantum cost, and delay. The various efficient reversible latches including the positive level triggered D latch, negative level triggered D latch, T latch have been designed.**

Keywords— Quantum dot cellular automata; Reversible quantum dot cellular automata gate; Feynman gate; Latch.

I. INTRODUCTION

Harvest prospect of almost energy free computation is crucial inspiration of reversible logic circuit analysis. In VLSI design, the most important factor is power dissipation. For every bit of information loss, it dissipates heat in an order of $kBT\ ln2$ Joules; where kB is Boltzmann constant, T is operating temperature [2]. Bennett proved that if the computation is carried out in reversible way, $kBT\ ln2$ energy dissipation will not take place due to information loss [3].Reversible circuits are a special type of circuit that does not lose any information. A gate is called reversible if its function computes as bijective in manner. A reversible logic gate is a $K \times K$ gate, if it has k inputs and k outputs with one to one mapping between input and output vector, and vice versa. Number of garbage outputs, Quantum cost, and delay are essential cost metrics in reversible circuits. Garbage outputs cannot be utilized as reversible logic circuit's outputs, used to preserve reversibility characteristic but don't accomplish necessary actions. In strategy of the reversible circuits, the exploration was initially restricted to design of the combinational logic circuits, as feedback can't be allowed in the reversible computing, which was simply a convention.

Yet, in the research article, [4] has also proved that the feedback can permissible in the reversible computing. Consistent with this paper, a sequential arrangement is reversible if its combinational part is reversible (i.e., the combinational system is acquired with removing delay elements; thus breaks the conforming arcs).Moreover, this is also revealed that the reversible finite automata can be formed with its transition functions' reversible realization and can be used as a combinational part of anticipated sequential circuit. First design the reversible sequential circuit was accomplished using the same concept [5]. Here the proposed reversible sequential was reversible JK latch in which have feedback loop from the output. Also researcher has disproved the assertion that reversible sequential circuits can't reversible in behaviour. In current literatures on proposal of the reversible sequential circuit design, major metric of optimization is reversible gate count [6]-[10]. The quantity of reversible gates can't be decent cost metric for complexity analyze as every reversible gates may have different computational complexities and types; also each reversible gates may has different delay, quantum costs [11]. Innovative approach of reversible latches design are introduced in this proposed article that diminish delay, number of garbage outputs, quantum cost; and the designs are more optimal likened to pre-existing latches.

There are various emergent nano-technologies, such as superconductor flux logic family, and optical computing, quantum-dot cellular automata computing, etc., where dissipated energy because of information ruin will be very important factor of overall heat extravagance of the circuit [12]-[13]. Depending on the positions of the electron, QCA provides an alternative way of computation [14]. Quantum dot cellular automata (QCA) exhibit small feature size, extreme low-power dealing and high clock frequency, [15]-[16]. Thus, the propound methodology of reversible latches design have been implemented in molecular QCA framework.

This literature is organized as follows: basic of QCA computing, reversible quantum dot cellular automata and related work are appeared in Section II. Section III presents design of several types of latches based on reversible quantum dot cellular automata gate. Section IV presents Implementation and simulation results of the proposed latches in QCA framework. Finally, conclusion and future aspects is reported in section V.

II. BACKGROUND

A. *Basics of Multilayer QCA computing*

Schematic diagram of molecular QCA cell is demonstrated in Fig. 1(a). There are two free electrons, positioned at the corners of molecular QCA cell which is constructed with four quantum dots [17]. The electrons can reside corners of the molecular QCA cell because of coulombic interaction, resulting in either P = +1 (logic 1) or P = -1 (logic 0) where p is polarization, as displayed in Fig. 1(b).

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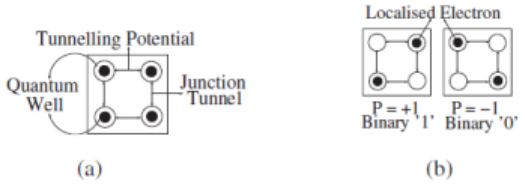

Fig. 1: (a) Structure of molecular QCA cell (b) Two different polarization of molecular QCA cell

The synchronization in molecular QCA is obtained by cascaded clocking of 4 discrete stage, as demonstrated in Fig. 2(a). The basic structure of molecular QCA circuit can be realized with wire crossing, NOT gate, and majority voter. The majority voter is demonstrated in Fig. 2(b). Basic gates like AND gate, OR gate can be realized using fixed polarization (+1 or -1) of one input of the majority voter, are shown in Fig .3.

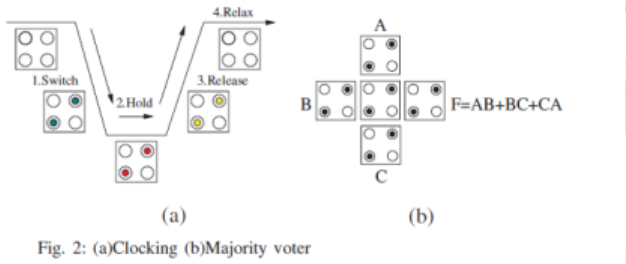

Fig. 2: (a)Clocking (b)Majority voter

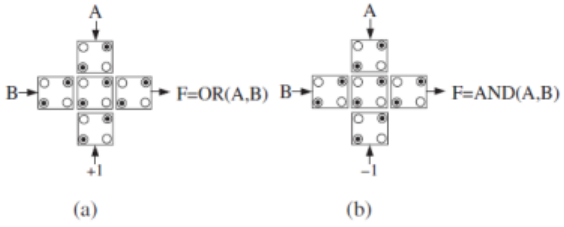

Fig. 3: Different types of gate realization. (a) OR gate. (b) AND gate.

B. Related Work

An operation R is called reversible if there is neither change in entropy nor energy to heat conversion due to the operation R. This adiabatic operation becomes very popular in this current time. Explicit analysis of the reversible gates are reported in [18]. Design of reversible sequential circuit had been reported first in [5], where reversible JK latch design was handled. Afterwards, reversible RS latch design had been reported in [19]. Double reversible NOR gates which was placed like cross-coupled, which were used for legitimate logic for RS latch design. In nature the architecture was without clock, no enable signal was there. The Fredkin gate had been used to design NOR gates. The proceeding was restricted to design reversible RS latch exclusively. Various reversible latches (i.e. T latch, D latch), including theirs corresponding flip-flops were designed in [6]. Implementations of the sequential circuits were costly as every non reversible gate had been mapped to their analogous reversible counterpart. Design of the reversible RS latch which avoid fan-out problem of [19] was reported in [8]. Main focus of this paper was reversible RS-latch. Several latches had been introduced as sub-units from the RS latch as segment of the master-slave flip-flops. The reversible flip flops and latches were designed in [9]. This design of sequential circuits were better than designs which were reported in [8] in the term of number of garbage outputs and gates count.

Reversible gates implemented with transistor were shown in [20] where the design of reversible RS latch had been detailed analyzed. Different types of reversible sequential circuits were reported in [6], [21], [22].

Reversible sequential circuit in QCA framework was introduced recently in [23]-[24]. These designs are better than other. Though testable feature have been introduced here but the designs of the sequential circuit is not cost effective. The proposed article overcomes these pitfalls. With favour of this proposed article on the reversible latches in QCA framework, several attractive contributions in which designs are optimized respect to variant cost metrics like quantum cost, garbage output, delay and cell count are provided.

C. Reversible Quantum Dot Cellular Automata

The reversible structure in QCA is known as reversible quantum dot cellular automata (RQCA) gate [24]. Mapping of the input to output in RQCA structure as follows: P=A, $Q = A \oplus B \oplus C$, R=A'B+ AC, where inputs are A, B, and C and outputs are P, Q, and R. Block diagram of the RQCA gate is shown in Fig. 4(a). It is 3 × 3 reversible gate having low quantum cost (QC) which is equal to 4. There are very few reversible gates which have such minimal QC. 4 NOT gates and 6 MVs gates are required to build the RQCA gate. The design, with cell count = 194, covers area = 0.21 $\mu m2$. As 5 clock zones are used to build it, input to output delay = 1.25 clock cycles. This should be remembered that the fan-out can't be permitted in the reversible logic, but is permit in low power QCA [23]. Feynman gate is used to overcome reversible circuit's fan-out problem. Feynman gate is displayed in Fig. 4(b)

Fig. 4: Block diagram of different Reversible Gates. (a) reversible quantum dot cellular automata (RQCA) gate. (b) Feynman gate

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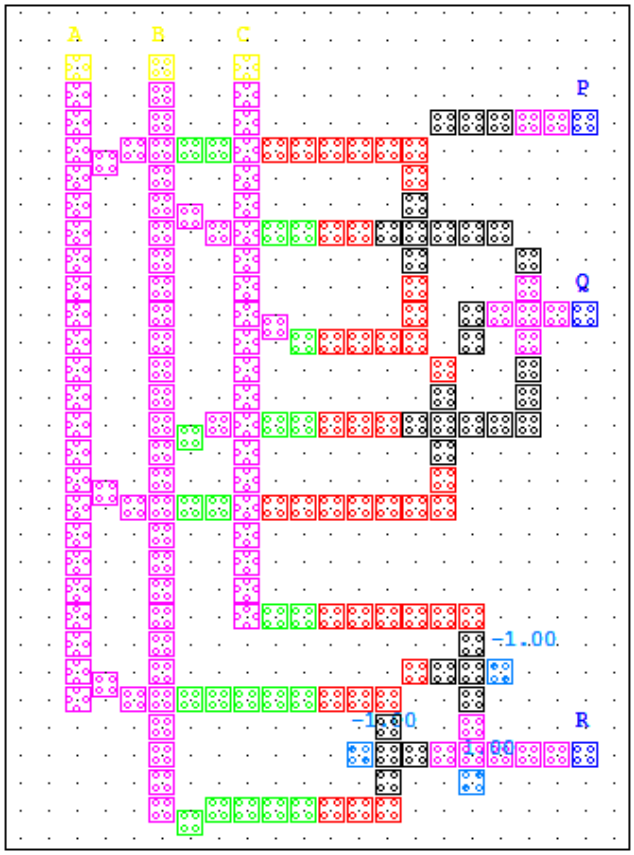

Fig 5: cell layout of RQCA gate

III. DESIGN OF LATCHES BASED ON REVERSIBLE QUANTUM DOT CELLULAR AUTOMATA GATE

RQCA gate is very efficient gate in term of quantum cost, area, garbage output, etc. Thus, RQCA Various types of latches have been designed in this section. As gate is used as the basic component to design latches based on reversible gate. Various types of latches that are optimal in term of number of garbage output, delay, quantum cost have been designed bellow.

A. Positive Level Triggered T Latch Based on Reversible Quantum Dot Cellular Automata Gate

Characteristical equation of the positive level triggered T latch is $Qn+1 = (T \oplus Qn)\ E+\bar{E}\ Qn$, where, E is enable signal, T is Input signal Qn is primary output signals of present state and $Qn+1$ is primary output signals of the next state. According to characteristical equation of the positive level triggered T latch, Q_n directly reflected to the output line when the primary input signal is low, as $Q_{n+1}=Q_n$. And the primary output of the positive level triggered T latch is $\bar{Q}n$ when the primary input signal is high, as $Q_{n+1}=\overline{Qn}$. The characterize equation can be mapped using single RQCA gate. Its quantum cost is 7.

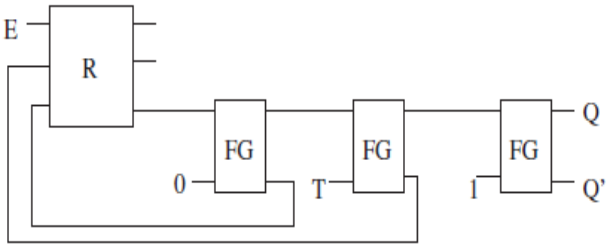

Fig 6: Positive level triggered T latch based on RQCA gate

B. Negative level Triggered T Latch Based on Reversible Quantum Dot Cellular Automata

Characteristical equation of the negative level triggered T latch is $Qn+1 = (T \oplus Qn)\ \bar{E}+E\ Qn$, where, E is enable signal, T is Input signal Qn is primary output signals of present state and $Qn+1$ is primary output signals of the next state. According to characteristical equation of the negative level triggered T latch, Q_n directly reflected to the output line when the primary input signal is low, as $Q_{n+1}=Q_n$. And the primary output of the negativelevel triggered T latch is $\bar{Q}n$ when the primary input signal is high, as $Q_{n+1}=\overline{Qn}$. The characterize equation can be mapped using single RQCA gate. Its quantum cost is 7.

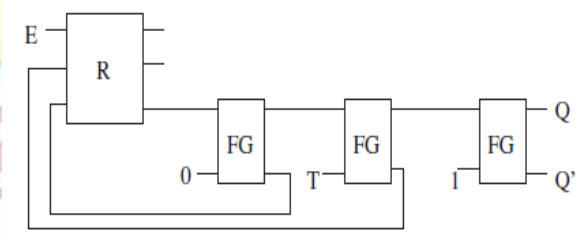

Fig 7: Negative level triggered T latch based on RQCA gate.

IV. RESULTS AND DISCUSSION

All designs have been validated with version 2.0.3 of the QCADesigner [26]. Following parameters have been used in the bistable estimation: cell size = 18 nm, convergence tolerance = 0.001000, number of samples = 182800, radius of effect = 41 nm,clock high = 9.8e22, clocklow=3.8e23, relative permittivity=12.9, clock amplitude factor = 2.000, maximum iterations per sample = 1000, and layer separation = 11.5000 nm. In QCA layout, RQCA gate will produced output after 1.25 delay of clock cycle as clock zones is used in it. Each of the proposed latches are made with single RQCA gate, thus it will be produced the output after 1.25 delay of clock cycle. Though fan-out can't be permitted in reversible circuit but fan-out can be permitted in QCA, thus all design are valid. [7] proposed a system, this paper presents an effective field programmable gate array (FPGA)-based hardware implementation of a parallel key searching system for the brute-force attack on RC4 encryption. The design employs several novel key scheduling techniques to minimize the total number of cycles for each key search

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and uses on-chip memories of the FPGA to maximize the number of key searching units per chip. Based on the design, a total of 176 RC4 key searching units can be implemented in a single Xilinx XC2VP20-5 FPGA chip. Operating at a 47-MHz clock rate, the design can achieve a key searching speed of 1.07 x 107 keys per second. Breaking a 40-bit RC4 encryption only requires around 28.5 h.

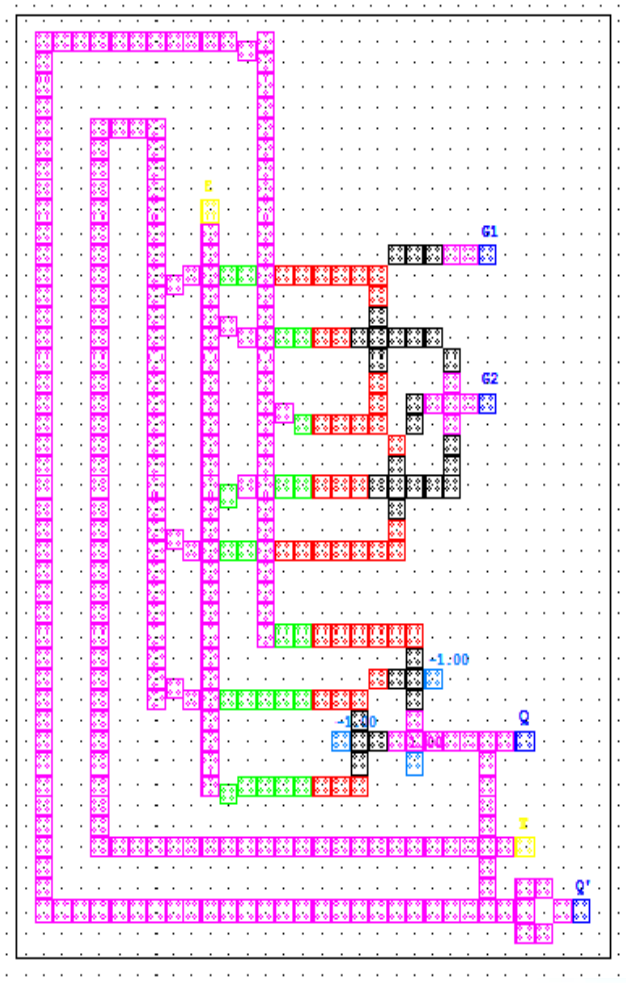

Fig 8 : QCA cell layout of positive level triggered T latch based on RQCA gate

Design of proposed positive level triggered T latch is implemented in molecular QCA framework. The QCA cell layout of the proposed positive level triggered T latch is demonstrated in Fig. 8; and the simulation results is reported in Fig. 9, which are same as expected truth table. These verifies the correctness of the circuit. Compact form of the Fig. 9summaries working functionality of the proposed design is disclosed in Table I.

Design of proposed negative level triggered T latch is implemented in molecular QCA framework. The QCA cell layout of proposed negative level triggered T latch is disclosed in Fig. 10; and the simulation waveform is reported in Fig. 11, which are same as expected truth table. This verifies the correctness of the circuit. Compact form of the simulation waveform (Fig. 11) that summaries working functionality of proposed design is reported in Table II.

All the proposed latches are more efficient than the existing latches in low power QCA in term of quantum cost, and QCA cells, etc. Similarly, other types of latches can be designed to achieve efficient sequential circuit using reversible quantum cellular automata gate.

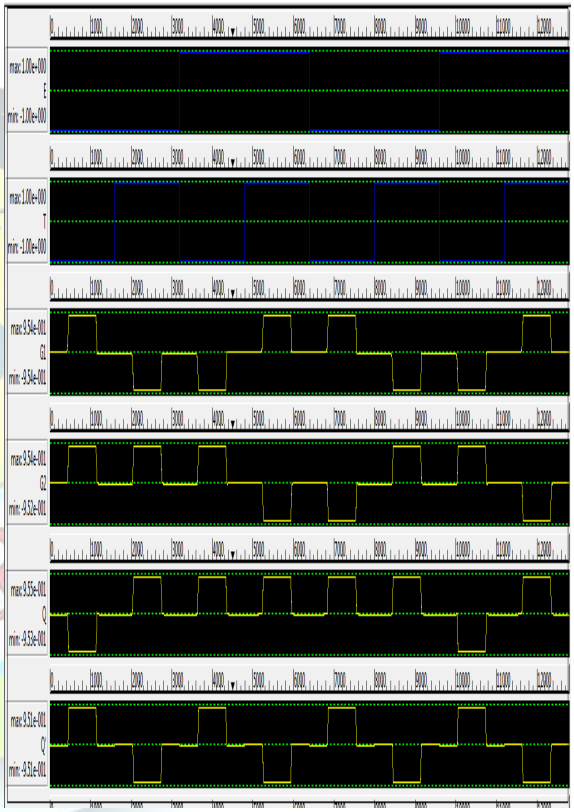

Fig 9 : Simulation waveform of positive level triggered T latch based on RQCA gate

TABLE 1: Verification of positive level triggered T latch

	Input			Output
	E	D	Q_n	Q_{n+1}
A	1	0	1	0
B	1	1	0	1
C	0	1	0	0

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D	0	0	1	1

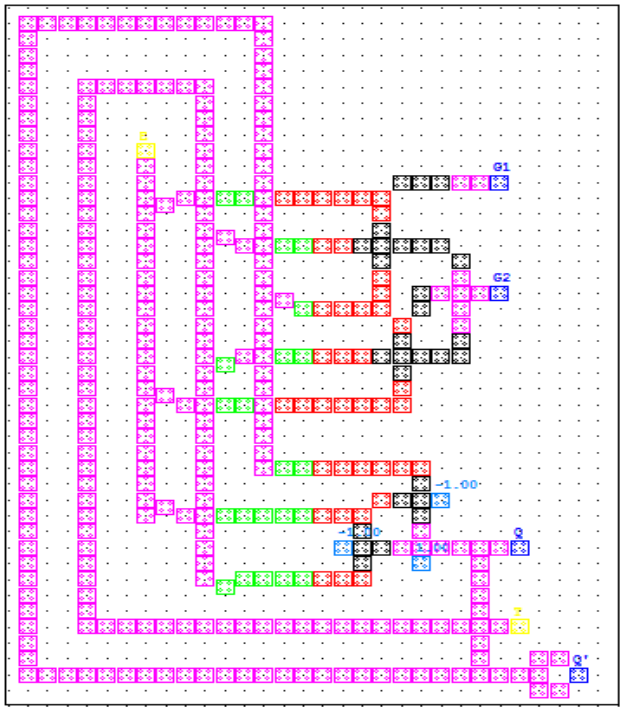

Fig 10 : QCA cell layout of negative level triggered T latch based on RQCA gate

TABLE 2: verification of positive level triggered T latch

	Input			Output
	E	T	Qn	Q_{n+1}
A	1	0	1	1
B	1	1	0	1
C	0	1	0	0
D	0	0	1	0

V. CONCLUSION

In this article optimal designs of latches based on reversible quantum dot cellular automata gate have been reported. The proposed latches are very much efficient in term of garbage outputs, quantum cost, delay. RQCA gate itself is very much efficient gate in term of quantum cost and other parameter of cost metric and having mux-ing capability; thus it has been chosen as basic component to design very much efficient latches. The proposed latches are also optimized the QCA cells and area. As, in current era, area of the circuit matters very much, thus the proposed latches are very much significant. The limitation of the proposed latches is that it does not have testability criteria. Thus, Introducing testability feature in proposed latches with optimizing cost is the future target. Finally, the proposed designs will form basis of the efficient reversible sequential circuits will be used in nano circuit and nano-computing regime.

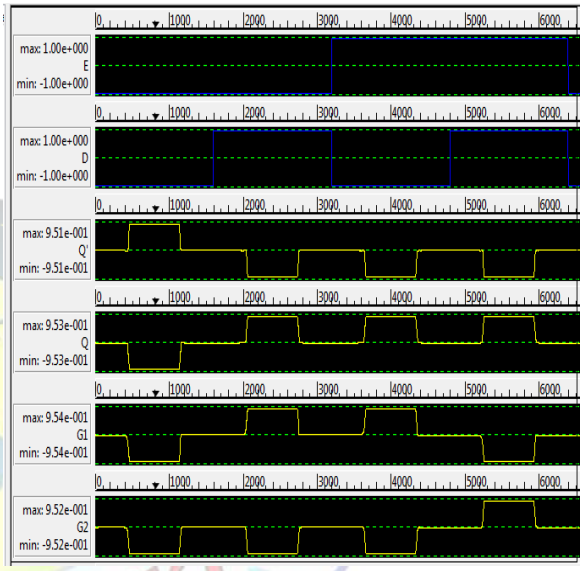

Fig 11 : Simulation waveform of negative level triggered T latch based on RQCA gate

TABLE III: Comparison analysis with proposed positive level triggered T latch based on RQCA gate

	Improvement in % from [23]	Improvement in % from [6]	Improvement in % from [9]
Quantum cost	56	77	30
Total delay	56	77	30
Garbage output	50	75	0

TABLE III: Comparison analysis with proposed negative level triggered T latch based on RQCA gate

	Improvement in % from [23]	Improvement in % from [6]	Improvement in % from [9]
Quantum cost	56.25	77	30
Total delay	56.25	77	30
Garbage output	50	75	0

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