ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Issue 5, May 2016

Novel Approach for Power Droop Reduction During Scan-Based Logic BIST

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Abstract: Scalable Approach for Power Droop Reduction during Scan-Based Logic Built In Self Test (BIST). In fact, the PD originated during the application of test vectors may produce a delay effect on the circuit under test signal transitions. This event may be erroneously recognized as presence of a delay fault, with consequent generation of an erroneous test fail, thus increasing yield loss. Several solutions have been proposed in the literature to reduce the PD during test of combinational ICs, while fewer approaches exist for sequential ICs. . In this paper, we propose a novel scalable approach to reduce the PD during at-speed test of sequential circuits with scan-based LBIST using the launch-on capture scheme. This is achieved by reducing the activity factor of the CUT, by proper modification of the test vectors generated by the LBIST of sequential ICs. The proposed approach presents a very low impact on fault coverage and test time, while requiring a very low cost in terms of area overhead.

Index Terms—Logic BIST (LBIST), microprocessor, power droop (PD), test.

I.INTRODUCTION

The aggressive scaling of microelectronic technology is allowing the fabrication of increasingly complex ICs. Together with several benefits (improved functionality, decreased cost per function, etc.), this comes through with several challenges, especially from the points of view of system test and reliability.

The increase in peak power (PP), and consequently in power droop (PD), are serious concerns for ICs' test and operation in the field. Particularly, the PP and PD during test may exceed those experienced during the IC in field operation, due to the higher switching activity (SA) induced by the applied test patterns. As a consequence, a delay effect may be generated on circuit under test (CUT) signal transitions, which may be erroneously recognized as presence of delay faults, with the consequent erroneous generation of a test fail (hereinafter referred to as false test fail), with consequent increase of yield loss.

Several solutions have been proposed in the literature to reduce PP, thus also PD, for combinational LBIST, while fewer approaches exist for scan-based LBIST. The solutions for combinational LBIST modify the internal structure of traditional LBIST LFSRs to generate intermediate test vectors. Such vectors, inserted between each couple of original test vectors, allow to reduce the SA of the CUT inputs, thus reducing the whole CUT SA. Therefore, the PP and PD are reduced as well. These techniques require low area overhead and feature negligible impact on fault coverage (FC) and test time, but are not effective in reducing PD during the capture cycles in scan-based LBIST.

In this paper, we consider the case of sequential CUTs with scan-based LBIST adopting an LOC scheme, which is frequently adopted for high-performance microprocessors. They suffer from the PD problems discussed above, especially during the capture phase, due to the high AF of the CUT induced by the applied test patterns.

The remainder of the paper is organized as follows. Section II Literature Survey, In section III we describe the considered scan-based LBIST. In Section IV, we introduce our approach for PD reduction during capture cycles. In Section V Implementation, VI results are shown finally, some conclusions are drawn in Section VII.

II. LITERATURE SURVEY

Test generator with preselected toggling for low power built-in self-test

This paper presents a new pseudorandom test pattern generator with preselected toggling (PRESTO) activity. It is comprised of a linear finite state machine (a linear feedback shift register or a ring generator) driving an appropriate phase shifter and armed with a

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International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
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number of features that allows this device to produce binary sequences with low toggling (switching) rates while preserving test coverage achievable by the best-to-date conventional BIST-based PRPGs with negligible impact on test application time.

Low power BIST for scan-shift and capture power

Low-power test technology has been investigated deeply to achieve an accurate and efficient testing. Although many sophisticated methods are proposed for scan-test, there are not so many for logic BIST because of its uncontrollable randomness. However, logic BIST currently becomes vital for system debug or field test. This paper proposes a novel low power BIST technology that reduces shift-power by eliminating the specified high-frequency parts of vectors and also reduces capture power. The authors show that the proposed technology not only reduces test power but also keeps test coverage with little loss.

Power Droop Testing

Circuit activity is a function of input patterns. When circuit activity changes abruptly, it can cause sudden drop or rise in power supply voltage. This change is known as power droop and is an instance of power supply noise. Although power droop may cause an IC to fail, such failures cannot currently be screened during testing as it is not covered by conventional fault models. In this paper we present a technique for screening such failures. We propose a heuristic method to generate test sequences which create worst-case power drop by accumulating the high-frequency and low-frequency effects. The generated patterns need to be sequential even for scan designs. We employ a dynamically constrained version of the classical D-algorithm for test generation, i.e., the algorithm generates new constraints on-the-fly depending on previous assignments. The obtained patterns can be used for manufacturing testing as well as for early silicon validation. A prototype ATPG is implemented to demonstrate the feasibility of the approach and test sequences are generated for ISCAS circuits.

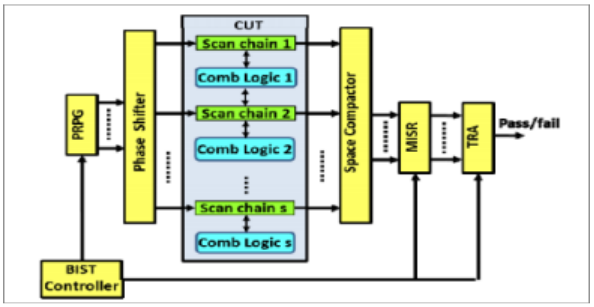

Fig. 1: Schematic of the considered scan-based LBIST architecture

III. EXISTING SYSTEM

CONSIDERED SCENARIO

We consider the widely adopted scan-based LBIST architecture represented in Fig.1. The state flip-flops of the CUT are converted into scan flip-flops, and arranged into many short scan chains (s scan chains in Fig. 1). Additional scan flip-flops are included in such scan chains to drive and sample the primary inputs (PI) and primary outputs (PO), respectively.

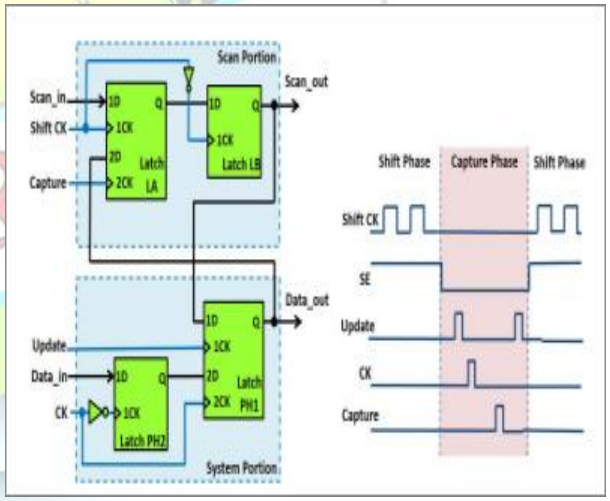

Fig. 2: Considered scan FF and signals' timing

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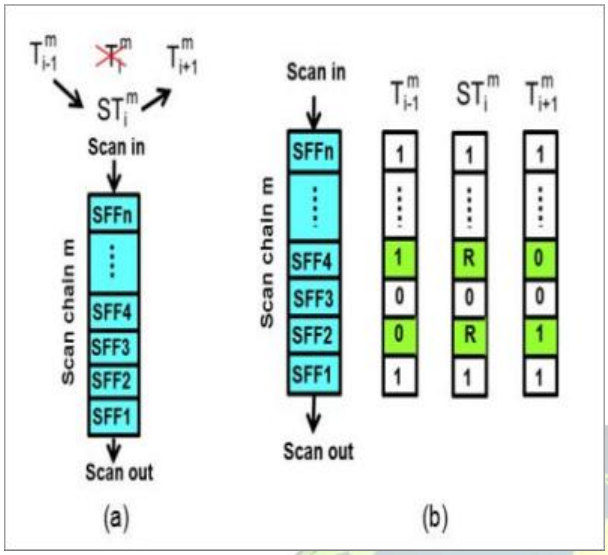

Fig. 3: Schematic of (a) sequence of test vectors filling each scan chain m, (b) bits in the ST vector ST^m_i and in the test vectors applied/to be applied at the previous/following capture phase (T^m_{i-1}/T^m_{i+1}).

The Pseudo-Random Pattern Generator (PRPG) is implemented by an LFSR. The Phase Shifter (PS), allowing to reduce the correlation among the test vectors applied to adjacent scan-chains, is composed by an XOR network expanding the number of outputs of the LFSR in order to match the number of scan chains s. In fact, the number of LFSR outputs is usually considerably smaller than the number of scan chains. At the same clock cycle, the PS provides as outputs, the current LFSR sequence together with many future/past sequences. As described later on, this feature will be exploited by our proposed solution in order to derive the new test vectors allowing to reduce PD during capture cycles.

The Space Compactor compacts the outputs of the s scan chains to match the number of inputs of the MISR. The MISR, as well as the Test Response Analyzer (TRA) and the BIST Controller are the same as in conventional scan-based LBIST. As known, two phases can be identified in scan-based LBIST: a shift phase, during which the scan chains are filled with test vectors, and a capture phase, in which the test vectors are applied to the CUT and the produced outputs are sampled. In particular, during the shift phase, at each clock cycle, the phase shifter provides a new bit to each one of the s scan chains (in parallel). Thus, in this phase, the test vector T_i^m to be applied to the CUT at the ith capture cycle is loaded into the mth scan chain (m = 1..s) after n shift cycles (where n is the number of scan flip-flops of the longest scan chain). After such shift cycles, a single capture cycle is performed, and the CUT response is sampled on the scan chains. Then, other n scan shift cycles are required to shift-out the CUT response and to shift-in the new test vector T^m_{i+1} (m = 1..s).

As for scan-flip-flops, we have considered the widely adopted scheme in, which updates its output only at the beginning of capture cycles, while keeping it constant to its previous value loaded during the shift phase.

IV. PROPOSED APPROACH FOR POWER DROOP REDUCTION DURING SCAN-BASED LBIST

The goal of our approach is to reduce the PD that may generate false test fails during at- speed test with scan-based LBIST. Such a PD occurs after the application of a new test vector to the CUT. This occurs at the launch CK (Update pulse in Fig. 2) within capture phases. The generated PD is proportional to the CUT AF induced by the application of a new test vector, which in turn depends on the AF of the scan FFs' outputs. For the considered scan FFs (Fig. 2), such an AF depends on the number of FFs' outputs switching when the new test vector is applied. Therefore, the target of our approach is to reduce the number of FFs' outputs transitions occurring after the application of a new test vector to the CUT.

In order to derive a mathematical description of our pro- posed solution, we make the following simplifying assumptions for Conv-LBIST.

1) All scan chains have the same number of scan FFs.
2) The maximum AF between two following test vectors T^m_i and T^m_{i+1} is the same for all scan chains (m = 1 ... s).

However, by logic-level simulations performed by the Synopsys Design Compiler tool, we have verified that our approach can achieve the same AF reduction also if such simplifying hypotheses are not satisfied.

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Available online at www.ijartet.com
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A. Approach With 1 Substitute Test Vector

For each scan chain m (m = 1 ... s) , one ST vector S T_i^m replaces the original test vector T_i^m to be applied to the CUT at the i th capture phase according to Conv-LBIST (Fig. 3). It will be shown that this enables a 50% AF reduction compared with Conv-LBIST.

In our approach, the ST vector S T_i^m to be charged in the Scan-Chain (SC) m and applied to the CUT at the ith capture phase is constructed based on the structure of test vectors T_{i-1}^m and T_{i+1}^m to be applied at the (i − 1)th and (i + 1)th capture phases.

Denoting by S T_i^m (j) , T_{i-1}^m (j) ,and T_{i+1}^m(j) the logic value of the j th bit in test vectors S T_i^m , T_{i-1}^m,and T_{i+1}^m , respectively, S T_i^m (j) is chosen as follows

$$ST_i^m(j) = \begin{cases} T_{i-1}^m(j), & \text{if } T_{i-1}^m(j) = T_{i+1}^m(j) \\ R, & \text{if } T_{i-1}^m(j) \neq T_{i+1}^m(j) \end{cases}$$

where R denotes a random bit. Therefore, in all bit positions j in which test vectors T_{i-1}^m and T_{i+1}^m present the same logic value, S T_i^m maintains the same logic value as in the previous test vector T_{i-1}^m. Instead, in the bit positions j in which test vectors T_{i-1}^m and T_{i+1}^m differ, ST_i^m assumes a random logic value R . The bit R can simply come from one of the outputs of the LFSR. Starting from the (i − 1)th capture phase (Fig. 3), the new test vector sequence in each scan chain m will be as follows :

$$T_{i-1}^m - ST_i^m - T_{i+1}^m - ST_{i+2}^m - T_{i+3}^m \cdots$$

Therefore, the number of bits changing logic value between the following test vectors with the new sequence T_{i-1}^m − S T_i^m − T_{i+1}^m will be equal to, or smaller than, those with the original test sequence T_{i-1}^m − T_i^m − T_{i+1}^m of Conv-LBIST.

In this regard, it is to be noted that the considered scan- FFs (Fig. 2) update their outputs only at capture phases, while maintaining them constant during the shift phases. [6] discussed about Improved Particle Swarm Optimization. The fuzzy filter based on particle swarm optimization is used to remove the high density image impulse noise, which occur during the transmission, data acquisition and processing. The proposed system has a fuzzy filter which has the parallel fuzzy inference mechanism, fuzzy mean process, and a fuzzy composition process. In particular, by using no-reference Q metric, the particle swarm optimization learning is sufficient to optimize the parameter necessitated by the particle swarm optimization based fuzzy filter, therefore the proposed fuzzy filter can cope with particle situation where the assumption of existence of "ground-truth" reference does not hold. The merging of the particle swarm optimization with the fuzzy filter helps to build an auto tuning mechanism for the fuzzy filter without any prior knowledge regarding the noise and the true image. Thus the reference measures are not need for removing the noise and in restoring the image. The final output image (Restored image) confirm that the fuzzy filter based on particle swarm optimization attain the excellent quality of restored images in term of peak signal-to-noise ratio, mean absolute error and mean square error even when the noise rate is above 0.5 and without having any reference measures.

Therefore, the AF between successive test vectors will determine the AF of the CUT at each capture cycle. The presence of a random bit R in ST_i^m in the bit positions where T_{i-1}^m and T_{i+1}^m differ allows the new sequence T_{i-1}^m − S T_i^m − T_{i+1}^m to preserve the randomness of the original sequence. Therefore, as shown in Section V, the number of test vectors required to achieve a target FC does not increase compared with the application of the original test sequence. The maximum AF between the following test vectors loaded in each SC in Conv-LBIST (AF^{sc}_{con}) is reduced to a half(AF^{sc}_{con}/2) by our approach. Consequently, denoting by AF^{tot}_{1ST} the maximum AF between any two successive test vectors applied to the CUT at successive capture phases, for our approach with 1 ST vector, it is

$$AF_{1ST}^{tot} = AF_{con}^{tot}/2$$

Where AF^{tot}_{1ST} is the max AF obtained with Conv-LBIST.

B. Approach With N Substitute Test Vectors

In order to reduce further the AF during capture phases of scan-based LBIST, a higher number N of ST vectors, ST_i^m, ST_{i+1}^m... ST_{i+N-1}^m, with $ST^m_{i+1} = \cdots$ = S ST_{i+N-1}^m = ST^m_i , can be used to replace, for each scan chain m , N original test vectors T^m_i up to T^m_{i-1}.

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Similar to the case of 1 ST vector, the ST vectors ST^m_i... ST^m_i to be applied at the ith ...(i+N − 1)th capture phases are constructed based on the test vector T^m_{i-1} to be applied at the (i − 1)th capture phase, and the test vector T^m_{i+N} to be applied at the (i + N)th capture phase. Denoting by ST^m_i (j) , T^m_{i-1} (j) and T^m_{i+N}(j) the logic value of the jth bit in test vectors S T^m_i, $T^m_{i-1}$and T^m_{i+N}, respectively,

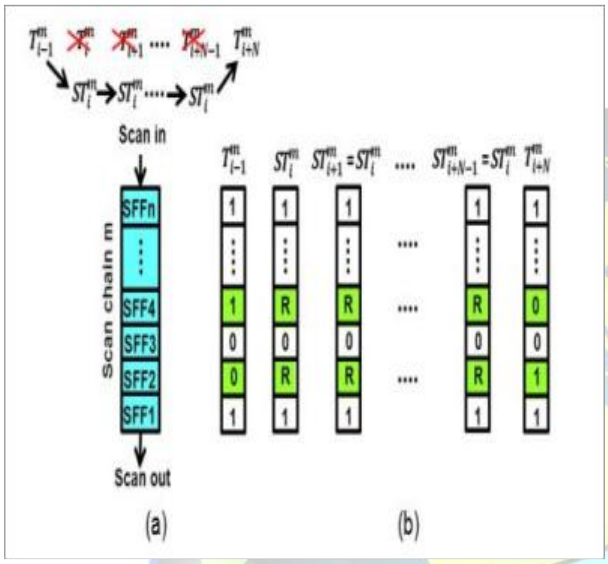

Fig. 4: Test vectors' selection of our approach with N ST vectors. (a) Sequence of test vectors filling each scan chain. (b) ST vectors ST^m_i ... ST^m_{i+N-1}.

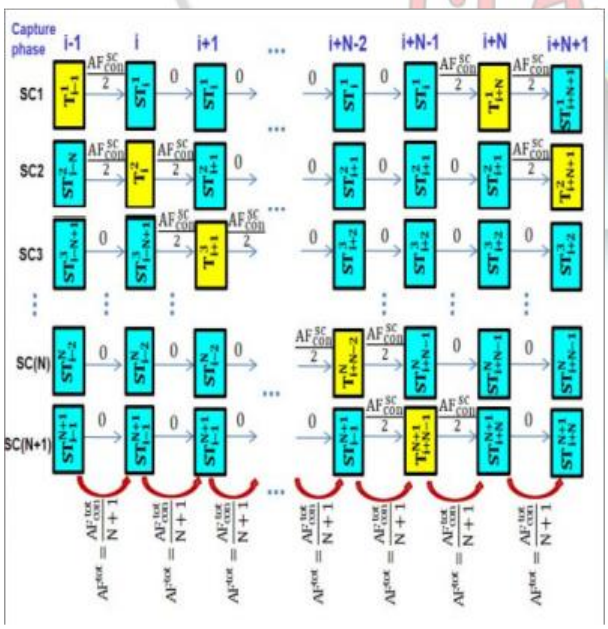

Fig. 5: Interleaved test vectors' application to the CUT and AF values for each capture phase for the case with N ST vectors.

$ST^m_i(j)$ is determined as follows:

$$ST_i^m(j) = \begin{cases} T_{i-1}^m(j), & \text{if } T_{i-1}^m(j) = T_{i+1}^m(j) \\ R, & \text{if } T_{i-1}^m(j) \neq T_{i+1}^m(j) \end{cases}$$

where, as before, R denotes a random bit. The number of bits changing logic value between successive test vectors with the new sequence $T^m_{i-1} - ST^m_i - \cdots - ST^m_{i+N-1} - T^m_{i+N}$ (Fig. 4) will be equal to, or smaller than in the original test sequence $T^m_{i-1} - T^m_i - \cdots - T^m_{i+N-1} - T^m_{i+N}$ of Conv-LBIST. The presence of a random bit R in STm i in the bit positions where T^m_{i-1} and T^m_{i+N} differ allows the new sequence $T^m_{i-1} - ST^m_i - \cdots - ST^m_{i+N-1} - T^m_{i+N}$ to preserve the randomness of the original sequence in these bit positions. The number of test vectors required by our approach to achieve a target FC is approximately the same as that in Conv-LBIST, even for the case of N = 10 ST vectors. As represented in Fig. 5, we interleave the insertion of the N ST vectors, so that they are applied at different capture phases for the different SCs. Thus, between any two successive capture phases, the same ST vector is loaded in (N − 1)-out-of-(N + 1) scan chains, which consequently exhibit $AF^{sc} = 0$. Instead, 2-out-of-(N+1) scan chains present a transition between an original test vector and an ST vector, thus presenting an $AF_{sc} = AF^{sc}_{con}/2$. If the number of scan chains s is a multiple of N + 1, the total AF between any two following test vectors is:

$$AF^{tot}_{N\,ST} = \sum_{m=1}^{s} AF^{sc\_m} = \frac{s}{N+1}\left(\frac{AF^{sc}_{con}}{2} + \frac{AF^{sc}_{con}}{2} + 0\right) = \frac{AF^{tot}_{con}}{N+1} \quad (1)$$

where, as before, $AF^{tot}_{con} = sAF^{sc}_{con}$. We have verified that, even if s is not a multiple of N + 1, and s N (e.g., s > 10N), that is if the number of SCs s is much higher than the number of ST vectors N, (1) gives a good approximation of the AF^{tot}_{NST}. From (1) we can also derive that, with our approach, it is $AF^{tot} = AFt^{ot}_{con}/3$ for N = 2, $AF^{tot} = AF^{tot}_{con}/4$ for N = 3, AFtot = $AF^{tot}_{con}/5$ for N = 4, and so on. As will be shown later,

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ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Issue 5, May 2016

such reductions are achieved at no increase in the number of test vector (TVs) needed to reach a target FC, and with a limited cost in terms of AO.

V. IMPLEMNTATION

To implement our approach, we assume the presence of a PS feeding the scan-chains of the CUT (Fig. 1). However, should a phase shifter not be present within the considered scheme, our approach can be implemented by adding an equivalent structure at the LFSR outputs.

A. Case of 1 Substitute Test Vector

Denoting by Om (m = 1 ...s) the PS output feeding the scan chain m, the logic value $T^m_i(j)$ in the jth position of the ith test vector of the scan chain m is given by

$$T_i^m(j) = O^m(\xi)$$

where ξ = n(i − 1) + j is the total number of shift CKs from the beginning of the test. This way, the logic values loaded in the jth position of SC m in the shift phases before the (i − 1)th, the ith, and the (i + 1)th capture phases will be equal to the logic value present at the output Om of the PS, after ξ − n, ξ, and ξ + n shift CKs, respectively, counted from the beginning of the test. Thus, for each SC m and capture phase i, we can express the logic values present in the jth position of the previous and the next test vectors ($T^m_{i-1}(j)$ and $T^m_{i+1}(j)$, respectively) as

$$T_{i-1}^m(j) = O^m(\xi - n); \quad T_{i+1}^m(j) = O^m(\xi + n). \qquad (2)$$

Since the PS gives to its outputs many past/future values of each output Om, we can determine the values of Om(ξ − n) and Om(ξ + n) from the current value present at two proper PS outputs. Therefore, there exist two PS outputs Ok and O p, with k = p = m, such that

$$O^m(\xi - n) = O^k(\xi); \quad O^m(\xi + n) = O^p(\xi). \qquad (3)$$

We exploit the relations in (2) and (3) to derive a low cost hardware implementation of our approach. As described in Section IV-A, our approach forges the ST vector ST^m_i by comparing T^m_{i-1} and T^m_{i+1}. Thus, we can derive ST^m_i by simply comparing the outputs O^k and O^p of the PS at each shift CK j.

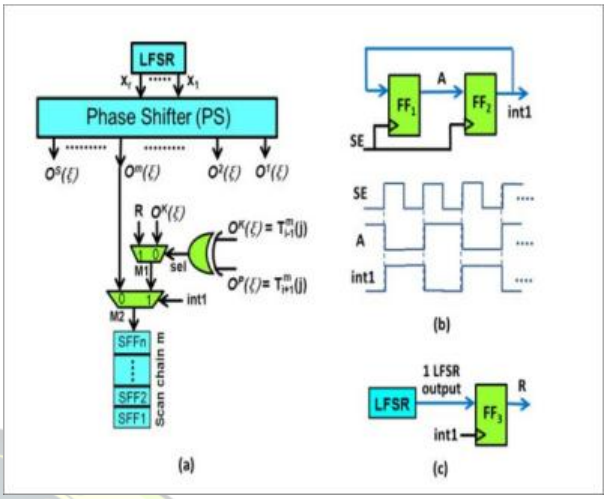

Fig. 6: Schematic of (a) possible implementation of our approach, (b) possible scheme to generate signal int1, and (c) strategy to generate the random bit R.

As an example, Fig. 6(a) shows a possible implementation of our proposed scheme, for the case in which the depth of the longest chain(s) is n. Our approach requires two multiplexers (M1 and M2) and an XOR gate for each scan chain m. M2 allows us to load the following in the scan chain m:

1) either the test vectors T^m_{i-1} and T^m_{i+1} generated by the PS during the shift phases before the (i −1)th and (i +1)th capture phases, by setting the selection signal int1 = 0;

2) or the ST vector ST^m_i provided by M1 during the shift phases before the ith capture phase, by setting int1 = 1. Particularly, the signal int1 is generated in such a way that it switches from 0 to 1 (and vice versa) at the following capture phases. Fig. 6(b) depicts an example of int1 generation, where FF1 and FF2 denote D FFs. Initially, FF1 is set to 1 and FF2 is set to 0 (int1 = 0). Both FF1 and FF2 are clocked by the SE signal. Thus, at each SE rising edge, int1 switches from 0 to 1 alternately.

The XOR gate compares the logic value at the PS output Ok (ξ) [equal to $T^m_{i-1}(j)$] with the logic value at the PS output O p(ξ) [equal to $T^m_{i+1}(j)$] at each shift CK j. Thus, it is: sel = 0, if Ok (ξ) = O p(ξ), indicating that $ST^m_i(j)$ should be equal to Ok (ξ) = $T^m_{i-1}(j)$; sel = 1, if Ok (ξ) = O p(ξ), indicating that STm i (j) should be a random value R. Finally, the bit R can be simply generated from any output of the LFSR. Since in our scheme we considered the same R value for the whole

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ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
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shift phase, we can simply generate R by sampling any output of the LFSR at the beginning of each shift phase. Fig. 6(c) shows a possible scheme to generate the bit R. One LFSR output feeds an FF (FF3), which is clocked by the int1 signal.

VI. RESULTS

Fig. 7(a)–(d) also reports the relative AF reduction allowed by our approach over Conv-LBIST [AF=100∗(AFOURAF$_{Conv-LBIST}$)/AF$_{Conv-LBIST}$] as a function of the number of ST vectors. We can observe that, for a number of ST vectors higher than 4, our approach enables an AF reduction higher than 80%. Moreover, we can note that, for all benchmarks, the AO of our approach over Conv-LBIST increases linearly with the number of ST vectors. A minimum of approximately 1.5% AO is achieved with 1 ST for the s38584 benchmark, and a maximum of approximately 14% AO is reached with 10 ST vectors for the s13207 benchmark.

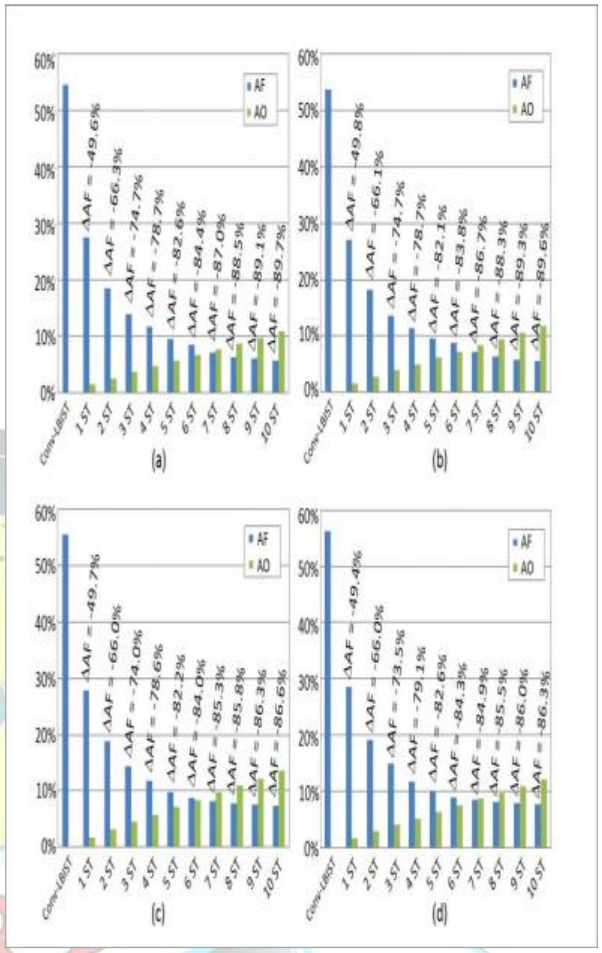

Fig. 7: Simulation results showing the AF of Conv-LBIST, as well as the AF and AO of our approach with up to 10 ST vectors for the considered benchmark circuits. (a) s38584. (b) s38417. (c) s13207. (d) s15850.

The comparison results are reported in Table II. The AF and #TV relative variations are calculated as: = 100∗(OUR – [9, 21])/[9, 21]. From Table II we can observe that the approaches in [9] and [21] require a significantly higher number of test vectors (more than twice in most cases) than that required by our solution to achieve the same target FC. In addition, our solution allows us to achieve a lower maximum AF.

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TABLE I
NUMBER OF TEST VECTORS (#TV) REQUIRED BY Conv-LBIST AND BY OUR SOLUTION TO ACHIEVE A TARGET FC

Benchmark			s38584	s38417	s13207	s15850
# SCs			59	67	28	25
Target FC			95.89%	95.53%	98.33%	94.00%
Conv-LBIST		#TV	32800	39104	30464	38112
Our solution	1 ST	#TV	32660	38667	30436	37217
		Δ#TV	-0.43%	-1.12%	-0.09%	-2.35%
	2 ST	#TV	32657	38587	30514	37357
		Δ#TV	-0.44%	-1.32%	0.16%	-1.98%
	3 ST	#TV	32660	38448	30601	37213
		Δ#TV	-0.43%	-1.68%	0.45%	-2.36%
	4 ST	#TV	32759	38627	30588	37486
		Δ#TV	-0.12%	-1.22%	0.41%	-1.64%
	5 ST	#TV	32790	38751	30607	37580
		Δ#TV	-0.03%	-0.90%	0.47%	-1.40%
	6 ST	#TV	32869	38699	30859	37604
		Δ#TV	0.21%	-1.04%	1.30%	-1.33%
	7 ST	#TV	32934	38755	30891	37616
		Δ#TV	0.41%	-0.89%	1.40%	-1.30%
	8 ST	#TV	32962	38872	30955	37838
		Δ#TV	0.49%	-0.59%	1.61%	-0.72%
	9 ST	#TV	32989	38904	31019	37854
		Δ#TV	0.58%	-0.51%	1.82%	-0.68%
	10 ST	#TV	32996	38917	31158	37866
		Δ#TV	0.60%	-0.48%	2.28%	-0.64%

TABLE II
NUMBER OF TEST VECTORS (#TV) TO ACHIEVE A TARGET FC AND MAXIMUM AF FOR OUR APPROACH WITH 1 ST VECTOR AND FOR THE SOLUTIONS IN [9] AND [21]

		s13207	s15850	s38417	s38584
Target FC (%) [9]		96.8	91.71	95.37	95.24
Solution in [9] with n=2	#TV	54500	29500	80500	49000
	AF (%)	30.7	31.9	27.9	28.9
Solution in [21] (WTM=25%)	#TV	33618	31835	43449	37594
	AF (%)	30.5	31.9	31.2	31.1
Our solution with 1 ST	#TV	14006	2514	21534	18496
	Δ#TV [9] (%)	-74	-91	-73	-62
	Δ#TV [21] (%)	-58.9	-92.1	-50.4	-50.8
	AF (%)	27.9	28.5	27.0	27.5
	ΔAF [9] (%)	-9.3	-10.8	-3.4	-4.7
	ΔAF [21] (%)	-8.5	-10.7	-13.5	-11.6

VII.CONCLUSION

We have presented a novel approach to reduce peak power and power droop during the capture cycles in scan-based Logic BIST, thus reducing the probability that the induced delay effect is erroneously recognized as presence of a delay fault, with consequent erroneous generation of a test fail. We showed that our approach allows to reduce by approximately 50% the switching activity (SA) in the scan chains between following capture cycles, with respect to standard scan-based LBIST. This is achieved by exploiting the operation of the phase shifter, usually inserted in LBIST structures in order to reduce the correlation among the test patterns applied to adjacent scan-chains. We also showed that our approach requires a significantly lower test time. The proposed approach exhibits no impact on test coverage and test time, while requiring a very low cost in terms of area overhead. Moreover, it is fully compatible with standard scan-based LBIST architectures.

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ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Issue 5, May 2016

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ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Issue 5, May 2016

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