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A Fault Current Limiting Function Multilevel Cascaded-Type Dynamic Voltage Restorer

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***Abstract*: This paper introduces another multilevel cascaded-sort dynamic voltage restorer (MCDVR) with fault current restricting function. This topology can work in two operational modes: 1) pay mode for voltage variances and unbalances, and 2) cut off restricting mode. The present constraining function of the MCDVR is performed by enacting against parallel thyristors amid the short out fault, and deactivating them amid ordinary operation. The mathematical model of the MCDVR system is likewise settled in this paper. The control conspire plan and ideal parameter choice are outlined based on the point by point hypothetical investigation of the converter. The transient states of the MCDVR in both the pay mode and current-constraining mode are likewise broke down. Simulation results based on the PSCAD/EMTDC programming and test results on a research center setup help to approve the proposed topology and the hypothetical examination.**

***Index Terms*—Dynamic voltage restorer (DVR), multilevel inverters, fault current limiter, voltage restoration.**

I. INTRODUCTION

There are two noteworthy difficulties that cutting edge power grids must manage: voltage vacillations and short out faults [1]-[2]. There are renewable energy based generators (e.g. wind, solar) in the grid that can have fluctuating output generation capabilities. Besides, the exponentially expanding power request and prominence of distributed generation have brought about expanding fault current levels.

A dynamic voltage restorer (DVR) could produce a remuneration voltage, which is embedded into the grid through a series transformer [3-5], and could limit any voltage changes. In any case, a vast short out current will be drafted into the voltage-source inverter (VSI) through the series transformer amid faults. To conquer this issue, one option is a side step conspire. It is a "safeguard" system in which the DVR can be taken disconnected. Another approach is to enhance the effectiveness of the DVR [7]. The control plans appeared in [7] permits the series compensator to accomplish load-side voltage restoration for upstream faults, and current restricting for downstream faults. The drawback of this approach is that an expansive limit storage system is vital at the DC side. In addition, the proposed topology comprises of a varistor and two or three against parallel thyristors, which are associated in parallel to the secondary winding of the series transformer [8].

The central assurance component is a varistor, and the low-saturation attractive attributes of the series transformer are hard to accomplish. All things considered, the topology just shields the series VSI from the over-current and does not restrain expansive currents from flowing in the system [9].

Then again, there are diverse topologies for fault current limiters (FCLs, for example, superconducting FCLs, solid-satisfy FCLs, and reverberation sort FCLs [10]-[11]. In any case, the extra hardware unavoidably prompts an expansion in the general venture and capital cost. Subsequently, a superior decision is enhancing the customary functionality of the DVR as far as possible the short out current. The series compensator could finish the different functions by including another branch [12]-[13]. Besides, the proposed DVR can change the power factor through a thyristor-exchanged inductor branch [12]. Besides, a typical method is the place the side step is associated in parallel to the primary of the series transformer [13]. The hardware comprises of a side step electronic switch, comprised of against parallel thyristors, and a mechanical sidestep switch which permits the static series compensator (SSC) to be skirted [14]. In spite of the fact that the SSC is ensured amid faults, the fault-current isn't constrained to the coveted esteem.

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A fault current constraining dynamic voltage restorer (FCL-DVR) was proposed in [15]. Notwithstanding, the transient state of the FCL-DVR was not portrayed in detail. The warm soundness and maximal withstand voltage of the present restricting module were likewise disregarded. The ideal parameter determination of the series transformer ratio has not been taken in [15]. Then again, high power multilevel inverters produces bring down harmonic currents, and requires bring down rating power switches [16]-[18]. These previously mentioned points are of incredible centrality for the plan and utilization of the multifunctional system.

In this paper, another multilevel cascaded-sort dynamic voltage restorer (MCDVR) is acquainted with lessen the ratio of the transformer. The MCDVR gives comparative course inverter execution benefits, for example, the lower power rating and cost of the power devices utilized. Additionally, it restricts the short out current rapidly amid faults, and offers more viable insurance to the system. The contents of the paper are organized as follows: the topology of the MCDVR and its current-limiting function are described in Section II. In Section III, an effective control scheme and optimal parameter selection for the MCDVR are proposed. In Section IV, the transient response state is studied in detail. In Section V, simulations and experimental results of the proposed MCDVR are provided. Finally, the main conclusions are presented in Section VI.

II.MCDVR TOPOLOGY

The MCDVR system based on multilevel inverters is appeared in Fig. 1. It comprises of a series-associated transformer T1, an energy storage capacitor Cdc, a seven-level course inverter, and a filter. The transformer T1 not just diminishes the voltage prerequisite of the inverters, yet additionally gives isolation between the inverter and the utility grid. There are likewise hostile to parallel thyristors K, which are the main contrast between the MCDVR and conventional DVRs [19]. In most reasonable inverters, there is likewise a sidestep switch associated in parallel with the infusion transformer [18]. Essentially, the energy storage capacitor (CDC) gives the expected power to make up for any voltage sag or variance in the utility grid. Albeit low-arrange harmonics are disposed of by the cascaded H-bridge, an extensive number of high-arrange harmonics are as yet show near the equal switching frequency [18], [20]. Therefore, a LC filter involving Lf and Cf is utilized as the filter for the cascaded multilevel DVR, and in addition an impedance to restrict the fault current. In this way the LC filter can accomplish two unique functions, and this will advance the full usage of the hardware.

A. Function of the MCDVR

Under the ordinary working condition, the counter parallel thyristors are not let go. In this way, the proposed MCDVR is successfully observed as just containing the H-bridge course DVR. This multilevel converter not just understands the higher power and voltage appraisals utilizing littler rating switches, yet additionally lessens the general harmonic substance. Furthermore, it adds to a littler dv/dt in the output and along these lines diminishes undesirable electromagnetic interference [21].

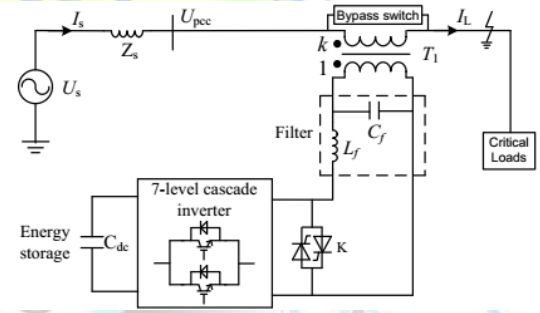

Fig. 1: Schematic diagram of the proposed MCDVR.

Then again, when a short out fault happens along the distribution line, the load current increments strongly. The thyristors are then enacted to embed the filter into the main current way through the series transformer. The filter, the series transformer and the counter parallel thyristors together shape variable impedance that works as the present restricting module. The fault current is restricted to the coveted esteem, and the components of the VSI and other hardware in the system can be ensured. As the voltage over the series transformer isn't the same in the distinctive modes, the mathematical model of the MCDVR is

$$U_{\text{DF-DVR}} = k\alpha U_{\text{dc}}\,\text{sgn}(x) + Z_{\text{lim}} I_{fault}(1-\text{sgn}(x)) \quad (1)$$

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Where *U*dc is the dc-link voltage, *k* is the turns-ratio of the series transformer, and α is the modulation depth. Importantly, sgn(*x*) is the return function, and *x* is any valid value. For example, if the system is in the voltage regulation mode, *x*=1 and sgn(*x*) =1. Thus (1) can be rewritten as

$$U_{\text{DF-DVR}} = k\alpha U_{\text{dc}}. \quad (2)$$

Instead, if the system is in the current-limiting mode, *x*=0 and sgn(*x*) =0. Then (1) can be rewritten as

$$U_{\text{DF-DVR}} = Z_{\text{lim}} I_{fault}. \quad (3)$$

B. Current Limiting by the MCDVR

The single-phase proportionate circuit of the MCDVR in current-restricting mode is appeared in Fig. 2. At the point when a short out fault happens, the IGBTs of the faulted phase in the VSI are killed and the course inverter is closed down. At that point, the thyristors are enacted. In this manner, the filter is embedded into the main current way through the series transformer T1, as appeared in Fig. 2(a).

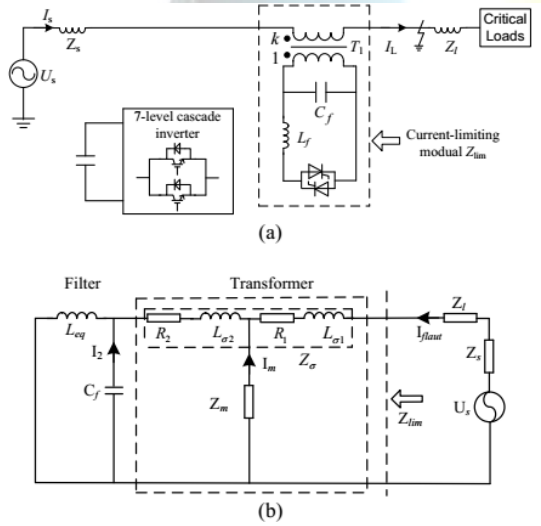

Fig. 2: MCDVR in current limiting condition: (a) Schematic diagram; (b) Single-phase equivalent circuit.

The short-circuit current during the fault is then

$$I_{fault}(t) = \frac{U_s(t)}{Z_s + Z_l + Z_{\text{lim}}} \approx \frac{U_s(t)}{Z_{\text{lim}}} \quad (4)$$

Where, *Z*lim is the limiting impedance. As *Z*lim>>*Z*s + *Z*l, the *I*fault is mainly determined by the magnitude of *Z*lim. Consequently, it can be limited to the desired value to protect the equipment in the system. *Z*lim is determined by *L*σ1, *L*σ2, *R*1, *R*2, *L*m, C*f*, and *k*. *L*σ1 and *R*1 are the leakage reactance and resistance of the primary side respectively. *L*σ2 and *R*2 are the leakage reactance and resistance of the secondary side respectively. *Z*m is the excitation impedance of the transformer.

Referring to Fig. 2(b), C*f* is usually a small value and hence $|1/jC\omega|$ is typically a large value. Furthermore, the influences of L*σ*1, *R*1, *Lσ*2, *and R2* can be ignored. It can then be concluded that the limiting impedance is

$$|Z_{\text{lim}}| \approx k^2 (|j\omega L_{\text{eq}}| // |(1/j\omega C_f)| // |Z_m|). \quad (5)$$

Where *L*eq is the equivalent impedance and therefore

$$L_{eq} = L_f \cdot \frac{\pi}{2\pi - 2\delta + \sin 2\delta} \quad (6)$$

Where δ is the trigger delay angle of the thyristors. In reality, $|Zm| >> k^2 |j\omega Leq|$ and $|1/j\omega C_f| >> |j\omega Leq|$. Thus, *I*fault is mainly determined by $|j\omega Leq|$. Hence, the short-circuit current can be limited to the desired value by suitable selection of α, *Lf* and *k*.

III. CONTROL SCHEME DESIGN AND OPTIMAL PARAMETER SELECTION

The MCDVR can work in one of the two operation modes as indicated by the state of the grid. In this area, the control conspire outline and ideal parameter choice are clarified.

A. Control Scheme

The primary disadvantage of the H-bridge inverter is the plausibility of coincidentally short circuiting the information dc-link voltage by all the while switching on the two transistors in a leg of the inverter. This is the reason, in such converters, a dead time is normally acquainted with evade this shoot-through and vast over currents. New course inverters have additionally been proposed to take care of this shoot-through issue, and they can enormously enhance the general system unwavering quality [22-23]. In this paper, the cascaded H-bridge inverter is embraced as it is in wide utilize [16], [24].

At the point when the MCDVR is in the voltage pay mode, it comprises of a multilevel inverter with three H-bridge cells in each phase (combining a 7-level output voltage), a little filter at

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the air conditioner side, and three dc link capacitors. One of the main focal points of this topology, contrasted with other multilevel topologies, is that the maximum number of levels is just restricted by isolation limitations. Additionally, the secluded structure of the converter prompts preferences as far as assembling and general system adaptability [24].

A considerable amount of research has been led on the control strategies for course inverter-based DVRs [5], [12]-[16]. The phase-moved PWM is a broadly utilized balance procedure for cascaded multilevel inverters as it offers an even power distribution among the cells and is anything but difficult to execute free of the quantity of inverters. This regulation moves the phase of every bearer by a reasonable edge to lessen the general harmonic substance of the output voltage [25]. As it offers various advantages, the outlined inverter plan and adjustment methodology are utilized as a part of this paper. In addition, the voltage remuneration control methodology for a MCDVR system, as depicted in [4], is utilized.

At the point when the MCDVR is in fault current-constraining mode, it works as examined beforehand. This paper mainly concentrates on the fault current identification strategy and the transient state of the fault current constraining operation mode. A fault current discovery technique is created to detect the load current and its rate of progress. The fault current is subsequently restricted to a satisfactory level quickly, even before achieving its initially crest [26]-[27]. The plans of the unequal unsettling influence are embraced [15], and are not examined in this paper for quickness. The points of interest of the transient state of the MCDVR are depicted further in Section IV.

B. Optimal Parameter Selection

1) Cascaded inverter design: Using a PWM control strategy, the switches in the multilevel inverters should satisfy the following conditions

$$N_S \geq (U_{dvr}/n)/kU_r \quad (7)$$

$$N_P \geq (kI_L)/I_r \quad (8)$$

Where *N*S and *N*P are the number of series switches in each inverter level and parallel branches in each leg of the inverter respectively. *U*dvr is the rated peak value of the series injected voltage of the MCDVR. *I*L is the rated value of the load current. *U*r and *I*r are the rated blocking voltage and the rated current of each switching component respectively. *n* is the total number of inverter levels in each phase. Then, the rated DC-link voltage of each inverter level *U*dch should meet

$$U_{dvr}/n \leq U_{dch} \leq N_S U_r . \quad (9)$$

From (7)-(9), the overall minimum capacity of the switching devices can be obtained

$$S_{min\_total} = nN_{S\_min}N_{P\_min}U_rI_r \geq U_{dvr}I_L \quad (10)$$

Where, *N*S_min and *N*P_min are the minimum values of *N*S and *N*P respectively. Smin_total is the total minimum capacity of the multilevel inverters. It can be concluded that the capacity of the switching device, which is depended on *U*r and *I*r, can be altered by setting the values of the turns-ratio *k*, *N*S_min and *N*P_min.

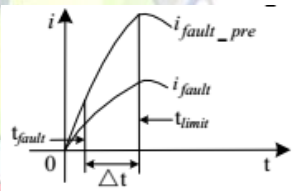

Fig. 3: Change in the fault current at different ratios of the series transformer.

When a short out fault happens (e.g. a three-phase to ground fault), the fault current will be 6-10 times that of the ordinary load current. Give us a chance to expect that the fault current is λ times more prominent than the load current in steady state. At the point when a short out fault happens, the secondary current is kλ times more noteworthy than that of the load current. The ratio of the series transformer is 8:1 in [15], while the ratio is decreased to 3.5:1 in this paper. The adjustment in the fault current at various transformer ratios is appeared in Fig. 3. The fault happens at tfault, and MCDVR goes into the current-liming mode at tlimit. ∆t is the fault recognition period. The secondary current Ifault_pre=8Il amid ∆t in [19], while Ifault_pre =3.5Il in this paper. Accordingly by diminishing the turns-ratio, the secondary side current amid the preparatory period of the fault (where the point of confinement module isn't in series with the line) can be lessened. In general, this will decrease the effect on the IGBTs and dc bus capacitor. After tlimit, the

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MCDVR enters the restricting mode and the fault current is constrained to the coveted esteem.

2) Fault-current limiting module design: When the MCDVR works in the fault current restricting mode, the fault current will flow through the series transformer T1, LC output filter, and the bidirectional thyristors. The series transformer withstands the supply voltage amid the faults, and henceforth the limit of the series transformer is

$$S_T \geq U_S I_{fault}. \quad (11)$$

In addition, the thermal stability of *Lf*, and the maximal withstand voltage of C*f* should be considered during the faults. This relation is expressed as:

$$Q_{Lf} \geq \int_{t\text{fault}}^{t\text{return}} (ki_{fault})^2 dt \quad (12)$$

Where, *QLf* is the thermal stability of *Lf* during the fault. *t*fault and *t*return are the time of the fault occurring and disappearing respectively. As the filter capacitor can be easily damaged by the overvoltage,

$$U_{Cf} \geq \max(u_{S\max}/k, u_{dc}) \quad (13)$$

Where *UCf* is the maximal withstand voltage of the filter capacitor. *u*dc and *u*Smax are the dc voltage and the maximum voltage across the series transformer respectively. [6] presented a brief outline on Electronic Devices and Circuits which forms the basis of the Clampers and Diodes.

When the thyristors are deactivated, the voltages between the thyristors are the same as the output voltage of the course converter. The maximum estimation of the output voltages is roughly equivalent to the DC side voltage, while the present flowing through the thyristors is zero. At the point when the thyristors are enacted amid the fault, the present flowing through the thyristor is k times of the fault current at the primary side. Consequently, the thyristors can be given by

$$Q_{\text{thy}} \geq \int_{t\text{fault}}^{t\text{return}} (ki_{fault})^2 dt \quad (14)$$

$$U_{\text{thy}} \geq \max(u_{cf}, u_{dc}) \quad (15)$$

Where *Q*thy is the thermal stability of the thyristors, and *U*thy is the maximal withstand voltage of the thyristors. Also, *ucf* is the voltage of the filtering capacitors and *ucf* = *us*/*k*.

3) Ride-through capability: Assuming that the magnitude of the voltage sag (with no phase-angle jump) is *U*sag in pu, the MCDVR should inject an active power given by

$$P_{\text{DVR}} = -C_{dc}u_{dc}du_{dc}/dt = \sqrt{3}U_L I_L \cos\varphi_L(1-U_{sag}) \quad (16)$$

to restore the pre-sag rated voltage *U*L at the load terminals [14]. Here, the load current *I*L and the power factor *φ*L are assumed to be constant. Furthermore, $P_L = \sqrt{3}\, U_L I_L \cos\varphi_L$ is the rated load power. If *t*sag is the voltage sag duration, the energy to be supplied by the MCDVR is

$$W_{\text{DVR}} = \int_{t_0}^{t_0+t_{sag}} (-C_{dc}u_{dc}\frac{du_{dc}}{dt})\,\text{dt} = \int_{t_0}^{t_0+t_{sag}} P_L(1-U_{sag})dt \quad (17)$$

then,

$$-C_{dc}[u_{dc}^2(t_0+t_{sag}) - u_{dc}^2(t_0)]/2 = P_L t_{sag}(1-U_{sag}). \quad (18)$$

If the initial dc-link voltage is assumed to be its rated value, then *u*dc(t0)=*U*dc0. Also, *u*dc(t0+tsag)=*k*d*U*dc0 where *k*d*U*dc0 is the minimum allowable dc-link voltage at the end of the voltage sag (0<*k*d<1). Thus, in order to compensate the maximum voltage sag magnitude for maximum expected sag duration *U*sag,max, the capacitance should be

$$C_{dc} \geq 2P_L t_{sag,\max}(1-U_{sag,\max})/U_{dc0}^2(1-k_d^2). \quad (19)$$

Expanding Udc0 permits the lessening of the size of the dc capacitor, yet the decision of that voltage likewise relies upon the maximum voltage rating of the H-bridge power electronic devices. Moreover, the capacitor voltage rating additionally constrains the maximum infusion voltage. Two adjusting plans are embraced [28], and are not talked about in this paper for curtness.

4) LC design: Despite the fact that the comparable switching frequency of the course multilevel inverter is high (e.g. 15kHz), there are a few higher harmonic components close to the proportional switching frequency. To constrict these components and successfully bring down the swell voltages and currents, a LC based filter is proposed. Setting the reverberation frequency of the filter as fc, at that

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point 2□ fc Lf □ 1/(2□ fc Cf). The comparable protection of the inverter on the dc link can be ascertained as takes after [29]

$$R_L = 3U_{dc}^2 / P_{DVR} \quad (20)$$

Hence, the resonance frequency is

$$f_c = 1/2\pi\sqrt{L_f C_f} = \sqrt{L_f / C_f}/2\pi L_f \quad (21)$$

In most engineering applications, a damping factor of = ρ (0.5 ~ 0.8)*RL* is present [15]. Assuming that the damping factor ρ = $\sqrt{(L_f / C_f)}$, then according to (20) and (21), *Lf* and C*f* can be calculated as

$$\begin{cases} L_f = \rho / 2\pi f_c \\ C_f = L / \rho^2 = 1/2\pi f_c \rho \end{cases} \quad (22)$$

The rated current in *Lf* is mainly determined by the fault current, which is described in detail in Section IV.

5) DC-link capacitor protection: Varistors are notable components regularly used to brace overvoltage transients [8]-[9], [30]-[31]. In this paper, varistors are intended to ensure the dc-link capacitor. In addition, the over-voltage security and under-voltage insurance of the dc-link capacitor are additionally connected in the product.

IV. TRANSIENT STATE ANALYSIS

A. From Compensation Mode to Current-Limiting Mode

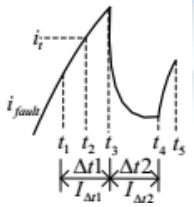

Fig. 4. The trend of the fault current during the forward switching scheme.

The forward switching plan (from the compensation mode to the present constraining mode) is to disconnect the VSI from substantial currents amid faults. The plan accomplishes this by quickly including constraining impedance in series with transmission line to restrict the short out current to the coveted esteem. As the plan includes the state changes of the multilevel inverters and thyristors, the forward switching sequence is given in Fig. 4.

At the point when a short out fault happens at t1, the line current increments quickly. Once the present size surpasses a preset edge it (which relies upon the transfer insurance) at t2, the IGBTs are killed to totally deactivate the inverter. Considering the detecting time of the fault identifier, the dead-time and non-perfect attributes of the switches, the IGBTs are really killed at t3. At that point, the control system gives a trigger signal to the thyristors at t4. Considering the non-perfect attributes of the thyristors, the way K through the thyristors is in conduction at t5. At that point, the forward switching is at long last finished.

(1) During Δt1, the fault current mainly relies upon the system impedance Zs, and the leakage impedance Zσ of the series transformer [30]. Subsequently,

$$I_{\Delta 1}(t) = U_s(t) / (|Z_s + Z_\sigma|). \quad (23)$$

From Fig.4, it is obvious that the fault current IΔt1 increments forcefully. The duration time Δt1 is critical to different devices and subsequently a quick fault current recognition technique is important.

(2) During Δt2, the MCDVR incorporates the supply power Us, the series transformer, and the filter capacitor Cf. The identical circuit is appeared in Fig. 5. Accordingly,

$$I_{\Delta 2}(t) = U_{\Delta 2}(t) / |Z_m| + U_{\Delta 2}(t) / |1/ j\omega C_f| \quad (24)$$

Where Zm>>Zσ, and Zσ is ignored. For the series transformer, the values of the excitation impedance Zm and 1/*j*ω*Cf* are large, and hence *I*Δt2 is much smaller than *I*Δt1.

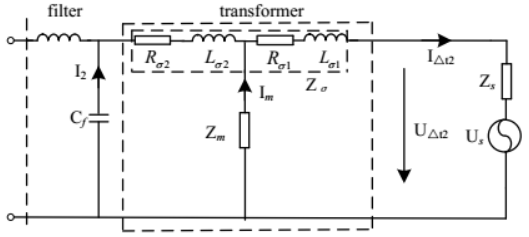

Fig. 5. Equivalent circuit of the MCDVR during Δt2.

(3) During the switching process of the thyristors, the fault current will increase. After the thyristors are activated, the fault current *I*fault is determined

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mainly by the limiting impedance Zlim, as given in (5). From (4) and (25), as Zlim is much smaller than Zm and 1/ $jC\omega f$, *I*fault is larger than $I\Delta t2$.

B. From Current-Limiting Mode to Compensation Mode

The regressive switching plan (from the present constraining mode to the pay mode) is to kill the thyristors after the fault. This plan includes the state changes of the multilevel inverters and the thyristors, and the regressive switching sequence is given in Fig. 6.

The short out fault vanishes at t6. In the event that the greatness of the load current is not as much as the arrival current rage at t7, the control system expels the trigger signal to the thyristors. rage is the reference estimation of the fault identification, and is bigger than the pinnacle estimation of the load current. At the point when the voltage over the thyristors is negative in extremity and the current is under the maintaining current, the thyristors are killed at t8. At that point, the majority of the IGBTs in the inverter are turned on at t9. Hence, the thyristors are as yet initiated for the period Δt3 (from t6 to t8) and are killed amid Δt4 (from t8 to t9).

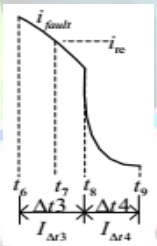

Fig. 6. The fault current during the backward switching scheme.

(1) During Δt3, the fault disappears. The equivalent circuit is shown in Fig. 7. It includes the power supply *U*s, the limiting modules, and the load Z*Load*. Ignoring Z*s* and Z*l*, the voltage across the current-limiting module is

$$U_{\Delta t3}(t) = U_s(t) - U_{Load}(t). \qquad (25)$$

As the leakage impedance Zσ is ignored,

$$I_{\Delta t3}(t) = U_{\Delta t3}(t) / (|Z_m // (1/ j\omega C_f) // j\omega L_f|). \qquad (26)$$

(2) During Δt4, the thyristors and the IGBTs also are turned off. The equivalent circuit of the system is shown in Fig. 8. It includes the supply power *U*s, the series transformer, and the load Z*Load*.

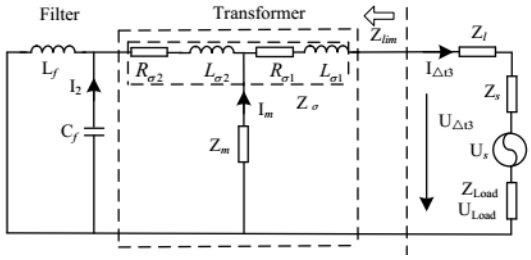

Fig. 7. Equivalent circuit of the MCDVR during Δt3.

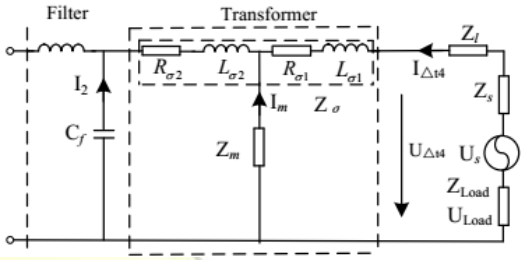

Fig. 8. Equivalent circuit of the forward switching sequence during Δt4.

Thus, the load current is

$$I_{\Delta t4}(t) = U_{\Delta t4}(t) / (|Z_m // (1/ j\omega C_f)|). \qquad (27)$$

From (26) and (27), because 1/ $jL\omega f$ is much smaller than *Zm* and 1/ $jC\omega f$, $I\Delta t3$ is larger than $I\Delta t4$. After the backward switching sequence, the line current will recover to the normal value.

V.SIMULATION RESULTS

To confirm the practicality of the MCDVR, simulations are run utilizing PSCAD/EMTDC programming. The system simulation display is appeared in Fig.1. The MCDVR is associated in series between the supply arrange and the ensured load. The relating parameter esteems utilized for the simulation are given in Appendix A. The supply voltage is thought to be 10kV and the source is accepted to have a reactance of 100ω. This compares to a fault level of 1MVA. In the simulations, while a seven-level course inverter is embraced, a few high-arrange harmonics are as yet exhibit close to the proportionate switching frequency. Thus, a LC filter ought to be considered in the cascaded H-bridge. On the off chance that a THD of 5% is considered as a limit for the load voltage, the proposed strategy can meet the prerequisite. Additionally, the seven-level course inverter can successfully ride-through both

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adjusted and uneven faults for voltage dips down to 80% at the converter terminals for 243 ms.

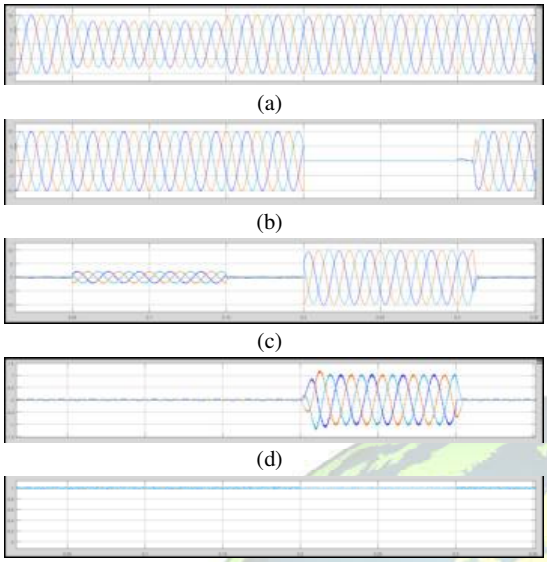


Fig. 9. Simulation results of the MCDVR system. Top to bottom: (a) the supply voltage Us, (b) the load voltage UL, (c) the secondary voltage Udvr, (d) the load current IL, and (e) the dc-link voltage.

Fig.9. demonstrates the execution of the MCDVR under voltage sags and faults. As appeared in Fig 9(a), voltage sag happens in the vicinity of 0.15s with a profundity of 20%. In Fig 9(b), it is observed that the load voltage UL is controlled to a constant amplitude amid this voltage sag.

The system is then subjected to a three-phase downstream fault by establishing the three-phase supply for 0.1s (i.e. five cycles). The load side voltage is about zero amid the fault (from 0.2s to 0.3s), as all the voltage would drop over the present restricting module as appeared in Fig. 9(b)- (c). The load current will be immediately constrained to the coveted an incentive because of the present restricting function as appeared in Fig. 9(d). In spite of the fact that the dc-link voltage drops somewhat at 0.2s, it comes back to its typical esteem instantly as appeared in Fig. 9(e).

A. Forward Switching Simulations

When the transient fault happens at t1=0.2s, the load current increments pointedly. The MCDVR goes into the present restricting mode before the amplitude of the fault current achieves its initially crest. The simulation results of the forward switching plan are appeared in Fig. 10. Considering the fault discovery defer time, the load current IL rises all of a sudden before t2 as appeared in Fig. 10(a). All the IGBTs are killed at t2. From Fig. 10(c), the output current Idvr of the VSI increments from t1 to t2. The control system gives trigger signals to the thyristors at t2. Amid t3<t<t5, the fault current is computed utilizing (24) and is little. After the thyristors are actuated at t5, the fault current is controlled by the present restricting module. In this way, when t1<t<t5, the output current of the VSI expands first before diminishing. Fig. 10(d) demonstrates that the dc-link voltage increments marginally amid the forward switching sequence.

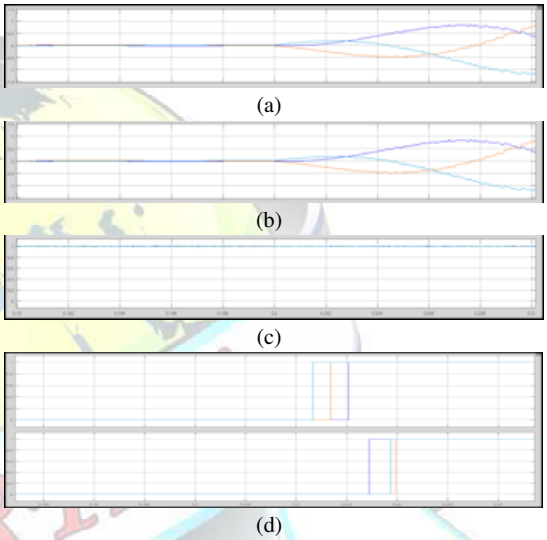
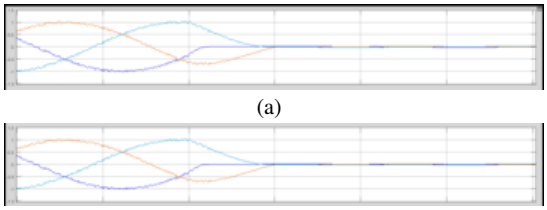


Fig. 10. Forward switching simulations of the MCDVR system, top to bottom: (a) the load current IL, (b) the current Iscr in the thyristor's path, (c) the dc-link voltage Udc, and (d) the timing sequence.

B. Backward Switching Simulations

Expecting that the transient fault is cleared at t6=0.3s, the MCDVR goes into the DVR mode and can accomplish the voltage controlling function amid sags. The simulation results of the regressive switching plan are appeared in Fig. 11. Considering the time taken to recognize that the fault has vanished, bolting signals are just given to the thyristors at t7 in the simulations.



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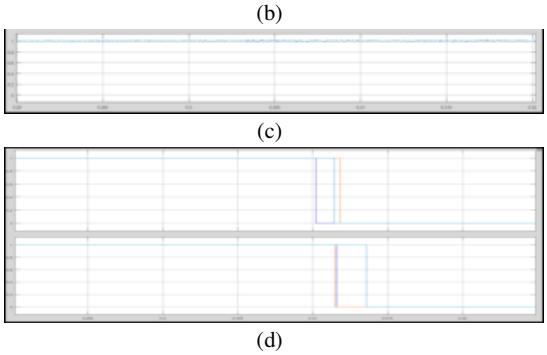

Fig. 11. Backward switching simulations of the MCDVR system, top to bottom: (a) the load current IL, (b) the current Iscr in the thyristor's path, (c) the dc-link voltage Udc, and (d) the timing sequence.

Because of the half-controlled normal for the thyristors, they are just killed totally at zero-intersection points. As talked about beforehand, the IGBTs are actuated at t8. In this way, when t8<t<t9, the output currents of the VSI are ascertained utilizing (27). Fig. 11(d) demonstrates that the dc-link voltage remains unaltered at 0.310s.

VI. CONCLUSIONS

Cascaded multilevel inverters have been connected in the business as a savvy means of series sag pay. In any case, a vast current will be drafted into the VSI through a series transformer amid faults, and this is unsafe to the VSI and the other gear in the grid. In this paper, the MCDVR was proposed to manage voltage sags and short out current faults. The MCDVR has not just the benefits of the H-bridge course inverter, yet additionally decreases the secondary side current in the preparatory period of the fault. A mathematical model of this system was likewise settled in this paper. A cautious investigation of the transient state checked the achievability of the proposed MCDVR. Based on the hypothetical examination, PSCAD/EMTDC simulations and the test results, we can finish up the accompanying:

1) The H-bridge course inverter can be received to lessen the series change ratio and the secondary current amid the preparatory period of the fault.

2) The transient state of the MCDVR system was presented in extraordinary detail.

3) The proposed control technique can confine fault current with two cycle. The textures between the simulation results and trial results help to check the proposed topology and hypothetical examination.

APPENDIX A

Source parameters: *U*s=10kV, Zs=1.21Ω, *f*0=50Hz.
Line: Zline=0.340Ω.
Load parameter: 1MW resistive Load
MFSC parameters: seven-level cascade inverter.
Switching frequency: 5 kHz.
DC link capacitor (per H-bridge module)
Cdc=10000μF.
LC filter inductor L*f*=2mH.
LC filter capacitor C*f*=15μF.
Series transformer ratio: 3.5:1.
Leakage reactance: 0.1p.u.
No load losses: 0.1 p.u.
Magnetizing current: 0.4%.

REFERENCES

[1] C.-S. Lam, M-C. Wong, and Y.-D. Han, "Voltage swell and overvoltage compensation with unidirectional power flow controlled dynamic voltage restorer," *IEEE Trans. Power Del.,* vol. 23, no. 4, pp. 2513-2521, Oct. 2008.

[2] M. Jafari, S. B. Naderi, M. Tarafdar Hagh, M. Abapour, and S. H. Hosseini, "Voltage sag compensation of point of common coupling (PCC) using fault current limiter," *IEEE Trans. Power Del.,* vol. 26, no. 4, pp. 2638-2646, Oct. 2011.

[3] F. Z. Peng and J. S. Lai, "A multilevel voltage-source converter with separate DC source for static var generation," *IEEE Trans. Ind. Applicat.,* vol. 32, no. 5, pp. 1130-1138, Sep./Oct. 1996.

[4] H. K. Al-Hadidi, A. M. Gole, and D. A. Jacobson, "Minimum power operation of cascade inverter-based dynamic voltage restorer," *IEEE Trans. Power Del.,* vol. 23, no. 2, pp. 889-898, Apr. 2008.

[5] D. M. Vilathgamuwa, A. A. D. R. Perera, and S. S. Choi, "Voltage sag compensation with energy optimized dynamic voltage restorer," *IEEE Trans. Power Del.*, vol. 18, no. 3, pp. 1603-1611, Oct. 2006.

[6] Christo Ananth, W.Stalin Jacob, P.Jenifer Darling Rosita. "A Brief Outline On ELECTRONIC DEVICES & CIRCUITS.", ACES Publishers, Tirunelveli, India, ISBN: 978-81-910-747-7-2, Volume 3,April 2016, pp:1-300.

[7] S. S. Choi, T. X. Wang, and D. M. Vilathgamuwa, "A series compensator with fault

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

current limiting function," *IEEE Trans. Power Del.*, vol. 20, no. 3, pp. 2248-2256, Jul. 2005.

[8] L. A. Moran, I. Pastorini, J. Dixon, and R. Wallace, "A fault protection scheme for series active power filters," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 928-938, Sep. 1999.

[9] I. Axente, M. Basu, M. F. Conlon, and K. Gaughan, "Protection of unified power quality conditioner against the load side short circuits," *IET Power Electron.*, vol. 3, no. 4, pp. 542-551, Aug. 2010.

[10] S. B. Naderi, M. Jafari, and M. T. Hagh, "Parallel-resonance-type fault current limiter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2538-2546, Jul. 2013.

[11] W. Fei, Y. Zhang, and Z. Y. Lu, "Novel bridge-type FCL based on self-turnoff devices for three-phase power systems," *IEEE Trans. Power Del.*, vol. 23, no. 4, pp. 2068-2078, Oct. 2008.

[12] H. K. Al-Hadidi, A. M. Gole, and D. A. Jacobson, "A novel configuration for a cascade inverter-based dynamic voltage restorer with reduced energy storage requirements," *IEEE Trans. Power Del.*, vol. 23, no. 2, pp. 881-888, Apr. 2008.

[13] F. M. Mahdianpoor, R. A. Hooshmand, and M. Ataei., "A new approach to multifunctional dynamic voltage restorer implementation for emergency control in distribution systems," *IEEE Trans. Power Delive.*, vol. 26, no. 2, pp. 882-890, Apr. 2011.

[14] D. Bruno, F. Federica, and P. Renato, "An effective SSC control scheme for voltage sag compensation," *IEEE Trans. Power Del.,* vol. 20, no. 3, pp. 2100-2107, Jul. 2005.

[15] Z. Shuai, P. Yao, Z. J. Shen, C. Tu, F. Jiang, and Y. Cheng, "Design considerations of a fault current limiting dynamic voltage restorer (FCL-DVR)," *IEEE Trans. Smart Grid,* vol. 6, no. 1, pp. 14-25, Jan. 2015.

[16] P. C. Loh, D. M. Vilathgamuwa, S. K. Tang, and H. L. Long, "Multilevel dynamic voltage restorer," *IEEE Trans. Power Del.*, vol. 2, no. 4, pp. 125-130, Dec. 2004.

[17] E. Babaei, M. F. Kangarlu, and M. Sabahi, "Dynamic voltage restorer based on multilevel inverter with adjustable dc-link voltage," *IET Power Electron.*, vol. 7, no. 3, pp. 576-590, Aug. 2014.

[18] A. M. Massound, S. Ahmed, P. N. Enjeti, and B. W. Williams, "Evaluation of a multilevel cascaded-type dynamic voltage restorer employing discontinuous space vector modulation," *IEEE Trans. Indust. Electron.,* vol. 57, no. 7, pp. 2398-2410, July. 2010.

[19] A. J. Visser, J. H. R. Enslin, and H. du. and T. Mouton, "Transformerless series sag compensation with a cascaded multilevel inverter," *IEEE Trans. Indust. Electron.*, vol. 49, no. 4, pp. 824-831, Aug. 2002.

[20] C. L. Poh, D. G. Holmes, and T. A. Lipo, "Implementation and control of distributed PWM cascaded multilevel inverters with minimal harmonic distortion and common-mode voltage," *IEEE Trans. Power Electron.*, vol. 20, no.1, pp. 90-99, Jan. 2005.

[21] B. Wang, G. Venkataramanan, and M. Illindala. "Operation and control of a dynamic voltage restorer using transformer coupled H-bridge converters," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1053-1061, Jul. 2006.

[22] S. Pengwei, C. C. Liang, L. Jih-sheng, and L. Chuang, "Cascade dual-buck full bridge inverter with hybrid PWM technique," in Proc. 2012 17th Annual APEC, Orlando, FL, 2012, pp. 113-119.

[23] A. K. Panda, and Y. Suresh, "Performance of cascaded multilevel inverter by employing single and three-phase transformer," *IET Power Electronics*, vol. 5, no. 9, pp.1697-1705, Aug. 2012.

[24] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverter," *IEEE Trans. on industry. Electri.*, vol. 57, no. 7, pp. 2197-130, Dec. 2010.

[25] J. Rodriguez, S. Bernet, Wu Bin, J. O. Pontt. and S. Kouro., "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Indust. Electron.,* vol. 54, no. 6, pp. 2930-2945,Dec. 2007.

[26] S. R. Mohanty, A. K. Pradhan, and A. Routray, "A cumulative sum-based fault detector for power system relaying application," *IEEE Trans. Power Del.*, vol. 23, no. 1, pp. 79-86, Jan. 2008.

[27] Y. Y. Xie, K. Tekletsadik, D. Hazelton, and V. Salvamanickam, "Second generation high-temperature superconducting wires for fault current limiter application," *IEEE Trans. Appli. Super conduct.*, vol. 17, no. 2, pp. 1981-1985, Jun. 2007.

[28] M. Zygmanowski, B. Grzesik, and J. Michalak, "Power conditioning system with cascaded H-bridge multilevel converter-DC-link voltage balancing method," European Conference on EPE, Birmingham, FL, Aug., 2011, pp. 1-10.

[29] K. Hyosung, K. J. Hwan, and S. S. Ki, "A design consideration of output filters for dynamic

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

voltage restorers," in Proc. IEEE Power Electronics Specialists Conference, Aachen, Germany, 2004, pp. 4268-4272.
[30] I. Jun-ichi, A. Wataru, T. C. Goh, and T. Akio, "Suppression method of rising DC voltage for the halt sequence of an inverter in the motor regeneration," in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), Denver, CO, 2013, pp. 15-19.
[31] J. N. Michael, and H. G. Donald, "An integrated approach for the protection of series injection inverters," *IEEE Trans. Ind. Applicat.*, vol. 38, no. 3, pp. 679-687, May/Jun. 202.
[32] Y. W. Li, D. M. Vilathgamuwa, P. C. Loh, and F. Blaabjerg, "A dual-functional medium voltage level DVR to limit downstream fault currents," *IEEE Trans. Power Electron.,* vol. 22, no. 4, pp. 1330-1340, July 2007.

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