ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

A step size error cancellation in self-charging algorithm for DC link voltage control in shunt active power filter

K. BALAKRISHNA,
M.Tech, TUDI NARASIMHA REDDY INSTITUTE OF TECHNOLOGY & SCIENCES, GUDUR, BIBINAGAR, YADADRIBHONGIRI, TELANGANA.
Mrs. N. MANASA,
Assistant professor, TUDI NARASIMHA REDDY INSTITUTE OF TECHNOLOGY & SCIENCES, GUDUR, BIBINAGAR, YADADRIBHONGIRI, TELANGANA.

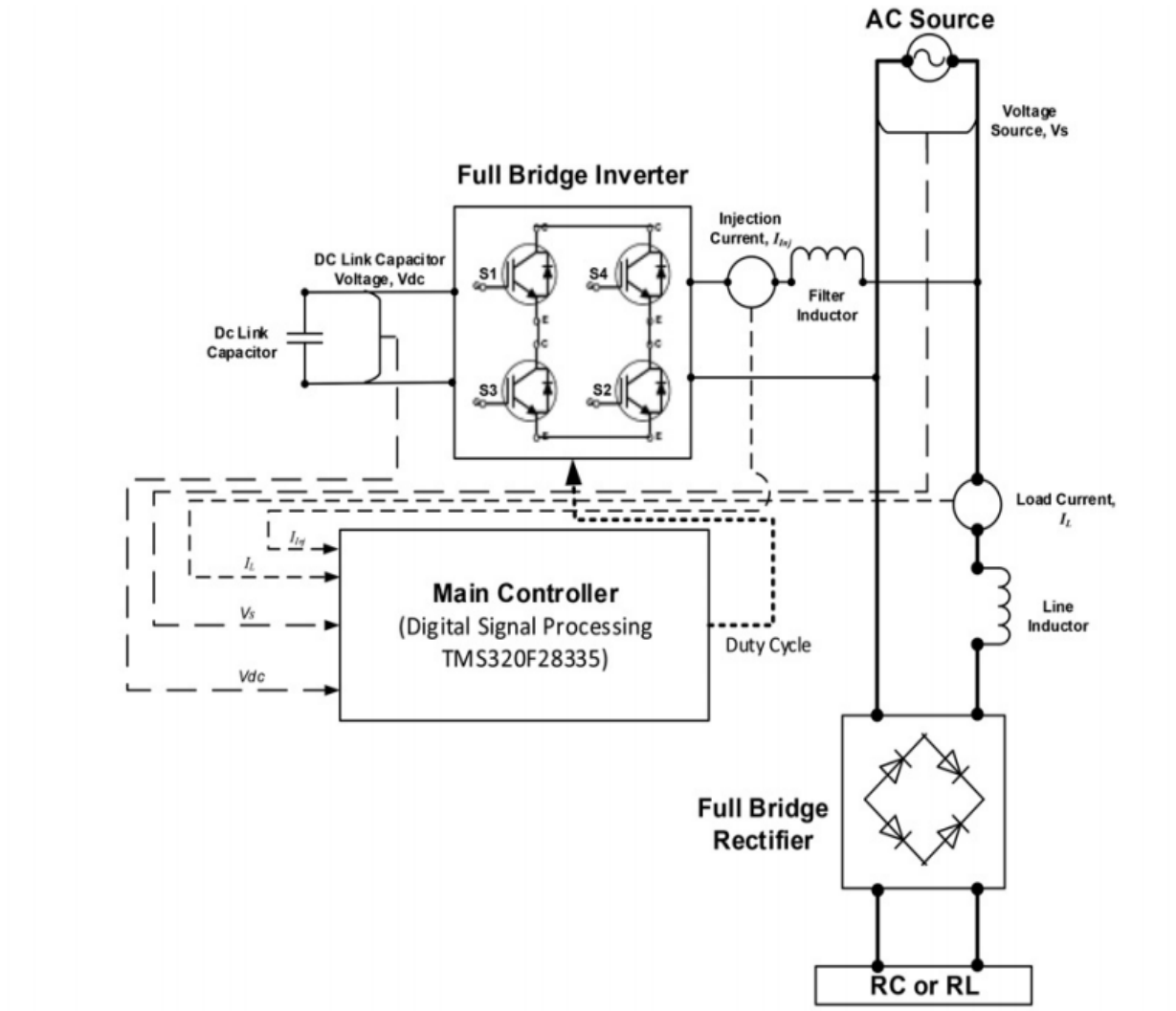
***Abstract*: This paper exhibits an improved self-charging calculation by presenting another element known as step size blunder cancelation for better execution of DC-link capacitor voltage control in single-phase shunt active power filter (SAPF). Past works of self-charging calculations were centered just for steady-state operation by utilizing either proportional– basic (PI) or fuzzy logic control (FLC). Nonetheless, in a specific operation of any power system, dynamic operation may likewise happen. In this manner, by presenting step size blunder cancelation as an extra element to the self-charging calculation, both steady state and dynamic operations can be secured. For assessment and examination investigation, self-accusing of PI and FLC calculations have been produced as well. Every one of the calculations were mimicked in MATLAB– Simulink, separately, together with the single-phase SAPF. The other two conventional self-charging calculations were additionally customized for correlation purposes. From the results and investigation, the proposed self-accusing of step size blunder cancelation demonstrates the best execution with high precision, quick reaction time and less overshoot and undershoot. It performs well in both steady state and dynamic operations as contrasted and both past self-charging strategies which just function admirably in steady-state operation.**

I. INTRODUCTION

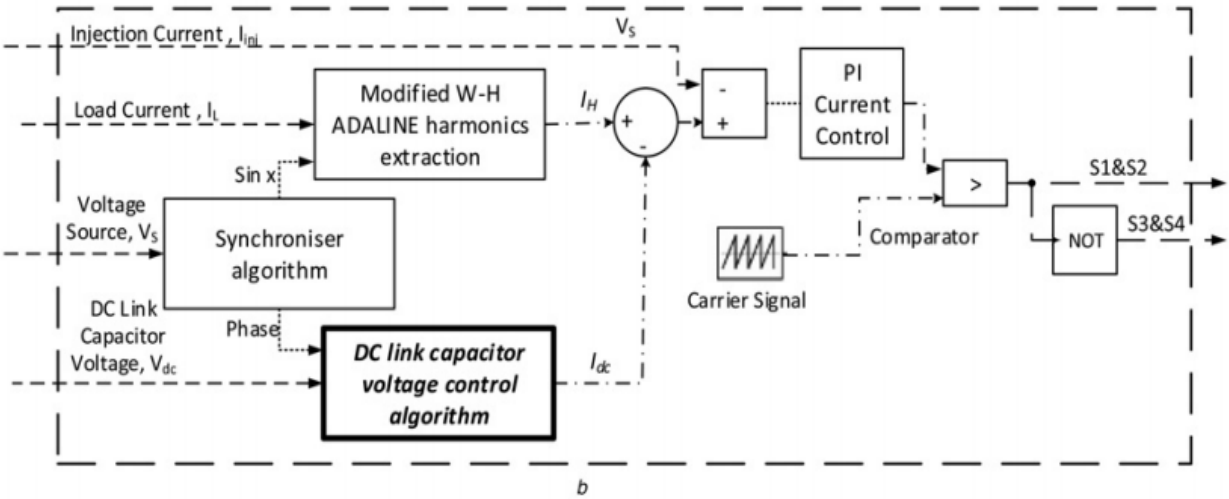
Power quality is characterized as wide assortment of electromagnetic marvels that describes the voltage and current at a given time and at a given area in the power system [1]. Conceivable power issues showed in voltage, current or frequency deviations, that reason disappointment or disoperation of client hardware, are considered as power quality issues [2]. Power quality issues are arranged as transients, voltage varieties, harmonics, inter-harmonics, flicker, and voltage awkwardness and frequency deviation [2, 3]. Harmonics are the main power quality issues in power system which can be alleviated by utilizing active power filter (APF). Harmonics can be sorted into voltage and current harmonics. Current harmonics are caused by nonlinear load operations created by power electronic devices and applications infused into the supply arrange through point of regular coupling [4]. The real disadvantages of current harmonics are capacitor blowing, hardware overheating, engine vibration and unnecessary nonpartisan currents [5]. To alleviate the present harmonics, shunt active power filter (SAPF) is utilized as opposed to series APF which mitigates voltage harmonics.

In SAPF, inverse heading of harmonic current is infused to the power system to guarantee sinusoidal shape at the fundamental frequency of the source current. Built up topology for single-phase SAPF is by utilizing full-bridge inverter where it comprises of four switching devices and a capacitor named as DC-link capacitor. The main function of DC-link capacitor is to go about as a constant DC storage for the inverter to deliver the infusion current (moderation current) to the source current. The conventional strategy to control DC-link capacitor voltage is by utilizing direct change between instantaneous voltage and wanted DC-link voltage. In any case, by utilizing this strategy, the DC-link capacitor voltage isn't precisely controlled and directed, and accordingly, unclean voltage is created [6– 14]. This real disservice adds to various impacts, for example, capacitor blowing and high total harmonic distortion (THD) because of flimsy infusion current [6].

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017



a



b

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

Fig.1: Single-phase SAPF (a) Circuit diagram (b).Control Strategies.

Control the charging and releasing of the DC-link capacitor as contrasted and the conventional calculation which just expect the distinction between wanted voltage and next charge voltage of DC-link--capacitor as the main parameter for controlling the capacitor voltage. [7] presented a brief outline on Electronic Devices and Circuits which forms the basis of the Clampers and Diodes.

Proportional integral (PI) [15–19] and fuzzy logic control (FLC) [20] are among the existing control techniques to control the voltage error produced from the self-charging algorithm. Self-charging with PI algorithm is popular as it is considered simple; however, it has some drawbacks, such as

† Fluctuation and imbalance of the DC-link voltage.
† Large overshoot and slow response [9].
† Existing of ripples, noise and spikes in the regulated DC-link voltage [11, 12].
† Unsatisfactory performance under parameter variations, nonlinearity and load disturbances; it only works in steady-state operation [13, 14].

PI is likewise difficult to be tuned and planned particularly by including SAPF, on the grounds that it needs exact mathematical model to get the additions for corresponding kp and basic ki. As an option, with high development of artificial keen strategies, FLC as one of them has much better execution, for example, significantly quicker, precise and exceptionally steady, and it functions admirably with complex system [21– 25]. FLC procedure does not require particular and exact mathematical models for planning and tuning, and it functions admirably utilizing uncertain data sources, viably handles non-linearity system and, is more robust and less complex than the PI method [21– 23]. It is additionally self-acting component and works as indicated by an arrangement of straightforward and meaningful etymological (if– at that point) rules [24, 25].

Despite the fact that FLC procedure is vastly improved than PI method, them two have same real downsides where their operations did not consider parameter variables, nonlinearity and load unsettling influences; the past works just considered the steady state operation and no further examination have been finished with dynamic operation [17– 20]. Dynamic operation dependably occurs in the power system, and particularly for DC-link capacitor, it might blow when over voltage happens, and conceivable disoperation of infusion current happens when under voltage happens. At whatever point there is an adjustment in the load, the voltage over the DC-link capacitor likewise experiences a relating change [10]. Particularly for the self-charging calculation, the current approach is utilizing PI or FLC to control the voltage blunder specifically, in this way prompts conceivable aggravation towards learning reaction of the calculation. By controlling the voltage blunder, which is an immediate control approach (main control signal), there is no such adaptability where either the voltage mistake changes or not, despite everything it must be prepared and controlled.

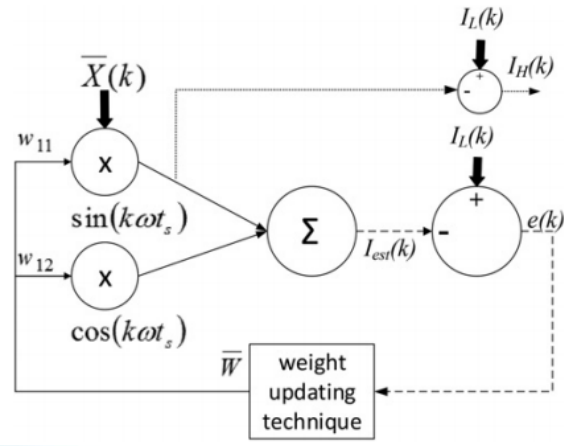


Fig. 2 Modified W–H ADALINE algorithm.

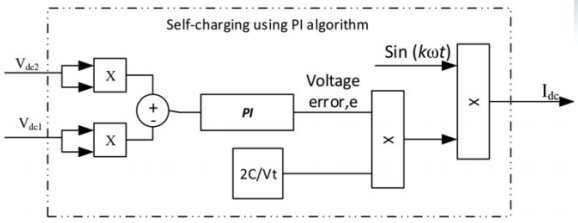
Consequently, this paper displays a work on enhancing self-charging calculation which ought to have the capacity to expand execution by controlling the DC-link capacitor in steady state and dynamic operations. By presenting extra element known as the step size mistake cancelation into the self-charging calculation, it ought to have the capacity to deal with steady state and dynamic operations. The proposed self-charging calculation is assessed and contrasted

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

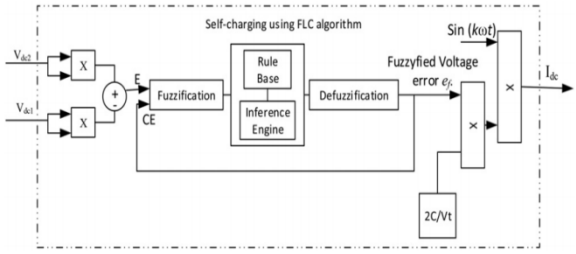
and both existing self-accusing of PI and FLC calculations. To additionally clarify about this work, Section 2 in this paper covers the proposed single-phase SAPF, Section 3 covers the harmonics extraction utilized as a part of the SAPF and took after by talk on self-accusing calculation of PI and FLC, and further improvements made to it in Section 4. Simulation work and equipment execution including the results are talked about in Sections 5, 6, individually. At last, Section 7 finishes up discoveries from this work.

II. SINGLE-PHASE SAPF

Fig. 1 demonstrates the general SAPF which contains full bridge inverter, DC-link capacitor and controller. The wellspring of harmonics is from rectifier-based circuit which produces one of the most elevated harmonics in electrical system [26– 28]. It is associated with two sorts of non-linear loads: inductive and capacitive. The SAPF's control techniques comprise of harmonics extraction calculation, DC-link capacitor voltage control calculation, synchronizer, current control calculation and switching calculation. In this paper, the featured calculation is the DC-link capacitor voltage control calculation. For harmonics extraction, altered Widrow– Hoff (W– H) ADALINE calculation is utilized [29– 35]; meanwhile, for current control calculation, PI method is utilized [29, 30, 34]. A synchronizer is utilized to create reference sinusoidal signal, and meanwhile, pulse-width tweak procedure is utilized for switching calculation. As specified in the introduction, DC-link capacitor voltage control is one of the main control systems in SAPF.



(a)



(b)

Fig.3: Self-charging technique using (a) PI algorithm (b) FLC algorithm.

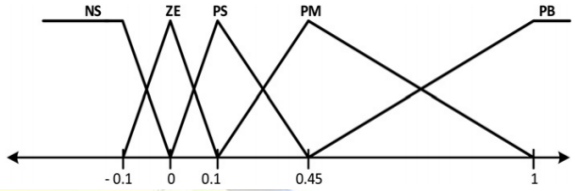


Fig. 4 Membership functions for E, CE and ef.

A decent DC-link capacitor voltage must be over than two-third of the grid voltage so as to ensure that an appropriate infusion current will be produced. Least capacitance estimation of the capacitor can be resolved as underneath [36, 37]

$$C \geq \frac{\max\left|\int_0^t I_{inj}(t)\right|}{\Delta V_{C\max}} \qquad (1)$$

Where Iinj represents the injection current and ΔVCmax represents the maximum ripple voltage of the DC-link capacitor.

III. HARMONICS EXTRACTION

Harmonics extraction utilizing ADALINE calculation performs by utilizing the principle of sine and cosine components (periodic signal) based on the idea of assessing harmonic components that exist in the electrical system. Fundamental component and harmonic components are spoken to by the non-linear load current IL for each example k and test period ts in computerized operation with appointed fundamental frequency ω [29– 35]. The non-linear load current can be spoken to as underneath

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

$$I_L(k) = \sum_{n=1,2...}^{N} \left[W_{an} \sin(nk\omega t_s) - W_{bn} \cos(nk\omega t_s)\right] \quad (2)$$

Where, Wan and Wbn are amplitudes of the sine and cosine components of the load current, n is the order of the harmonic to N maximum order. Equation (2) can be arranged to vector form as follows

$$\overline{I_L}(k) = \overline{W}^T \overline{X}(k) \quad (3)$$

Where the weight matrix is W^T = [w11w21, . . . , wanwbn] and X represents the sine and cosine vector as

$$\overline{X} = \begin{bmatrix} \sin(k\omega t_s) \\ \cos(k\omega t_s) \\ . \\ . \\ \sin(nk\omega t_s) \\ \cos(nk\omega t_s) \end{bmatrix}$$

The algorithm is used to train equivalent value of IL(k). The main feature of this extraction algorithm is the weights updating technique where the W–H method is used [29–35]. Injection current Iinj is used to compensate harmonic distortion, which is direct opposite polarity to harmonic current IH, as shown in Fig. 2.

Table 1 Rule-base for self-charging with FLC algorithm [20]

CE\E	NS	ZE	PS	PM	PB
NS	NS	NS	ZE	PS	PM
ZE	NS	ZE	PS	PM	PB
PS	ZE	PS	PM	PB	PB

One of the improvements made in adjusted W– H ADALINE is it utilizes just the principal request of harmonic components as opposed to n number of harmonic components as in typical W– H ADALINE.

By utilizing this calculation, it has beaten issue of the conventional W– H ADALINE calculation where number of weights n must be refreshed which requires longer reaction time [35]. It needs just to refresh the two weights of the fundamental component, making it is autonomous of number of harmonic requests. This improvement is based on the mathematical relationship of the components being orthogonal to each other. With this change, the iteration speed is enormously upgraded, bringing about quicker estimation. In any case, refreshing just the two weights results in a huge normal square mistake e, and subsequently learning rate α must be included as in (4) [35]

$$\overline{W}(k+1) = \overline{W}(k) + \frac{\alpha e(k)\overline{Y}(k)}{\overline{Y}^T(k)\overline{Y}(k)} \quad (4)$$

Where

$$\overline{W} = \begin{bmatrix} w_{11} \\ w_{21} \end{bmatrix}, \quad \overline{Y} = \begin{bmatrix} \sin(k\omega t_s) \\ \cos(k\omega t_s) \end{bmatrix}$$

and α is learning rate. Suitable learning rate is important as it will help the algorithm to optimally produce the accurate fundamental of harmonic current. The harmonic current IH(k) can be produced from load current deduction (from load current's fundamental sine part) as in (5) [30]

$$I_H(k) = I_L(k) - W \sin(k\omega t_s) \quad (5)$$

IV. DC-LINK CAPACITOR VOLTAGE CONTROL

4.1 Self-charging with PI and FLC algorithms

An extra genuine power must be attracted to manage the DC-link capacitor voltage from the supply side or the grid to charge the capacitor. Amid the charging procedure, voltage of the DC-link capacitor dependably transforms from the coveted voltage which adds to contrast in energy put away in the DC-link capacitor itself. Accordingly, the distinction in energy put away ΔE in the DC-link capacitor is spoken to as beneath

$$\Delta E = \frac{C}{2}\left[(V_{dc2})^2 - (V_{dc1})^2\right] \quad (6)$$

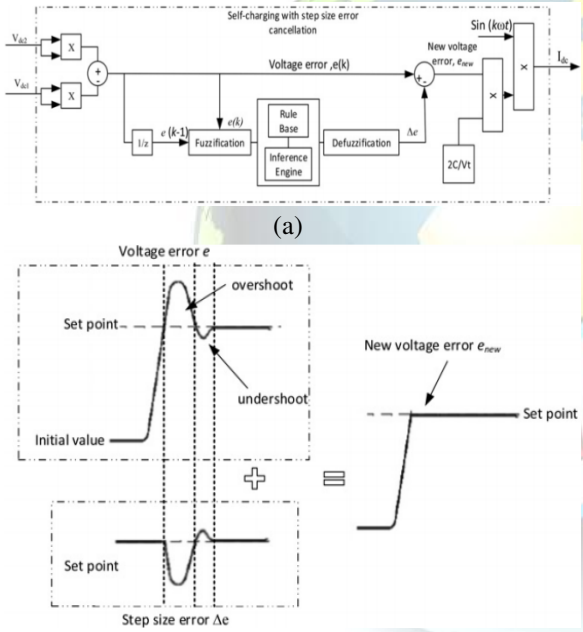
Where C is the capacitance value of the DC-link capacitor, Vdc1 is the desired voltage of the DC-link capacitor and Vdc2 is the instantaneous voltage of the DC-link capacitor. On the other hand, the

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

charging energy delivered by single-phase AC system Eac for the capacitor is

$$E_{ac} = Pt_c$$
$$E_{ac} = V_{rms} I_{dc,rms} \cos\theta t_c \quad (7)$$

Where P is the additional real power required, tc is the charging time of the capacitor, Vrms is the rms value of the supply voltage, Idc, rms is the rms value of the charging capacitor current Idc and θ is the difference of phase angle between supply voltage and charging capacitor current. However, tc can be defined as T/2 since the charging process only takes half of a cycle for the capacitor, where T is the period of the supply frequency, which is 50 Hz.



(a)

(b)

Fig. 5 Self-charging with step size error cancellation (a) Block diagram (b) Conceptual operation.

Table 2 Rule-base for self-charging with step size error cancellation

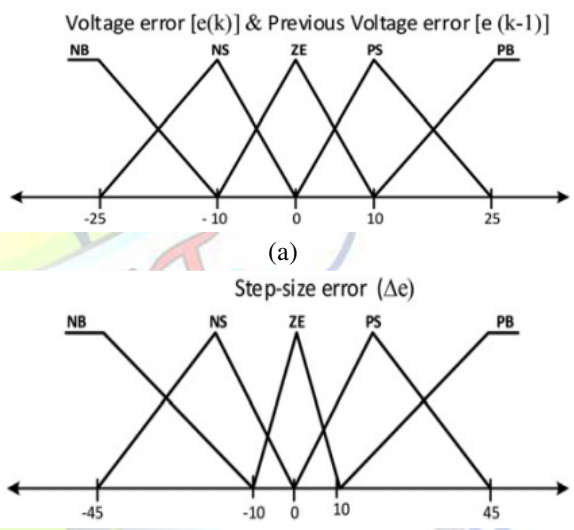
e\e(k – 1)	NS	ZE	PS	PM	PB
NB	ZE	NS	NB	NB	NB
NS	PS	ZE	NS	NB	NB
ZE	PB	PS	ZE	NS	NB
PS	PB	PB	PS	ZE	NS
PB	PB	PB	PB	PS	ZE

Vrms and Idc, rms can be expressed in peak values as below

$$\therefore E_{ac} = \frac{V}{\sqrt{2}} \frac{I_{dc}}{\sqrt{2}} \frac{T}{2}$$
$$E_{ac} = \frac{V I_{dc} T}{4} \quad (8)$$

By neglecting the switching losses in the inverter and according to the energy conservation law, the following equation holds:

$$\Delta E = E_{ac}$$
$$\frac{C}{2}\left[(V_{dc2})^2 - (V_{dc1})^2\right] = \frac{V I_{dc} T}{4} \quad (9)$$
$$\therefore I_{dc} = \frac{2C\left[(V_{dc2})^2 - (V_{dc1})^2\right]}{VT}$$



(a)

(b)

Fig. 6: Membership functions for the change of voltage error (a) previous voltage error (b) step size error.

Voltage error e is defined as

$$e = (V_{dc2})^2 - (V_{dc1})^2 \quad (10)$$

The voltage error e in the self-charging calculation gives the most astounding impact towards assurance of DC-link capacitor charging current Idc. The DC-link capacitor voltage calculation is wanted to control the revive rate by controlling the Idc (allude to Fig. 1b). As said in the introduction, PI was broadly used

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

in DC-link capacitor voltage control. Fig. 3a demonstrates block diagram of self-accusing of PI calculation. The base estimations of parameters for PI procedure can decided as beneath [11]

$$k_p \geq 2C\xi\omega \quad (11)$$

$$k_i \geq C\omega \quad (12)$$

Where ki represents integral gain, kp represents proportional gain, C represents the capacitance value of the DC-link capacitor, j represents damping factor which is usually 0.707 and ω represents the angular frequency.

The self-charging of FLC calculation is appeared in Fig. 3b. FLC is partitioned into four classifications, which incorporate fuzzification, fuzzy inference, rule-base and defuzzification. Amid fuzzification, the numerical information variables are changed over into phonetic variables based on the membership functions. Different fuzzy levels could be utilized for info and output variables. The self-accusing of FLC calculation utilizes error E and change in error CE as contributions with test time k, as appeared in (13) and (14); while the output of FLC calculation is the fuzzified voltage error ef.

$$E(k) = (V_{dc2})^2 - (V_{dc1})^2 \quad (13)$$

$$CE(k) = e_f(k) \quad (14)$$

After E and CE are acquired, these data sources are changed over into semantic variables and after that the fuzzy output is produced by turning upward in a rule-base table. The FLC calculation is based on ace rule of 'If X and Y, Then Z'. To decide the output of the fuzzy logic, the fuzzy inference is utilized. The strategy for inference is Mamdani [38]. More often than not, weights are added to the rules to enhance thinking exactness and to decrease unfortunate ensuing. The fuzzy output is changed over back to numerical variable from etymological variable amid defuzzification. The most well-known technique utilized for this defuzzification is the centroid of region since it has great averaging properties and more precise results can be delivered [39]. The membership functions in the self-accusing of FLC calculation are appeared in Fig. 4 and the rule-base is appeared in Table 1.

4.2 Self-charging with step size error cancellation

In order to address dynamic operation, an improvement to the self-charging algorithm is carried out by introducing step size error cancellation as shown below

$$e_{new} = e + \Delta e$$
$$e_{new} = \left[(V_{dc2})^2 - (V_{dc1})^2\right] + \Delta e \quad (15)$$

Where e_{new} is the new voltage error, e is the voltage error as in (10) and Δe is the proposed step size error. Thus, the new charging current Idc is

$$\therefore I_{dc} = \frac{2C\left[\left[(V_{dc2})^2 - (V_{dc1})^2\right] + \Delta e\right]}{VT} \quad (16)$$

When the capacitor voltage is controlled at wanted set point, the charging DC-link capacitor current Idc must be or practically equivalents to zero. As opposed to specifically control the voltage error, step size error cancelation is included the self-charging calculation as appeared in Fig. 5a. Its main function is to give adaptability for the calculation to drop any difference in voltage error as far as overshoot and undershoot. There will be no unsettling influence happens straightforwardly since the self-accusing of step size error cancelation calculation gives elective way to control the voltage error, instead of the self-accusing of PI and FLC calculations which specifically control the voltage error.

This change adds to quick reaction and improved execution. In the event that any overshoot or undershoot happens to the voltage error, the improved self-charging will drop all overshoot and undershoot and specifically influence them to equivalent to zero. On the off chance that overshoot happens, at that point Δe will be negative, and meanwhile, when undershoot happens, Δe will be positive; both to counter back the overshoot and undershoot of the voltage error. The step size error

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

will just give impact towards the condition if any overshoot or undershoot happens to the voltage error particularly after the capacitor voltage achieves the coveted voltage. To control Δe, FLC procedure is picked as its solid favorable circumstances over PI strategy are obviously specified before. FLC is utilized to control the step size on the grounds that the cancelation must be exact and precise to get the coveted results.

A few adjustments have been made to advance the FLC strategy, which include fuzzification sources of info and number of fuzzy rules. Existing self-accusing of FLC calculation utilizes E and CE as the main contributions for fuzzification, yet for the self-accusing of step size error cancelation, the fuzzification inputs are set to voltage error e(k) and past voltage error e(k – 1). Fig. 6 demonstrates the membership functions of the FLC procedure and Table 2 demonstrates the rule-base; both for the self-accusing of step size error cancelation. The mappings of the membership functions are made based on open-circle genuine information of the voltage error e.

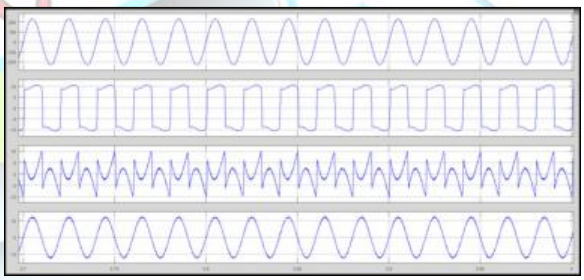
V. SIMULATION RESULTS

The proposed single-phase SAPF was associated with the proving ground which comprises of supply grid source and non-linear loads. Two sorts of non-linear loads were produced by utilizing a diode H-bridge rectifier with 470 µF capacitor and 50 Ω resistors (capacitive) associated in parallel as the first, and meanwhile 160 mH inductor and 15 Ω resistor (inductive) associated in series for the second one. Simulation works were done under steady state and dynamic operations utilizing the self-accusing of step size error cancelation as the proposed DC-link capacitor voltage control. Also, for examination reason, the self-accusing of PI calculation and the self-accusing of FLC calculation were utilized as well. The examining time for simulation was set to 150 µs. Table 3 indicates parameters and components for single-phase SAPF, and meanwhile, Table 4 gives the noteworthy parameters their setting esteems utilized as a part of these three self-charging calculations.

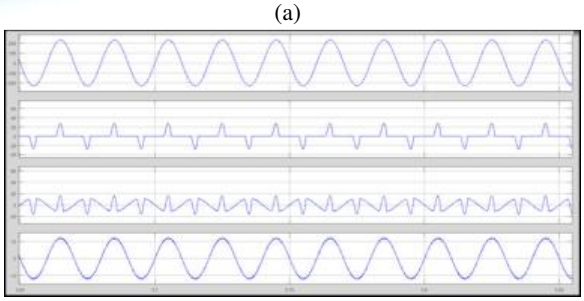
The main vital factors used to investigate execution for every DC-link capacitor voltage control calculation is level of exactness, overshoot, undershoot and reaction time. The level of exactness PA is alluded to the ratio of the normal output of DC-link capacitor voltage Vdc, normal with the coveted DC-link capacitor voltage Vdc, wanted, as demonstrated as follows

$$\therefore PA = \frac{V_{\text{dc,average}}}{V_{\text{dc,desired}}} \times 100 \qquad (17)$$

For exhibitions in identified with reaction time, overshoot and undershoot, dynamic operations through load change tests were done when the progressions were performed from capacitive to inductive and from inductive to capacitive, individually. Fig. 7 demonstrates the simulation aftereffect of SAPF which covers source voltage Vs, load current IL, infusion current Iinj and source current Is, for both inductive and capacitive loads. From Fig. 7, the source current is legitimately remunerated and the harmonics are evacuated which coming about THDs of 2% for the inductive load and 3.13% for the capacitive load; both are underneath 5%, as to take after IEEE Standard 519 2014: IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems [1].



(a)



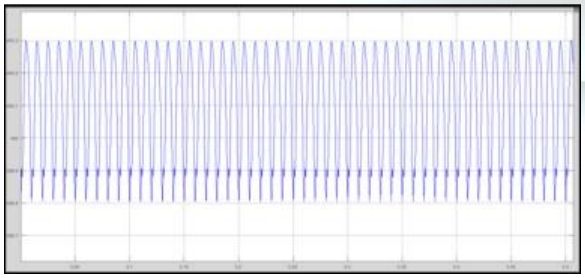
(b)

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

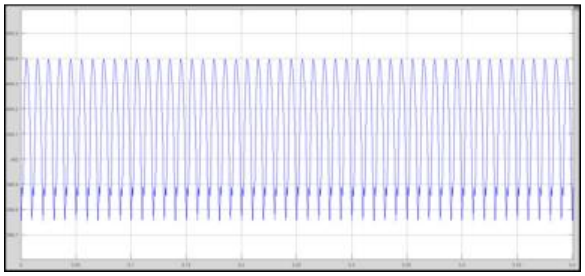
Fig. 7: Simulation result of SAPF which covers source voltage Vs, load current IL, injection current Iinj and source current Is, for a Inductive load b Capacitive load.

5.1 Steady-state operation

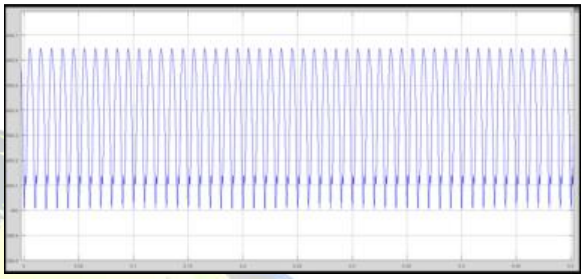
Exhibitions of every DC-link capacitor voltage control calculation for inductive and capacitive loads are appeared in Figs. 8 and 9, individually. All self charging calculations control the DC-link capacitor voltage well, however their rates of precision are extraordinary. Among them, the proposed calculation produces 100% precision of the managed DC-link capacitor voltage for both non-linear loads. The self accusing of FLC calculation meanwhile delivers smidgen higher directed voltages with 0.1 V (99.97% precision) and 0.2 V (99.95% exactness) over the coveted voltage for inductive and capacitive loads, individually. Meanwhile, the self-accusing of PI calculation demonstrates the most exceedingly terrible managed voltages by delivering 0.3 V (99.92% exactness) and 0.5 V (99.87% precision) over the coveted voltage for inductive and capacitive loads, individually. From the simulation in steady-state operation, all the self accusing calculations perform of high precision of DC-link capacitor voltage; in any case, among them, the proposed self-charging calculation demonstrates the most astounding exactness which is around 0.3– 0.13% superior to anything the current self-charging calculations.



(a)

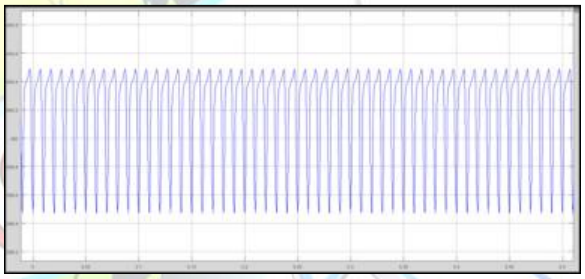


(b)

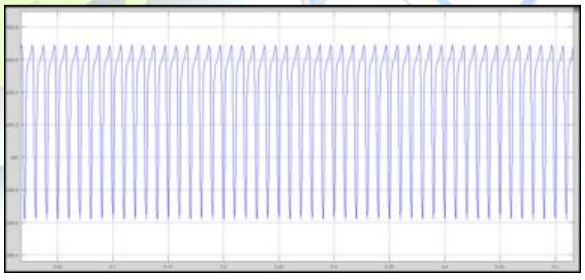


(c)

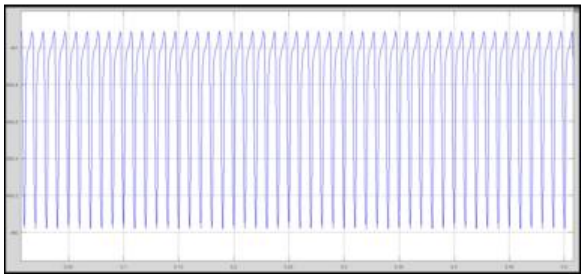
Fig. 8: Performance of DC-link voltage control algorithms for inductive load with the desired voltage of 400 V.



(a)



(b)



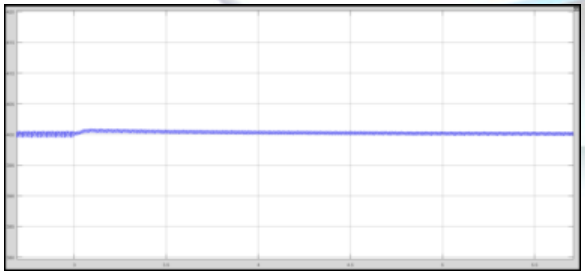
ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

(c)

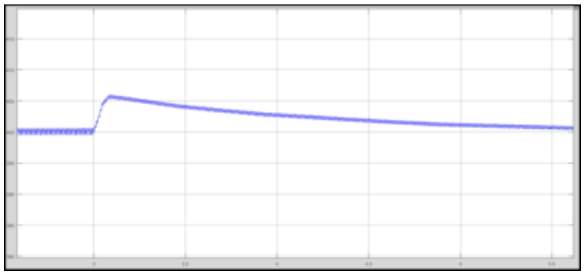
Fig. 9: Performance of DC-link voltage control algorithms for capacitive load with the desired voltage of 400 V.

5.2 Dynamic operation

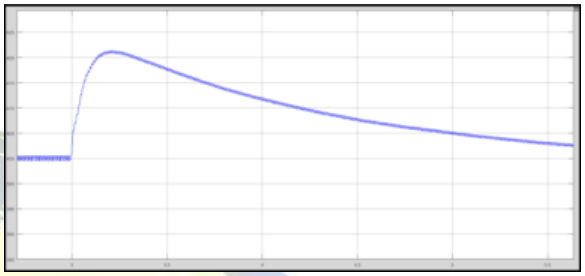
Figs. 10 and 11 demonstrate the impact of every DC-link capacitor voltage control calculation towards the managed DC voltage for operations from capacitive to inductive and inductive to capacitive, individually. For capacitive to inductive, the self-accusing of step size error cancelation calculation demonstrates the best execution with just overshoot of 0.5 V and reaction time of 0.1 s. The second best execution is the self-accusing of FLC calculation which performs with overshoot of 5 V and reaction time of 2 s. The most exceedingly bad execution is appeared by the self accusing of PI calculation with the most elevated overshoot of 21 V and the longest reaction time of 4s. For inductive to capacitive, the self-accusing of step size error cancelation calculation additionally demonstrates the best execution with undershoot of 1 V and just reaction time of 0.5 s. Then again, the self-accusing of PI calculation demonstrates the most exceedingly awful execution with undershoots of 27V and reaction time in around 4s. The self-accusing of FLC calculation, in spite of the fact that is superior to anything the self-accusing of PI calculation, still has high undershoot of 8 V and reaction time of 2 s.



(a)

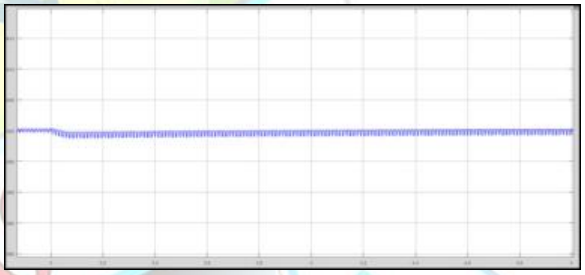


(b)

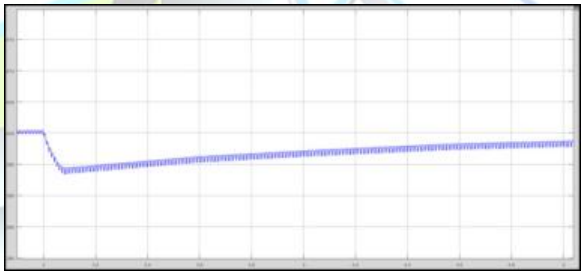


(c)

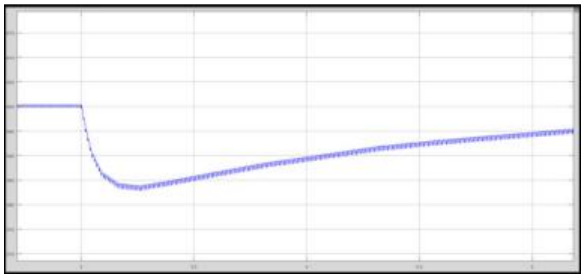
Fig. 10: Performance of DC-link voltage control algorithm for capacitive to inductive.



(a)



(b)



(c)

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

Fig. 11: Performance of DC-link voltage control algorithm for inductive to capacitive.

From all the simulation results, in both steady state and dynamic operations, the self accusing of step size error cancelation calculation demonstrates the best execution with high exactness, low overshoot, low undershoot and quick reaction time. The self-accusing of PI and FLC calculations, as broadly utilized some time recently, perform well under steady-state condition. In any case, amid dynamic operation, those self-charging calculations don't perform well as they can't track and control impact from the quick changing of the non-linear loads. The two calculations are relegated to control the voltage error straightforwardly, neglect either the voltage error has certain esteem or just zero; in this way, there is plausibility of postponement to deliver the charging current of the DC-link capacitor because of impact of operation from PI or FLC system. Therefore, they perform with ease back tracking which prompts conceivable high overshoot and undershoot, and moderate reaction time.

VI. CONCLUSION

This paper has displayed another DC-link capacitor voltage control calculation which presents another element, known as step size error cancelation. It has been added to upgrade the ability of the self-charging calculation which would in a roundabout way control the voltage error. Backhanded control gives adaptability of controlling the voltage error; beats the past calculations which straightforwardly control the voltage error despite the fact that there is no such change to its esteem. As to confirm execution of the proposed calculation, assessment under both steady state and dynamic operations has been completed. Examination in steady-state operation has broadly been utilized earlier; subsequently, through extra investigation with dynamic operation which adds to uniqueness of this work, more complete results and discoveries have been acquired for assist evaluation.

The proposed calculation has successfully been exhibited and relative assessment has been completed with the built up self-accusing calculations of PI or FLC keeping in mind the end goal to check its better execution. The simulation work affirms that the proposed calculation can accomplish high exactness in steady-state operation, and low overshoot with quick reaction time in dynamic operation. Noteworthy diverse has been observed amid dynamic operation where the proposed calculation can control any impact from the progressions between the non-linear loads.

Equipment usage has affirmed viability of the proposed calculation through both steady state and dynamic operations as did in the simulation work. Quick reaction time, low overshoot and low undershoot unmistakably demonstrate the benefits of the proposed calculation over the set up self-charging calculations particularly amid dynamic operation.

REFERENCES

1 IEEE Standard 1159: 'IEEE Recommended Practice for Monitoring Electric Power Quality', Institute of Electrical and Electronics Engineers, New York, 2014

2 Dugan, R.C., McGranaghan, M.F., Santoso, S., Beaty, H.W.: 'Electrical power systems quality' (McGraw-Hill, New York, 2003, 2nd edn.)

3 Stones, J., Collinson, A.: 'Power quality', Power Eng. J., 2001, 15, (2), pp. 58–64

4 Tey, L.H., Soand, P.L., Hu, Y.C.: 'Improvement of power quality using adaptive shunt filter', IEEE Trans. Power Deliv., 2005, 20, pp. 1558–1568

5 Yongtao, D., Wenjin, D.: 'Harmonic and reactive power compensation with artificial neural network technology'. Proc. 7th World Congress on Intelligent Control and Automation, 2008, pp. 9001–9006

6 Mikkili, S., Panda, A.K.: 'Types-1 and -2 fuzzy logic controllers-based shunt active filter Id–Iq control strategy with different fuzzy membership functions for power quality improvement using RTDS hardware', IET Power Electron., 2013, 6, (4), pp. 818–833

7 Christo Ananth, W.Stalin Jacob, P.Jenifer Darling Rosita. "A Brief Outline On ELECTRONIC DEVICES & CIRCUITS.", ACES Publishers, Tirunelveli, India, ISBN: 978-81-910-747-7-2, Volume 3,April 2016, pp:1-300.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 3, March 2017

8 Choi, W.H., Lam, C.S., Han, Y.D.: 'Analysis of DC-link voltage controls in three-phase four-wire hybrid active power filters', IEEE Trans. Power Electron., 2013, 28, (5), pp. 2180–2191
9 Guo, X., Wang, D., Chen, R., Liu, S., Li, Y.: 'Active power filter DC bus voltage control based on fuzzy PI compound control'. World Automation Congress (WAC), 2012, pp. 1–4
10 Bhattacharya, A., Chakraborty, C.: 'A shunt active power filter with enhanced performance using ANN-based predictive and adaptive controllers', IEEE Trans. Ind. Electron., 2011, 58, (2), pp. 421–428
11 Afghoul, H., Krim, F.: 'Comparison between PI and fuzzy DPC control of a shunt active power filter'. Second IEEE ENERGYCON Con. & Exhibition Advances in Energy Conversion Symp., 2012, pp. 146–151
12 Mehta, G., Patidar, R.D., Singh, S.P.: 'Design, analysis and implementation of DSP based single-phase shunt active filter controller'. Proc. Emerging Trends in Electrical and Computer Technology (ICETECT), 2011, pp. 166–173
13 Ponpandi, R., Durairaj, D.: 'A novel fuzzy-adaptive hysteresis controller based three phase four wire-four leg shunt active filter for harmonic and reactive power compensation', Energy Power Eng., 2011, 3, pp. 422–435
14 Husen, S.S., Patel, P.J.: 'A literature review and industrial survey on active power filter', Int. J. Eng. Dev. Res., 2014, 2, (1), pp. 118–125
15 Farahat, M.A., Zobah, A.: 'Active filter for power quality improvement by artificial neural networks technique'. Thirty ninth Int. Universities Power Engineering Conf., 2004, vol. 1, pp. 878–883
16 Abdel Aziz, M.M., Zobaa, A.F., Hosni, A.A.: 'Neural network controlled shunt active filter for nonlinear loads'. Eleventh Int. Middle East Power Systems Conf., 2006, pp. 180–188
17 Priya, S.M., Keerthana, K.: 'Regulating unified power quality conditioner output using Kalman filters', Int. J. Mod. Eng. Res., 2013, pp. 62–73
18 Khoor, M.S., Machmoum, M.: 'A low voltage dynamic voltage restorer with self-charging capability'. European Conf. on Power Electronics and Applications, 2007, pp. 1–9
19 Kwan, K.H., So, P.L., Chu, Y.C.: 'An output regulation-based unified power quality conditioner with Kalman filters', IEEE Trans. Ind. Electron., 2012, 59, (11), pp. 4248–4262
20 Abdul Rahman, N.F.A., Radzi, M.A.M., Mariun, N., Che Soh, A., Rahim, N.A.: 'Integration of dual intelligent algorithms in shunt active power filter'. IEEE Conf. on Clean Energy and Technology (CEAT), 2013, pp. 259–264
21 Rachid Dehini, A.B., Ferdi, B.: 'Artificial neural networks application to improve shunt active power filter', Int. J. Comput. Inf. Eng., 2009, 3, pp. 8–15
22 Xin, T., Tsang, K.M., Chan, W.L.: 'A power quality compensator with DG interface capability using repetitive control', IEEE Trans. Energy Convers., 2012, 27, pp. 213–219
23 Bhim Singh, A.C., Al-Haddad, K.: 'Computer-aided modeling and simulation of active power filters', Electr. Mach. Power Syst., 1999, 27, pp. 1227–1241
24 Jain, S.K., Agrawal, P., Gupta, H.O.: 'Fuzzy logic controlled shunt active power filter for power quality improvement', IEE Proc. Electr. Power Appl., 2002, 149, pp. 317–328
25 Suresh, Y., Panda, A.K., Suresh, M.: 'Real-time implementation of adaptive fuzzy hysteresis-band current control technique for shunt active power filter', IET Power Electron., 2012, 5, pp. 1188–1195
26 Singh, B., Al-Haddad, K., Chandra, A.: 'A review of active filters for power quality improvement', IEEE Trans. Ind. Electron., 1999, 46, (5), pp. 960–971
27 Lin, B.R., Yang, T.Y.: 'Three-level voltage-source inverters for shunt active filter', IEE Proc. Electr. Power Appl., 2004, 151, (6), pp. 744–751
28 Moreno, V.M., López, A.P., Garcías, R.I.D.: 'Reference current estimation under distorted line voltage for control of shunt active power filters', IEEE Trans. Power Electron., 2004, 19, (4), pp. 988–984
29 Routimo, M., Salo, M., Tuusa, H.: 'Comparison of voltage-source and current source shunt active power filters', IEEE Trans. Power Electron., 2007, 2, (2), pp. 636–643
30 Lega, A., Mengoni, M., Serra, G., Tani, A., Zarri, L.: 'General theory of space vector modulation for

five-phase inverters'. Int. Symp. on Industrial Electronics ISIE, 2008, pp. 237–244
31 Cirrincione, M., Pucci, M., Vitale, G.: 'A single-phase DG generation unit with shunt active power filter capability by adaptive neural filtering', IEEE Trans. Ind. Electron., 2008, 55, (5), pp. 2093–2110
32 Singh, B., Verma, V., Solanki, J.: 'Neural network-based selective compensation of current quality problems in distribution system', IEEE Trans. Ind. Electron., 2007, 54, (1), pp. 53–60
33 Vasumathi, B., Moorthi, S.: 'Harmonic estimation using modified ADALINE algorithm with time-variant Widrow–Hoff (TVWH) learning rule'. IEEE Symp. on Computers & Informatics, 2011, pp. 113–118
34 Wenjin, D., Taiyang, H.: 'Design of single-phase shunt active power filter based on ANN'. IEEE Int. Symp. on Industrial Electronics, 2007, pp. 770–774
35 Radzi, M.A.M., Rahim, N.A.: 'Neural network and band-less hysteresis approach to control switched capacitor active power filter for reduction of harmonics', IEEE Trans. Ind. Electron., 2009, 54, (5), pp. 1477–1484
36 Shu, Z., Zhu, H., He, X., Na, D., Jing, Y.: 'One-inductor-based auxiliary circuit for dc-link capacitor voltage equalization of diode-clamped multilevel converter', IET Power Electron., 2012, 6, (7), pp. 1339–1349
37 Orfanoudakis, G.I., Yuratich, M.A., Sharkh, S.M.: 'Analysis of dc-link capacitor current in three-level neutral point clamped and cascaded H-bridge inverters', IET Power Electron., 2103, 6, (7), pp. 1376–1389
38 Chaouachi, A., Kamel, R.M., Nagasaka, K.: 'A novel multi-model neuro-fuzzy-based MPPT for three-phase grid-connected photovoltaic system', Sol. Energy, 2010, 84, pp. 2219–2229
39 Wu, Y., Zhang, B., Lu, J., Du, K.L.: 'Fuzzy logic and neuro-fuzzy system: a systematic introduction', Int. J. Artif. Intell. Expert Syst. (IJAE), 2011, 2, pp. 47–80.

Mr. K. BALAKRISHNA is currently pursuing M.Tech in Electrical Power System Tudi Narasimha Reddy institute of technology & sciences, Gudur, Bibinagar, Yadadribhongiri, Telangana., Affiliated to JNTU Hyderabad. He received Bachelor of technology Degree in Electrical and Electronics Engineering from JAWAHARLAL NEHRU INSTITUTE OF TECHNOLOGY, Affiliated to JNTU Hyderabad in 2014, and his field of interest includes power systems.
Email id: kbalakrishna931@gmail.com

Mrs. N. MANASA
She is currently working as Assistant Professor in EEE DEPARTMENT with Tudi Narasimha Reddy institute of technology & sciences, Gudur, Bibinagar, Yadadribhongiri, Telangana., Affiliated to JNTU Hyderabad. Her interest subjects are Electrical measurements and instrumentation, Electrical power system.
Email id: manu.nanduri@gmail.com