



## A Novel Approach of Convolution Encoder and viterbi decoder

P. Vineetha<sup>(1)</sup>

Dr.K.Babulu<sup>(2)</sup>

<sup>1</sup> Dept of ECE, University college of engineering,kakinada(autonomous) jntuk, Kakinada, East godavari, Andhra Pradesh, India,

<sup>2</sup> Professor, Dept of ECE, University college of engineering,kakinada(autonomous) jntuk, Kakinada, East Godavari, Andhra Pradesh, India,

**Abstract:** The best way of decoding against random errors is to compute the received sequence with every possible code sequence. This is called maximum likelihood (ML) decoding. The criterion for deciding between two paths is to select the one having the smaller metric. The rule maximizes the probability of a correct decision. Initially the digital signal is applied to the constellation mapper then the obtained output is given to puncture block. Punctured codes can be used in communication systems with a rate-adaption mechanism. It converts the code rate from one to two bits which can be carried by conventional encoder. The viterbi decoder performs the decoding mechanism by accepting the encoder output through the interface which can be converted into original form through the constellation demapper blocks.

The MB OFDM reduces the number of computations and maintains the orthogonality. The Proposed Viterbi decoder reduces memory and the hardware resources. Exploiting parallelism with-n way parallel architecture enables to keep throughput constraint at n times lower clock speeds. The proposed architecture checks every node for path metric value and eliminates the path that is found if it is not

having Minimum distance. This architecture is simulated, synthesized and implemented by VERILOG language using XILINX ISE Tool.

**Keywords:** Puncturer, Viterbi, BMU, ACS.

### INTRODUCTION

In telecommunication, a convolutional code is a type of error-correcting code that generates parity symbols via the sliding application of a boolean polynomial function to a data stream. The sliding application represents the 'convolution' of the encoder over the data, which gives rise to the term 'convolutional coding.' The sliding nature of the convolutional codes facilitates trellis decoding using a time invariant trellis. Time invariant trellis decoding allows convolutional codes to be maximum likelihood soft decision decoded with reasonable complexity. The ability to perform economical maximum likelihood soft decision decoding is one of the major benefits of convolutional codes.

This is in contrast to classic block codes which are generally represented by a time variant trellis and therefore are typically hard decision decoded. Convolutional codes are often characterized by the base code rate and the depth (or memory) of the encoder  $[n,k,K]$ . The base



code rate is typically given as  $n/k$ , where  $n$  is the input data rate and  $k$  is the output symbol rate. The depth is often called the "constraint length" 'K', where the output is a function of the previous  $K-1$  inputs. The depth may also be given as the number of memory elements 'v' in the polynomial or the maximum possible number of states of the encoder (typically  $2^v$ ). Convolutional codes are often described as continuous.

However, it may also be said that convolutional codes have arbitrary block length, rather than that they are continuous, since most real world convolutional encoding is performed on blocks of data. Convolutionally encoded block codes typically employ termination. The arbitrary block length of convolutional codes can also be contrasted to classic block codes, which generally have fixed block lengths that are determined by algebraic properties. The Viterbi decoding algorithm, proposed in 1967 by Viterbi, is a decoding process for convolutional codes in memory-less noise. The algorithm can be applied to a host of problems encountered in the design of communication systems. The Viterbi decoding algorithm provides both a maximum-likelihood and a maximum a posteriori algorithm. A maximum a posteriori algorithm identifies a code word that maximizes the conditional probability of the decoded code word against the received code word, in contrast a maximum likelihood algorithm identifies a code word that maximizes the conditional probability of the received code word against the decoded code word. The two algorithms give the same results

when the source information has a uniform distribution. Traditionally, performance and silicon area are the two most important concerns in VLSI design.

A viterbi decoder uses the Viterbi algorithm for decoding a bit stream that has been encoded using Forward error correction based on a Convolutional code. The Viterbi algorithm is commonly used in a wide range of communications and data storage applications. It is used for decoding convolutional codes, in baseband detection for wireless systems, and also for detection of recorded data in magnetic disk drives. The requirements for the Viterbi decoder or Viterbi detector, which is a processor that implements the Viterbi algorithm, depend on the applications where they are used. This results in very wide range of required data throughputs and power or area requirements.

## 2 DESIGN ASPECTS

The Viterbi decoding algorithm is a decoding process for convolutional codes for memory-less channel. Figure 1 depicts the normal flow of information over a noisy channel. For the purpose of error recovery, the encoder adds redundant information to the original Information, and the output is transmitted through a channel. Input at receiver end ( $r$ ) is the information with redundancy and possibly, noise. The receiver tries to extract the original information through a decoding algorithm and generates an estimate ( $e$ ).

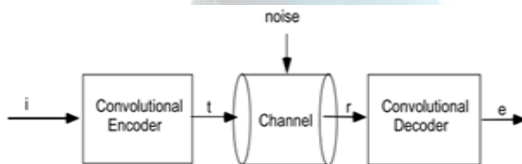
A decoding algorithm that maximizes the probability  $p(r|e)$  is a maximum likelihood (ML) algorithm. An algorithm which maximizes the  $p(r|e)$  through the proper selection of the



estimate (e) is called a maximum a posteriori (MAP) algorithm. The two algorithms have identical results when the source information  $i$  has a uniform distribution.

## 2.1 CONVOLUTIONAL ENCODER

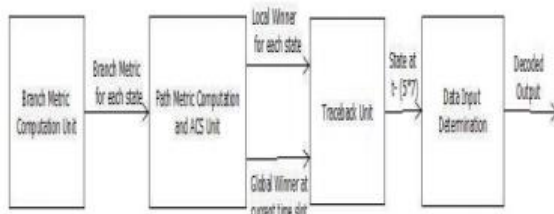
Data is coded by using a convolutional encoder. It consists of a series of shift registers and an associated combinatorial logic. The combinatorial logic is usually a series of exclusive-or gates. The conventional encoder  $\frac{1}{2}$  K=9 used for the purpose of this project. The octal numbers 171 and 133 when represented in binary form correspond to the connection of the shift registers to the upper and lower exclusive-or gates respectively



**Figure 1:** The Convolutional Encoder

## 2.2 VITERBI DECODER

This project uses a hard decision Viterbi decoder for the purpose of developing and verifying the new energy saving algorithm. Once the algorithm is verified, a soft decision Viterbi decoder may be used in place of the hard decision decoder. Figure 2 shows the various stages required to decode data using the Viterbi Algorithm. The decoding mechanism comprises of three major stages namely the Branch Metric Computation Unit, the Path Metric Computation and Add-Compare-Select(ACS) Unit and the Traceback Unit. A schematic representation of the decoder is described below.

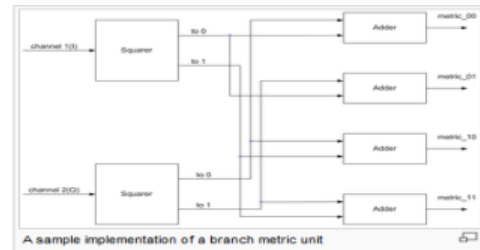


**Figure 2:** Schematic representation of the Viterbi decoding block

### Branch Metric Computation (BMC)

For each state, the Hamming distance between the received bits and the expected bits is calculated. Hamming distance between two symbols of the same length is calculated as the number of bits that are different between them. These branch metric values are passed to Block 2. If soft decision inputs were to be used, branch metric would be calculated as the squared Euclidean distance between the received symbols. The squared Euclidean distance is given as  $(a_1 - b_1)^2 + (a_2 - b_2)^2 + (a_3 - b_3)^2$  where  $a_1, a_2, a_3$  and  $b_1, b_2, b_3$  are the three soft

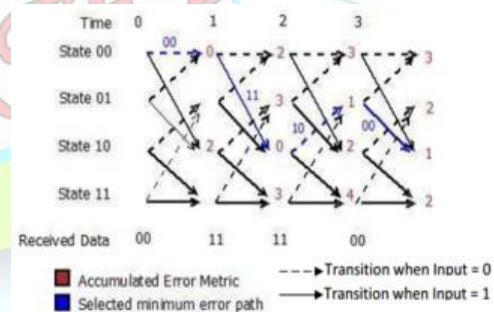
decision bits of the received and expected bits respectively.



**Figure 3:** Branch Metric Unit

### Trace back Unit

The global winner for the current state is received from Block 2. Its predecessor is selected in the manner. In this way, working backwards through the trellis, the path with the minimum accumulated path metric is selected. This path is known as the traceback path. A diagrammatic description will help visualize this process.



**Figure 4:** Selected minimum error path for a  $\frac{1}{2}$  code rate

The state having minimum accumulated error at the last time instant is State 10 and traceback is started here. Moving backwards through the trellis, the minimum error path out of the two possible predecessors from that state is selected. This path is marked in blue. The actual received data is described





at the bottom while the expected data written in blue along the selected path. It is observed that at time slot three there was an error in received data (11). This was corrected to (10) by the decoder.

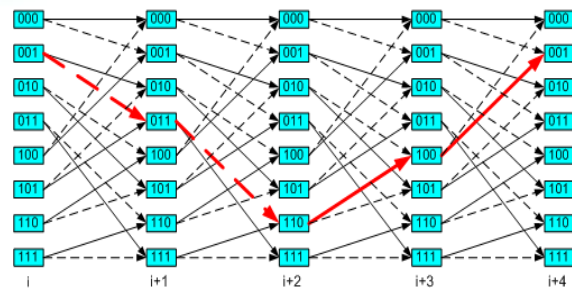
Local winner information must be stored for five times the constraint length. For a  $K=7$  decoder, this results in storing history for  $7 \times 5 = 35$  time slots. The state of the decoder at the time instant 35 time slots prior can then be accurately determined. This state value is passed to Block 4. At the next time slot, all the trellis values are shifted left to the previous time slot. The path metric for the last received data and compute the minimum error path is then calculated. If the global winner at this stage is not a child of the previous global winner, the traceback path has to be updated accordingly until the traceback state is a child of the previous state. [3] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm. By this design, the power dissipation, delay and noise can be reduced.

## Trellis Diagram

A convolutional encoder is often seen as a *finite state machine*. Each state corresponds to some value of the encoder's register. Given the input bit value, from a certain state the encoder can move to two other states. These state transitions constitute a diagram which is called a *trellis diagram*. A solid line corresponds to input 0, a dotted line – to input 1 (note that encoder states are designated in such a way that the rightmost bit is the newest one).

Each path on the trellis diagram corresponds to a valid sequence from the encoder's output. Conversely, any valid sequence from the encoder's output can be represented as a path on the trellis diagram. One of the possible paths is denoted as red (as an example). Note that each state transition on the diagram corresponds to a pair of output bits. There are only two allowed transitions for every state, so there are two allowed pairs of output bits, and the two other pairs are forbidden.

If an error occurs, it is very likely that the receiver will get a set of forbidden pairs, which don't constitute a path on the trellis diagram. So, the task of the decoder is to find a path on the trellis diagram which is the closest match to the received sequence.



**Figure 5:** A trellis diagram corresponding to the encoder

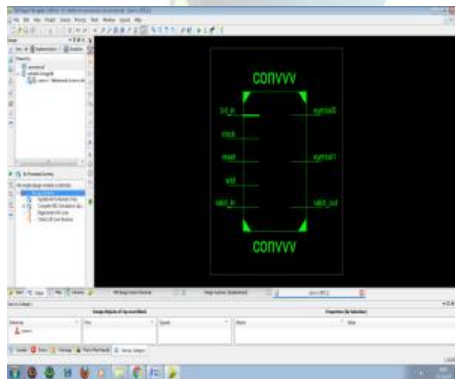
Let's define a *free distance*  $d_f$  as a minimal Hamming distance between two different allowed binary sequences (a Hamming distance is defined as a number of differing bits).

## 4 RESULTS

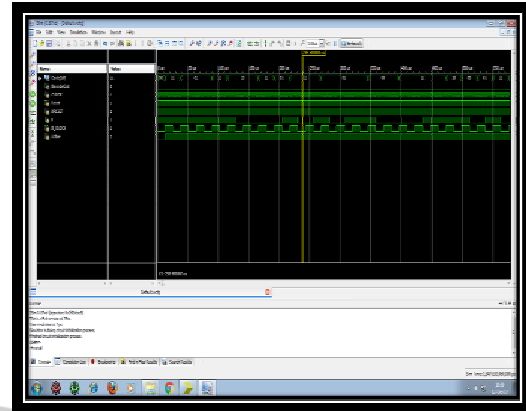
### CONVOLUTIONAL ENCODER

The viterbi decoder decodes the noisy data received through the channel. This detects and corrects the bit errors introduced by noise generation block and reproduce the data which is given as input to convolution encoder.

**FIG 6 SCHEMATIC DIAGRAM OF CONVOLUTIONAL ENCODER**



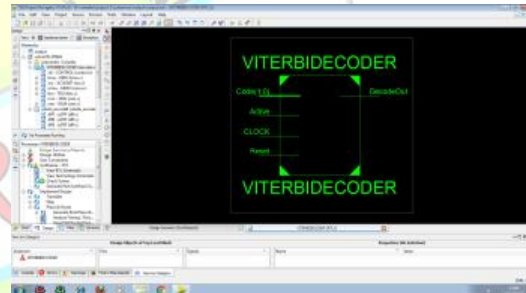
The output waveform of convolutional encoder are shown in the figure 6.1



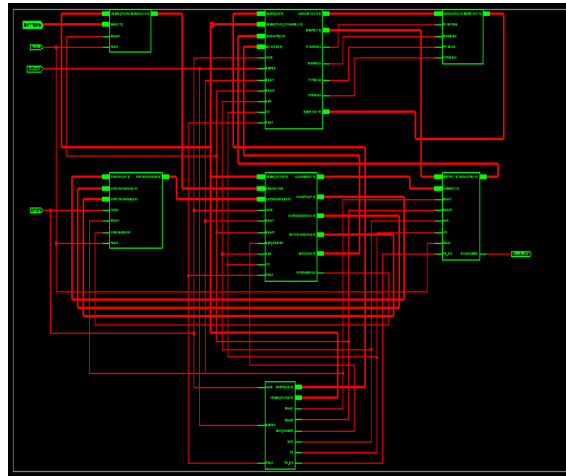
**FIGURE 6.1 OUTPUT WAVEFORM OF CONVOLUTIONAL ENCODER**

The RTL schematic of viterbi decoder is shown in figure 7

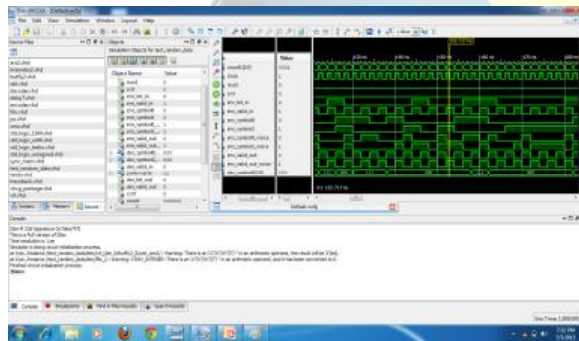
**FIG 7 SCHEMATIC DIAGRAM OF VITERBI DECODER**



**Fig 7.1 INTERNAL DIAGRAM OF VITERBI DECODER**



The simulation results of the viterbi decoder are shown in fig 7.2



**Fig 7.2 OUTPUT WAVEFORM OF VITERBI DECODER**

The viterbi decoder takes the received noisy signals `enc_symbol0_noise` and `enc_symbol1_nose` as inputs and generates an error free data `dec_bit_in`. This data is accumulated into register for analyzing the error correcting capability of entire system.

## 5 CONCLUSIONS

We have proposed a high speed VD design for TCM systems. The precomputation architecture that incorporates T-algorithm efficiently reducing the decoding speed

preciably. We have also analysed computation algorithm .where the optimal computation steps are calculated and discussed. This algorithm is suitable for TCM systems which always employ high rate convolution code. Finally we presented a design case. Both the ACSU and SMU are modified to correctly to decode the signal. The synthesis results show that VD could improve maximum decoding speed. By using FPGA device and hybrid microprocessor the decoding benefits can be achieved in future. In future to improve the decoder performance the

Viterbi algorithm is carried out in reconfigurable hardware. Power saving architecture can be designed for the above decoder which is executable in the mobile devices. Viterbi decoder can also be implemented using JAVA. Therefore in the future Viterbi algorithm may be used for various scenarios. So in the future the complexity can be greatly reduced.

## 6 REFERENCES

- [1] A. Batra, J. Balakrishnan, and A. Dabak, "Multi-band OFDM: A new approach for UWB," in Proc. IEEE Int. Symp. Circuit Syst. (ISCAS), 2004, pp. 365–368.
- [2] MultiBand OFDM Alliance Special Interest Group and WiMedia Alliance, Inc., San Ramon, CA, "MultiBand OFDM Physical Layer Specification, Release 1.1," 2005.
- [3] Christo Ananth, Bincy P Chacko, "Analysis and Design of Low Voltage Low Noise LVDS Receiver", IOSR Journal of Computer Engineering (IOSR-JCE), Volume 9, Issue 2, Ver. V (Mar - Apr. 2014), PP 10-18



ISSN 2394-3777 (Print)

ISSN 2394-3785 (Online)

Available online at [www.ijartet.com](http://www.ijartet.com)

*International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)*  
*Vol. 4, Special Issue 2, January 2017*

- [4] Bernard Sklar ,“Digital communication Fundamentals and Applications”, 2<sup>nd</sup> edition ,Prentice Hall, ISBN:81-7808-373-6, 2001.
- [5] Michael Purser , “Introduction to Error-correction codes”, Artech House INC,ISBN: 0-89006-784-8 ,1996 .

