ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology
Vol. 4, Special Issue 2, January 2017

REALISATION OF POWER OPTIMIZED FM0/MANCHESTER ENCODING ARCHITECTURE USING SOLS TECHNIQUE

Kalle Manoj Pavan Kumar [(1)] **Dr. S.Chandra mohan reddy** [(2)]

[1]PG Scholar, Dept of ECE, Jawaharlal Nehru Technological University Anantapur College of engineering (autonomous), Pulivendula,Y.S.R. Kadapa,Andhra Pradesh, India

[2]Associate Professor, Dept of ECE, Jawaharlal Nehru Technological University Anantapur College of engineering (autonomous), Pulivendula,Y.S.R. Kadapa,Andhra Pradesh, India

Abstract:-Dedicated-Short-Range Exchanges [1] are one-way or two-way short-range to medium-go remote correspondence channels especially expected for auto use and a looking at set of traditions and gages. In media transmission and data amassing, Manchester coding[2] (also known as Phase Encoding, or PE) is a line code in which the encoding of each datum bit has no short of what one change and includes a comparative time. The inspirations driving FM0 and Manchester codes can give the transmitted banner dc-change and are for the most part grasped in encoding for downlink. The Manchester encoding is recognized with a XOR operation for CLK which incorporates a change inside one cycle and data X.

The equipment blueprint of FM0 encoding should begin with the FSM of FM0 first. The DSRC gages everything considered handle FM0 and Manchester codes to fulfill dc-change, and redesign the standard persevering quality. The coding-normal combination between the FM0 and Manchester codes truly limits the probability to outline a completely reused VLSI design. In this paper, the Similarity-Oriented Logic Simplification (SOLS) framework is proposed to beat this restriction, which overhauls the apparatus use rate. In this project Cadence virtuoso tool is used for layout and schematic simulation, logical verification, and further synthesizing. In this paper the sparse kogge implementation results less area and reduced power than the existing kogge implementation.

Keywords: Dedicated-Short-Range Communication, cadence tool

I. INTRODUCTION

This standard demonstrates a crucial application interface that extend the DSRC tradition abilities to allow executing non-IP sort various uses of different sorts and with different helpfulness in the correspondence between a Land Mobile Station and Base Station in a DSRC system as described by the ARIB STD-T75 **"DEDICATED SHORT-RANGE COMMUNICATION (DSRC) SYSTEM" and ARIB STD-T88 "DEDICATED SHORT-RANGE COMMUNICATION (DSRC) APPLICATION SUB-LAYER"** standards.

The DSRC structure secured by this standard contains a Base Station and Land Mobile Station and equipment for testing. The standard decidses the going with six sorts of fundamental application interfaces for roadside-to-vehicle correspondence inside such a DSRC system.

Remembering the true objective to hinder security spills when singular information or settlement information is exchanged between Land Mobile Station and Base Station, and to keep the threat of structure ambushes by a threatening Base Station or Land Mobile Station, shared affirmation and rigging approval must be completed. To finish this, a security platform (DSRC-SPF) is composed over the application sub-layer's close-by port

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology
Vol. 4, Special Issue 2, January 2017

tradition (LPP). Information about the association between the security arrange (DSRC-SPF) and the fundamental application interface is given in Annex 2. An IP sort application here is a framework application that is executed on the Internet Protocol dictated by ARIB STD-T88 "DEDICATED SHORT RANGE COMMUNICATION (DSRC) APPLICATIONSUB-LAYER,[3]" additionally, a non-IP sort application is a non-arrange application that does not use the framework tradition stack and runs particularly on the application sub-layer .

Handling of Reserved Fields:

Variables, information fields, et cetera implied as "Held" in this standard are normal for future enlargements of definitions. In a couple of illustrations, specific regards or identifiers are given in this standard, be that as it may it must be seen that such regards may be obligated to change in future rectifications.

Encoding Rules:

The DSRC can be immediately organized into two arrangements: auto to-vehicle and auto to-roadside. In auto to-vehicle, the DSRC enables the message sending likewise, conveying among vehicles for prosperity issues and open information presentation [2], [3]. The prosperity issues join blind spot, crossing point alerted, interacts detachment, and crash caution. The auto to-roadside focuses on the keen transportation advantage, for instance, electronic toll aggregation (ETC) system. With ETC, the toll collecting is electrically capable with the contactless IC-card organize. Moreover, the ETC can be connected with the portion for ceasing organization, and gas-refueling. In this way, the DSRC system expects a basic part in display day auto industry. The system outline of DSRC handset is showed up in Fig. 1. The upper and base parts are dedicated for transmission and tolerating, independently. This handset is organized into three essential modules: chip, baseband dealing with, and RF front-end. The microchip unravels rules from media get the chance to control to design the endeavors of baseband getting ready and RF front-end. The baseband getting ready is accountable for adjust, bumble review, clock synchronization, and encoding. The RF frontend transmits and gets the remote banner through the antenna. The DSRC standards have been set up by a couple relationships in different countries. These DSRC rules of America, Europe, and Japan are showed up in Table I. The data rate independently centers at 500 kb/s, 4 Mb/s, and 27 Mb/s with conveyor repeat of 5.8 and 5.9 GHz. The change methods intertwine abundance move keying, arrange move keying, and orthogonal repeat division multiplexing. All things considered the waveform of transmitted banner is required to have zero mean for generosity issue, and this is moreover suggested as dc-alter. The transmitted banner includes self-decisive twofold game plan, which is difficult to secure dc-modify. The reasons of FM0 and Manchester codes can outfit the transmitted signal with dc-alter. Both FM0 and Manchester codes are extensively gotten in encoding for downlink.

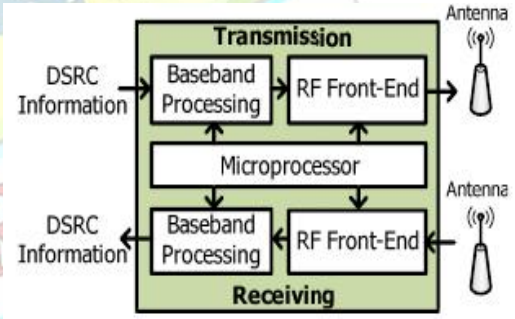


Fig.1 System architecture of DSRC transceiver

The DSRC standards have been established by several organizations in different countries. These DSRC standards of America, Europe, and Japan are shown in Table I.

The data rate individually targets at 500 kb/s, 4 Mb/s, and 27 Mb/s with carrier frequency of 5.8 and 5.9 GHz.

The modulation methods incorporate amplitude shift keying, phase shift keying, and orthogonal frequency division multiplexing. Generally, the waveform of transmitted signal is expected to have zero-mean for robustness issue, and this is also referred to as dc-balance. The microprocessor interprets instructions from media

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology
Vol. 4, Special Issue 2, January 2017

access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF front-end transmits and receives the wireless signal through the antenna. [5] presented a short overview on widely used microwave and RF applications and the denomination of frequency bands. The chapter start outs with an illustrative case on wave propagation which will introduce fundamental aspects of high frequency technology.

II. PRINCIPLES OF FM0 AND MANCHESTER CODE

If X is the logic-0,The fm0 code has the transition between the A and B. If X is the logic-1, there is no transition is allowed between the A and B. The transition is allocated in each FM0 code. The wave form is given below the following diagram. The fm0 has the clock and then the x.the clock and then the cycle having the cycle in each transaction.

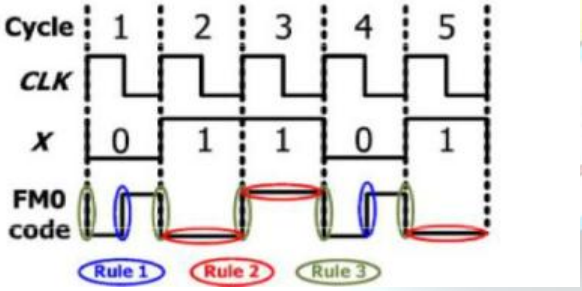


Fig.2 FM0 Encoding.

The Manchester Encoding is realized with the XOR operation for using the CLOCK and X. The clock always has a transition within the one cycle.

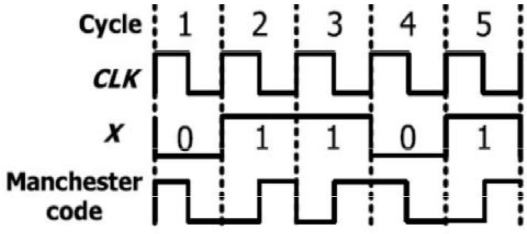


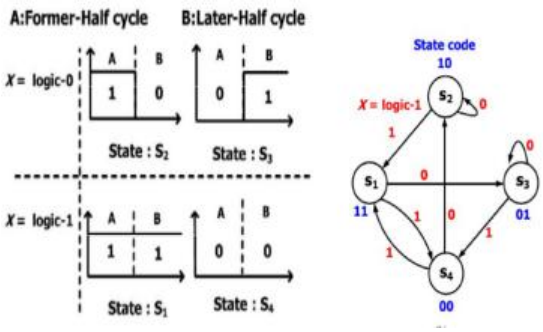
Fig.3. Manchester Encoding.

Dedicated short range communication (DSRC) is a fast, short to mid range, wireless technology. It enables one way or two way communication between vehicles or between vehicles and roadside. It is to used make streets safer, travel easier and minimizes the impact vehicles have on the environment. It provides vehicles and infrastructure the ability to communicate with each other at a rate of 10 times per second. In DSRC communication, the most important concern is collision detection.

Each DSRC orchestrated vehicle passes on its key data including speed, heading, run and so forth to a short degree of segment, say a few hundred meters. All other DSRC masterminded vehicles in the range gets this message. Later on this message is decoded by the expert vehicles and a caution or alarmed might be issued to the driver.

The DSRC correspondence depends upon organize correspondence among vehicles and thusly does not require dealing with. In this manner it is in like way suggested as single bounce. This sort of correspondence can in like way be proposed as unbalanced passed on lighting up. Each DSRC organized vehicles can stretch out this system to its neighbors and therefore this structure can twist up perceptibly unbounded. In the event of security, affirmation is additionally a fundamental concern. In this way all security exchanges are done in the control direct in a way. The success correspondence consolidates two sorts of messages which are Routine security messages: These are status messages including change of speed, go, and so forth that are dependably sent by the vehicle and Event security messages: These are messages that indication an occasion like a hard brake.

The Manchester Encoding [6] is an XOR operation only. The FM0 code starts with the FSM principle. The FSM of FM0 code classified into four states. The four states as shown in the below figure.



ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology
Vol. 4, Special Issue 2, January 2017

Fig.4.FSM of FM0 Fig 5.State diagram

Suppose the initial state is S1, and its state code is 11 for A and B, respectively. If the X is logic-0, the state-transition must follow both rules for FM01 and 3. The only one next-state that can satisfy both rules for the X of logic-0 is S3.

If the X is logic-1, the state-transition must follow both rules for FM0 2 and 3. The only one next-state that can satisfy both rules for the X of logic-1 is S4. Thus, the state-transition of each state can be completely constructed. The FSM of FM0 can also conduct the transition table of each state A(t) and B(t) represent the discrete-time state code of current-state at time instant t. Their previous-states are denoted as the A(t − 1)and the B(t − 1), respectively. With this transition table, the Boolean functions of A(t) and B(t) are given as A(t) = B(t − 1) and B(t) = X ⊕ B(t − 1) With both A(t) and B(t), the Boolean function of FM0 code is denoted as CLK A(t) +~ CLK B(t).

HARDWARE ARCHITECTURE OF FM0/MANCHESTER CODE:

This is the hardware outline of the fm0/Manchester code [7]. The best part is demonstrated the fm0 code and after that the base part is implied as the Manchester code. in FM0[9] code the DFFA and DFFB are used to store the state code of the fm0 code and moreover mux_1 and not entryway is used as a piece of the fm0 code.

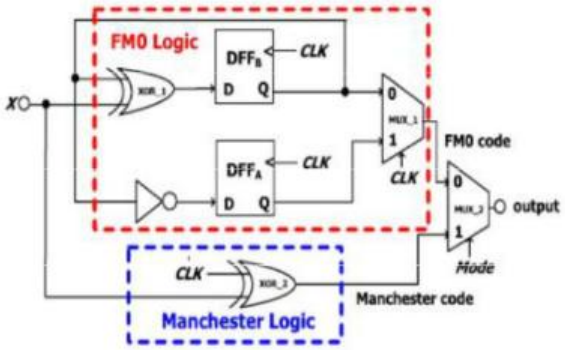


Fig 6.Architecture of FM0/Manchester Encoding

Building Prefix Structures:

Parallel-prefix structures are seen to be fundamental in better adders due than the deferral is logarithmically relating to the snake width. Such structures can when in doubt be isolated into three stages, pre-figuring, prefix tree and post-estimation. An instance of a 8-bit parallel-prefix structure is showed up in Figure 3.2. In the prefix tree, collect deliver/multiply are the fundamental signs used. The social event deliver/incite conditions rely upon single piece make/multiply, which are prepared in the pre-estimation organize.

$$g_i = a_i \cdot b_i$$

$$p_i = a_i \wedge b_i \quad \text{where}$$

$0 < I < n$. $g_{-1} = cin$ and $p_{-1} = 0$. Sometimes, pi can be computed with OR logic instead of an XOR gate. The OR justification is required especially when Ling's arrangement is associated. Here, the XOR basis is utilized to save an entryway for brief total ti.

In the prefix tree, group create/cause signals are prepared at each piece.

$$G_{i:k} = G_{i:j} + P_{i:j} \cdot G_{j-1:k}$$

$$P_{i:k} = P_{i:j} \cdot P_{j-1:k}$$

More basically, the above condition can be conveyed using a picture “o “demonstrated by Brent and Kung. Its ability is exactly the same as that of a dull cell. That is

$(G_{i:k}; P_{i:k}) = (G_{i:j}; P_{i:j}) \circ (G_{j-1:k}; P_{j-1:k})$;

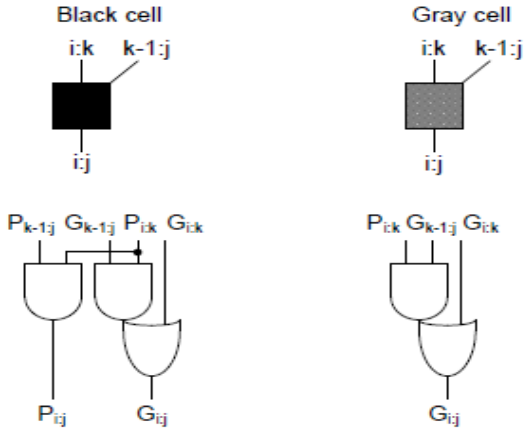


Fig.7 Cell Definitions

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology
Vol. 4, Special Issue 2, January 2017

Or

Gi:k = (gi; pi) o (gi-1; pi-1) o ……o (gk; pk)

Pi:k = pi . pi-1. …… . pk

The "o" operation will help make the rules of building prefix structures. In the post-computation, the sum and carry-out are the final output.

si = pi . Gi-1:-1

cout = Gn:-1

Where "-1" is the position of pass on input. The create/spread signs can be assembled in different shape to get a similar right passes on. In perspective of different techniques for social event the deliver/multiply flags, assorted prefix models can be made. Figure 3.3 exhibits the implications of cells that are used as a piece of prefix structures, including dim cell and diminish cell. Dim/diminish cells execute the more than two conditions, which will be seriously used as a piece of the going with trade on prefix trees.

Prefix tree family:

Parallel-prefix trees have diverse structures. These prefix trees can be perceived by four main issue. 1) Radix/Valency 2) Logic Levels 3) Fan-out 4) Wire Tracks In the going with talk about prefix trees, the radix is believed to be 2 (i.e. the amount of commitments to the basis entryways is reliably 2). The more compelling prefix designs have basis levels [log2 (n)], where n is the width of the wellsprings of information. In any case, these plans require higher fan-out, or many wire-tracks or thick method of reasoning entryways, which will exchange off the execution e.g. speed or power.

Some unique designs have alleviated fan-out and wire tracks at the cost of more method of reasoning levels. Exactly when radix is settled, The arrangement trade off is made among the basis levels, fan-out and wire tracks.

III. Kogge-Stone Prefix Tree:

Kogge-Stone [8] prefix tree is among the kind of prefix trees that use the slightest method of reasoning levels. Frankly, Kogge-Stone is a person from Knowles prefix tree. The 16-bit prefix tree can be viewed as Knowles [1, 1, 1, 1]. The numbers in the segments address the most extraordinary branch fan-out at each method of reasoning level. The best fan-out is 2 in all reason levels for all width Kogge-Stone prefix trees.

The key of building a prefix tree is the methods by which to execute Equation according to the specific features of that kind of prefix tree and apply the gauges delineated in the past fragment. Dim cells are installed like dull cells beside that the diminish cells last yield pass on outs as opposed to transitional G/P gathering.

The reason of starting with Kogge-Stone prefix tree is that it is the most easy to function similar to using a program thought. The case in Figure 3.5 is 16-bit (a vitality of 2) prefix tree. It isn't difficult to extend the structure to any width if the fundamentals are totally a great many. The number cells for a Kogge-Stone prefix tree can be counted as follows. Each logic level has n-m cells, where $m = 2^{\text{l level}} - 1$. That is, each logic level is missing m cells. That number is the sum of a geometric series starting from 1 to n/2 which totals to n-1. The total number of cells will be $n\log_2 n$ subtracting the total number of cells missing at each logic level, which winds up with $n\log_2 n - n + 1$. When n = 16, the area is estimated at 49.

Parallel prefix adders:

The PPA is like a Carry Look Ahead Adder. The production of the carriers the prefix adders can be designed in many different ways based on the different requirements. We use tree structure form to increase the speed of arithmetic operation. Parallel prefix adders are faster adders and these are faster adders and used for high performance arithmetic structures in industries. The parallel prefix addition is done in 3 steps.

1. Pre-processing stage
2. Carry generation network
3. Post processing stage

The parallel prefix adder operation has the following 3-stage structure is briefly explained as, in the first stage Pre-calculation of **pi, gi** for each stage, in the second stage Calculation of carry **ci** for each stage, in the third stage Combine **ci** and **pi** of each stage to generate the sum bits **si** final sum.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology
Vol. 4, Special Issue 2, January 2017

1. Pre-Processing stage:

In this stage we compute, the generate and propagate signals are used to generate carry input of each adder. A and B are inputs. These signals are given by the equation 1&2.

Pi=Ai Bi..... (1)
GI=Ai .Bi..... (2)

2. Carry generation stage:

In this stage we compute carries corresponding to each bit. Execution is done in parallel form.
After the computation of carries in parallel they are divided into smaller pieces. carry operator contain two AND gates , one OR gate. It uses propagate and generate as intermediate signals which are given by the equations 3&4.

Post processing stage:

This is the final stage to compute the summation of input bits. it is same for all adders and sum bit equation given Focus is on the Kogge-Stone adder, known for having minimal logic depth and fan-out. Here we designate BC as the black cell which generates the ordered pair in equation (1); the gray cell (GC) generates the left signal only. The interconnect area is known to be high, but for an FPGA with large routing overhead to begin with, this is not as important as in a VLSI implementation. The regularity of the Kogge-Stone prefix network has built in redundancy which has implications for fault-tolerant designs. The sparse Kogge-Stone adder, shown in Fig 9, is also studied. This hybrid design completes the summation process with a 4 bit RCA allowing the carry prefix network to be simplified.

Fig.8. 16 bit Kogge-Stone adder

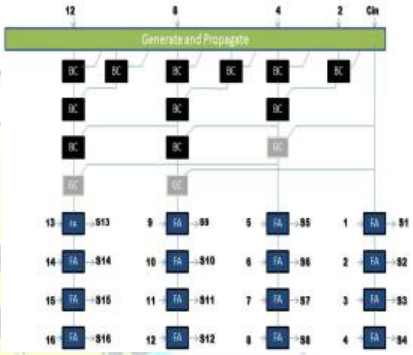
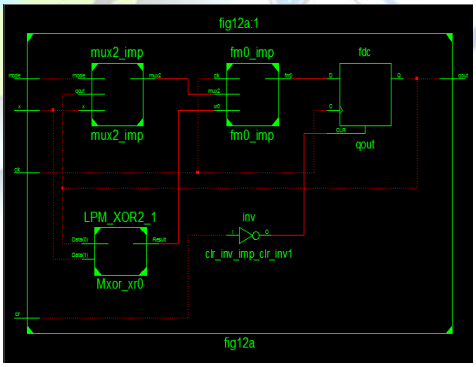


Fig.9. 16 bit sparse Kogge-Stone adder

IV. RESULTS

RTL SCHEMATIC:



ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology
Vol. 4, Special Issue 2, January 2017

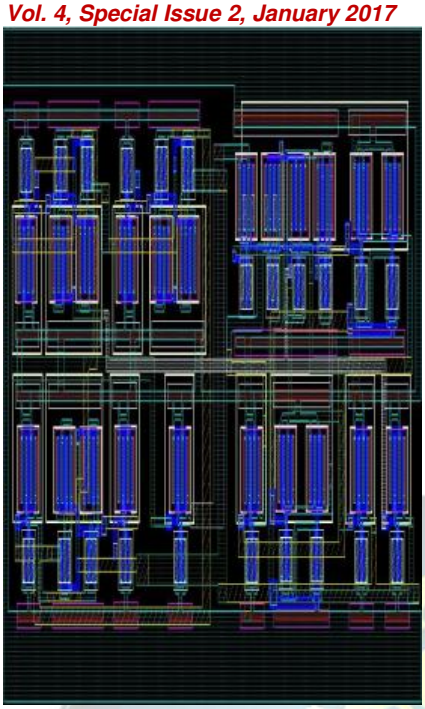
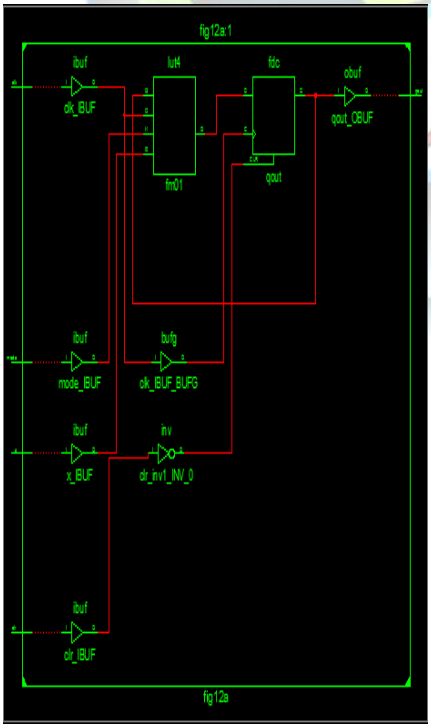


Fig.10 Layout of FM0/Manchester Encoding in 55nm Technology

TECHNOLOGY SCHEMATIC:



COMPARISION:

	NO OF LUT'S	POWER DELAY(ns)
EXIXTING METHO	95	7.22 2.732
PROPOSED METHOD	10	0.76 0.732

V. CONCLUSION

The coding-tolerable assortment among FM0 and Manchester encodings causes the requirement on hardware utilization of VLSI building diagram. A repression examination on gear utilization of FM0 and Manchester encodings is discussed in detail. In this paper, the totally reused VLSI designing using SOLS system for both FM0 and Manchester encodings is proposed. The SOLS strategy sheds the obstruction on hardware use by two focus systems: extend insignificant retiming and alter justification operation sharing. The modify method of reasoning operation sharing successfully merges FM0 and Manchester encodings with the unclear justification parts. The encoding limit of this paper can totally support the DSRC standards of America, Europe, and Japan.

This paper develops a totally reused VLSI configuration, and in addition shows a forceful execution differentiated and the present works .The proposed sparse kogge implementation results less area and reduced power than the existing kogge implementation. In future there may be a chance to modify the design using some other encoding techniques which will leads some more reduction in power consumption. In future, there is also a chance to develop a LAYOUT using cadence tool for this design due to technology node improvement.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology
Vol. 4, Special Issue 2, January 2017

REFERENCES

[1] J. B. Kenney, "Dedicated short-range communications (DSRC) standards in the United States," *Proc. IEEE*, vol. 99, no. 7, pp. 1162–1182, Jul. 2011.

[2] J. Daniel, V. Taliwal, A. Meier, W. Holfelder, and R. Herrtwich, "Design of 5.9 GHz DSRC-based vehicular safety communication," *IEEE Wireless Commun. Mag.*, vol. 13, no. 5, pp. 36–43, Oct. 2006.

[3] P. Benabes, A. Gauthier, and J. Oksman, "A Manchester code generator running at 1 GHz," in *Proc. IEEE, Int.*

[4] *Conf. Electron., Circuits Syst.*, vol. 3. Dec. 2003, pp. 1156–1159.

[5] Christo Ananth, [Account ID: AORZMT9EL3DL0],"A Detailed Analysis Of Two Port RF Networks - Circuit Representation [RF & Microwave Engineering Book 1]", Kindle Edition, USA, ASIN: B06XQY4MVL, ISBN: 978-15-208-752-1-7, Volume 8, March 2017, pp:1-38.

[6] M. A. Khan, M. Sharma, and P. R. Brahmanandha, "FSM based Manchester encoder for UHF RFID tag emulator," in *Proc. Int. Conf. Comput., Commun. Netw.*, Dec. 2008, pp. 1–

[7] M. A. Khan, M. Sharma, and P. R. Brahmanandha, "FSM based FM0 and Miller encoder for UHF RFID tag emulator," in *Proc. IEEE Adv. Comput. Conf.*, Mar. 2009, pp. 1317–1322.

[8] J.-H. Deng, F.-C. Hsiao, and Y.-H. Lin, "Top down design of joint MODEM and CODEC detection schemes for DSRC coded-FSK systems over high mobility fading channels," in *Proc. Adv. Commun. Technol.* Jan. 2013, pp. 98–103.

[9] I.-M. Liu, T.-H. Liu, H. Zhou, and A. Aziz, "Simultaneous PTL buffer insertion and sizing for minimizing Elmore delay," in *Proc. Int. Workshop Logic Synth.*, May 1998, pp. 162–168.