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DESIGN AND ANALYSIS OF BIDIRECTIONAL ACTIVE BUCK PFC RECTIFIER WITH MULTILEVEL MULTI-OUTPUT USING FUZZY CONTROLLER

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ABSTRACT-A new family of buck type PFC (power factor corrector) rectifier with Fuzzy controller is proposed in this paper, which can be operated in CCM (continuous conduction mode) and at the input side generates multilevel voltage waveform. In this paper we are using the fuzzy controller compared to other controllers i.e. The fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. In this paper a 5-level rectifier operating in buck mode has been proposed which is called HPUC as a slight modification to PUC multilevel converter. The proposed HPUC (Hani Packed U-Cell) rectifier operates in boost mode while splitting the output voltage terminals to have multiple-output with reduced voltage levels as buck mode. By using the fuzzy controller for a nonlinear system allows for a reduction of uncertain effects in the system control and improve the efficiency. Dual DC output terminals are provided to have a 5-level voltage waveform at the input points of the rectifier where it is supplied by a grid via a line inductor. Producing different voltage levels reduces the voltage harmonics which affects the grid current harmonic contents directly. The performance of the proposed transformer-less, reduced filter and multilevel rectifier topology has been analyzed by using the simulation results.

Index Terms—Buck PFC rectifier, Hani packed U-cell (HPUC), multilevel converter, Fuzzy controller, packed U-cell (PUC5), power quality.

INTRODUCTION

To overcome the input AC voltage and current power factor issue, PFC rectifiers have been proposed in this paper. Based on their output DC voltage amplitude these rectifiers can be divided into two types. Such as PFC buck rectifier and PFC boost rectifier. If the output DC voltage level is less than the input AC peak voltage value, it is called a PFC buck rectifier and a PFC boost rectifier generates a DC voltage greater than the AC peak voltage [4]. In this paper, a new family of bidirectional bridgeless buck PFC rectifiers is introduced which is an efficient cure to all above-mentioned issues. Supplying multiple-output terminals result in producing a multilevel voltage waveform at the rectifier input that reduces the harmonic content of the rectifier voltage and consequently the grid current harmonic without using large inductive filters at the AC side.

PFC buck rectifiers are mainly known with their discontinuous conduction mode (DCM) which complicates formulating the output voltage. Large-size LC filters at the output as well as non-removable AC side filters are inherent disadvantages of PFC buck rectifiers. To generate a reduced DC voltage is combination of diode-bridge and dc-dc buck converter in which the AC voltage is rectified by that diode-bridge and then DC voltage is stepped down at a desired level by the chopper. Such two stage structures present more power losses, low efficiency and high manufacturing costs in medium and high power applications.

To have a reduced DC voltage at the output, bridgeless PFC boost rectifiers are usually connected to the main grid after a step-down transformer [12]. Therefore, to have a 125 V DC at the output terminal Boost mode operation of the overall system helps removing bulky filters from both sides specially the DC side inductor.

PROPOSED PFC BUCK RECTIFIER TOPOLOGY AND OPERATION PRINCIPLE

The proposed rectifier topology has been shown in figure 1.

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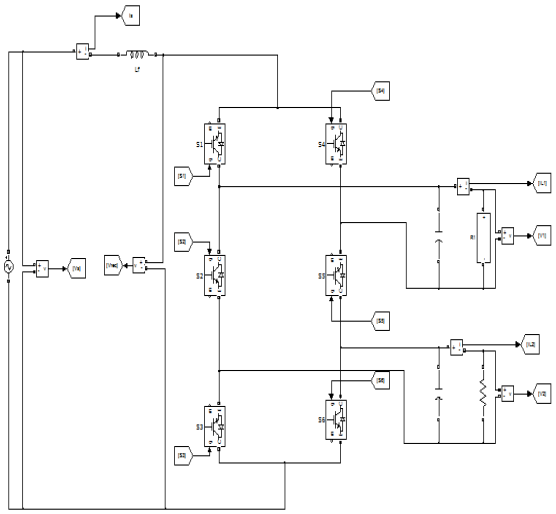

Fig. 1. Proposed HPUC five-level buck PFC rectifier

It has 6 active switches and two output DC terminals. The output terminals are providing voltages V1 and V2 to loads that should be identical as E to have a five-level voltage waveform at the rectifier input. Rectifier input voltage is measured at points 'a' and 'd' as Vad. The switching states associated to the introduced rectifier have been listed in table I.

TABLE I
SWITCHING STATES OF THE PROPOSED HPUC FIVE-LEVEL BUCK PFC RECTIFIER

Switching State	S_1	S_2	S_3	S_4	S_5	S_6	V_{ad}	V_{ad} voltage levels
1	1	0	1	0	1	0	V_1+V_2	+2E
2	1	0	0	0	1	1	V_1	+E
3	0	0	1	1	1	0	V_2	+E
4	1	1	1	0	0	0	0	0
5	0	0	0	1	1	1	0	0
6	1	1	0	0	0	1	$-V_2$	–E
7	0	1	1	1	0	0	$-V_1$	–E
8	0	1	0	1	0	1	$-V_1-V_2$	–2E

The proposed HPUC rectifier is a modification to the well known PUC converter in which the lower U-cell components are connected in reverse direction. The PUC converter was proposed as an inverter to generate 7-level voltage waveform while using a single isolated DC source and a controlled capacitor

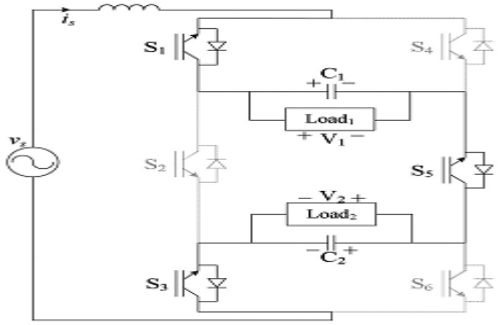

Fig. 2. Operating sequences and conducting paths of the proposed HPUC five-level buck rectifier State1 V1+V2 =+2E.

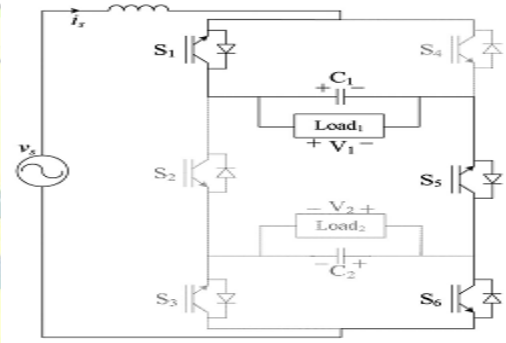

Fig. 2. Operating sequences and conducting paths of the proposed HPUC five-level buck rectifier State2 V1 =+E

It is clear from table I that each pair of switches S1-S4, S2-S5 and S3-S6 is working in complementary manner. All switching states and associated conducting paths are shown in figure 2 which will be used in voltage regulator design section.

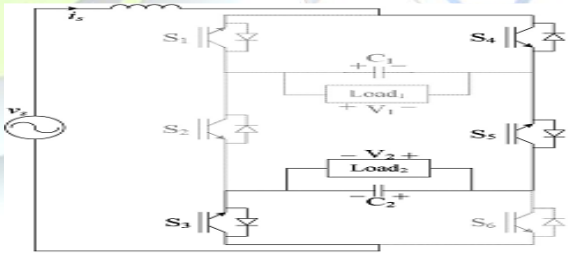

Fig. 2. Operating sequences and conducting paths of the proposed HPUC five-level buck rectifier State3: V2 =+E.

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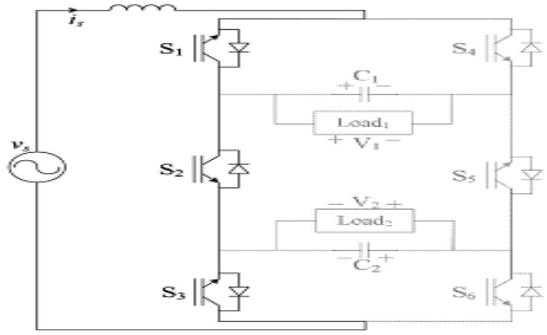

Fig. 2. Operating sequences and conducting paths of the proposed HPUC five-level buck rectifier

State4 :V2 =+E.

By controlling output DC voltages, Vad would have five levels including ±2E, ±E, 0 that the maximum value is +2E. The principal concept of proposing this topology as a buck rectifier relies on this maximum value of Vad which should be more than the AC source peak value (vs max). The following relations can be written, accordingly.

$$V_{ad} \geq v_s \rightarrow 2E \geq V_{S\,max} \rightarrow E \geq \frac{V_{S\,max}}{2} \qquad (1)$$

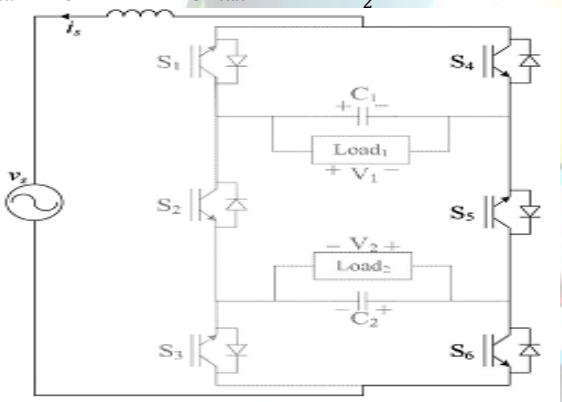

Fig. 2. Operating sequences and conducting paths of the proposed HPUC five-level buck rectifier

State5 : 0

For instance, if RMS voltage of the AC source is 120V, then the maximum value would be 170V and the following relations would be obtained. To maintain the stable operation of the converter in buck mode, the maximum generating DC voltage is set at vs max which would be 170 V here.

$$\frac{V_{S\,max}}{2} \leq E \leq V_{S\,max} \rightarrow 85V \leq E \leq 170V \qquad (2)$$

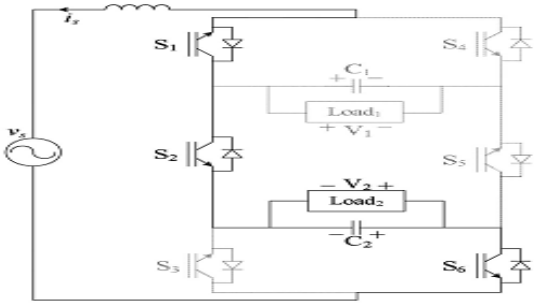

Fig. 2. Operating sequences and conducting paths of the proposed HPUC five-level buck rectifier

State6 : −V2 =−E.

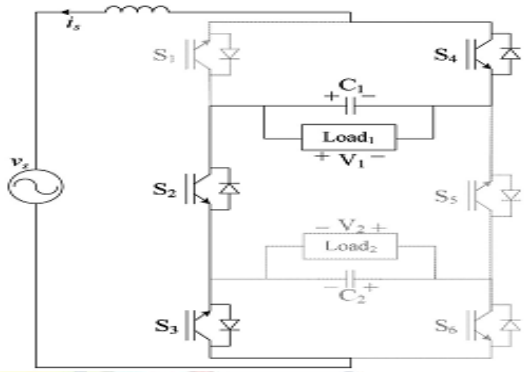

Fig. 2. Operating sequences and conducting paths of the proposed HPUC five-level buck rectifier

State7 :−V1 =−E.

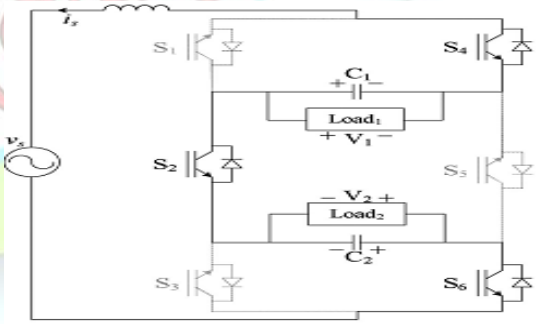

Fig. 2. Operating sequences and conducting paths of the proposed HPUC five-level buck rectifier

State8 :−V1−V2 =−2E.

As mentioned above, this rectifier is a boost converter in grid point of view due to generating peak voltage of V1+V2 at the input (Vad) which is always equal or greater than the vs max. On the other hand, by splitting the produced DC voltage between two output terminals, each one would have half voltage amplitude so their amplitude are always less than or equal to the vs max that guarantees the buck mode operation of proposed rectifier from loads points of

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view. It could be concluded that by using two output terminals, the grid is deluded by the converter.

Therefore, the stepped down DC voltages are achieved however the overall rectifier is in step-up mode. As results, the bulky inductor at DC side as well as the capacitor filter at AC side of conventional PFC buck rectifiers would be removed. Moreover, low harmonic Vad and also low THD line current (is) are attained even when the proposed rectifier is running at low switching frequency leads to low power losses and high efficiency.

SWITCHING TECHNIQUE AND INTEGRATED VOLTAGE REGULATOR

Due to utilizing more than one DC capacitor in multilevel converter topologies, regulating and balancing their voltages is the most challenging part of the controller. Redundant switching states can play an important role in facilitating the controller duty of regulating the output DC terminals voltages. In this regard, the switching states should be analyzed precisely to find the charging and discharging path for capacitors. Table II lists such investigation results on the proposed rectifier switching states.

TABLE II
EFFECT OF SWITCHING STATES ON OUTPUT DC CAPACITORS

Switching State	Line Current Sign	V_{ad}	V_{ad} voltage levels	Effect on C_1	Effect on C_2
1	$i_s > 0$	V1+V2	+2E	Charging	Charging
2	$i_s > 0$	V1	+E	Charging	Discharging
3	$i_s > 0$	V2	+E	Discharging	Charging
4	$i_s \geq 0$	0	0	Discharging	Discharging
5	$i_s \leq 0$	0	0	Discharging	Discharging
6	$i_s < 0$	-V2	-E	Discharging	Charging
7	$i_s < 0$	-V1	-E	Charging	Discharging
8	$i_s < 0$	-V1-V2	-2E	Charging	Charging

It is clear that redundant switching states of 2, 3, 6 and 7 can help regulating capacitors voltages beneficially. Hence, the switching pattern of the PWM block would be modified in order to decide between switching states 2 or 3 when the line current is positive and the +E voltage level should be generated at the output. It means that if V1 is less than V2 then switching state 2 would be applied to switches and if V1 is more than V2 then the output pulses would be generated by switching state 3. The same process is defined to choose between switching states 6 or 7 when line current is negative and output voltage should be –E.

All these actions are taken inside the PWM block shown in figure 3.

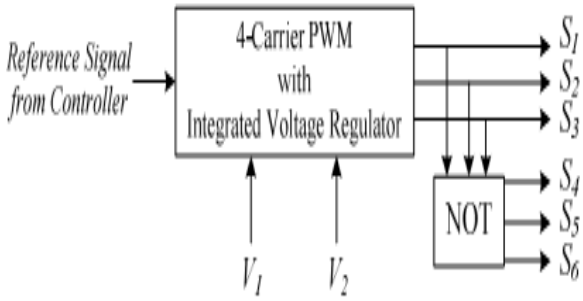

Fig. 3. Input/output signals of PWM block with integrated voltage regulator.

Moreover, the reference signal is first modulated by 4 vertically shifted carriers in order to determine the associated voltage level and then the required pulses are sent to the switches considering capacitors voltages and redundant switching states .

All these procedures are to simplify regulating DC voltage terminals. Therefore, the voltage control loop would generate less error due to balancing the DC voltages by the redundant switching states. Figure 3 depicts the PWM block input/output signals in detail.

CONVENTIONAL CONTROLLER

A cascaded PI controller has been applied to regulate the three state space variables including capacitors voltages (V1 & V2) as well as grid current (is) and to provide a unity power factor operation of the five-level rectifier [24]. Figure 4 shows the block diagram of the implemented controller. A phase lock loop (PLL) block is used to extract the voltage angle and generate the synchronized current reference is* which should be drawn by the rectifier in order to ensure the power factor correction.

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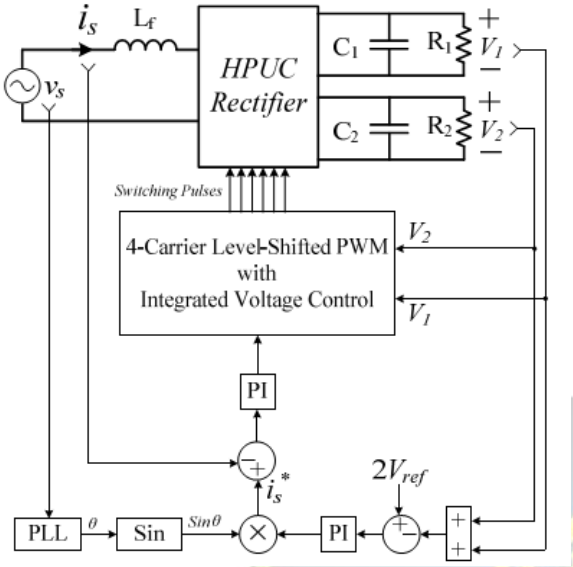

Fig. 4. Block diagram of the HPUC rectifier and conventional controller

Concluding that the controller is regulating total DC voltage as 2Vref using the flowing current through the converter while the switching technique and redundant states would charge and discharge the capacitors equally to have identical voltage levels (Vref) at the DC output terminals. That decoupled voltage control helps balancing capacitors voltages even in faulty conditions where the switching actions could not balance two DC voltages while the sum of DC voltages is regulated at 2Vref. This mode helps preventing any uncontrolled charging up of the capacitors to an unlimited level.

POWER BALANCE ANALYSIS

Noticing to the HPUC rectifier configuration in the figure 1, it is clear that S2 and S5 have voltage rating of two times more than the other four switches (S1, S3, S4, and S6).

Therefore, S2 and S5 can be split into two series switches in order to suffer equal voltage rating as shown in figure 5. The point (m) is chosen to split two cells which are kind of full bridge modules. Similarly to the work performed on cascaded H-bridge (CHB) multilevel converter [27, 28], the following analysis is done to show the power balance ratio between two independent loads connected to the proposed rectifier.

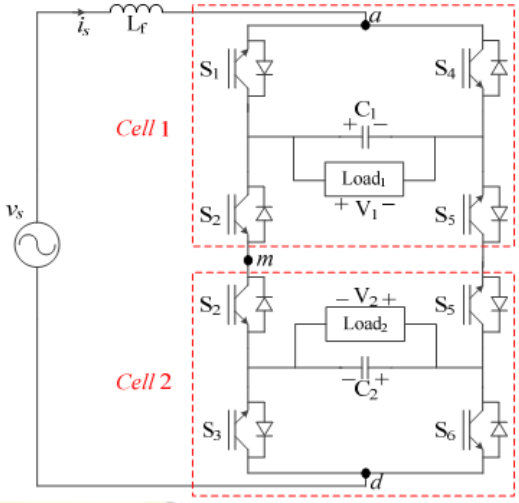

Fig. 5. Split configuration of the HPUC rectifier into two cells for power balance analysis

The following equation is visible on the rectifier structure:

$$V_{ad} = V_{am} + V_{md} \quad (3)$$

Therefore an extended representation of the HPUC rectifier topology shows that the latter is formed by two series cells (Cell 1 and Cell 2). Each cell generates a DC voltage to supply the load; however the common switches and current paths do not allow each cell to operate separately. To continue with the analysis, following definitions are provided:

vf = RMS (Vad) : rectifier RMS voltage

v s = Grid RMS voltage

vL = RMS (VL) : Line Inductor RMS voltage

Moreover, since each cell voltage (Vam & Vmd) are 3-level waveforms including 0 and ±E volts, their RMS values are defined as:

v1 = RMS (Vam) = 0.7797×m1×V1

v2 = RMS (Vmd) = 0.7797× m2×V2

Where, m1 and m2 are the modulation indexes of each cell that are between 0 and 1. So their maximum value would be defined as:

vmax1 = 0.7797V1

vmax2 = 0.7797V2

It should be noticed that these maximum values of RMS voltages are obtained in case of two separately working cells. The one line diagram of the HPUC rectifier can be drawn as shown in figure 6-a. By neglecting circuit power losses and capacitor energy consumption, it can be said that the power consumed in Cell 1 is P1 and similarly for Cell 2 power is P2. The total power is drawn from the grid as P. They can be formulated as below:

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$$P_1 = \frac{V_1^2}{R_1}, P_2 = \frac{V_2^2}{R_2}$$

$$P = v_s i_s = P_1 + P_2 \quad (4)$$

From Eq. (4) and since DC voltages are controlled, this yield to Eq. (5):

$$\frac{P_1}{P_2} = \frac{R_2}{R_1} \quad (5)$$

In the HPUC rectifier, the buck mode of operation is proposed where V1 + V2 = Max(Vad). Therefore considering RMS values, the following relation is achieved:

$$v_1 \le v_f, v_2 \le v_f, v_1 + v_2 = v_f \quad (6)$$

Based on voltage relations, the phasor diagram of the rectifier can be drawn as in figure 6-b.

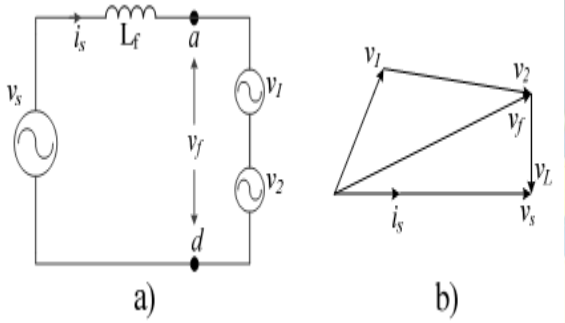

Fig. 6. a) one line diagram of the HPUC rectifier b) Phasor diagram of the system voltages

Moreover, for the maximum voltage of each cell the following relation can be written [28]:

$$v_{max1} \le v_f, v_{max2} \le v_f, v_{max1} + v_{max2} \le v_f \quad (7)$$

The maximum voltages that can be generated by each cell would produce the maximum power that can be delivered to the loads (P1 & P2) in a stable operation. Thus, the diagram shown in figure 7-a is obtained and the shaded area shows the area where maximum power can be delivered to loads while the rectifier works in stable mode. It means that the DC voltages are equally balanced and the input grid current is locked to the grid to deliver only active power.

Based on figure 7-a, v1 and v2 can be placed in the shaded area so the boundary would be the maximum and minimum limits for those voltages that gives the maximum and minimum power generated by each cell. Since the rectifier should always draw active power from the grid, therefore the minimum and maximum limits are projected on the x-axis to ensure the unity power factor operation as 0° phase shift with current which is illustrated in figure 7-b.

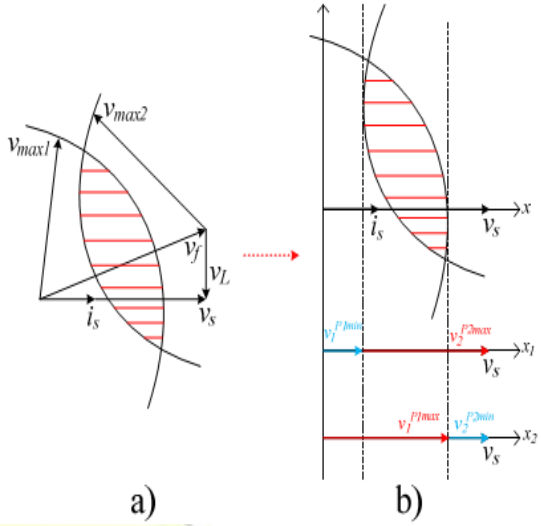

Fig. 7. a) stable operation area of the HPUC rectifier b) Minimum and maximum power generated by each cell and associated voltages

Based on above explanation and figure 7, power relations are extracted for each cell power as Eq. (8).

$$P_{1max} = \frac{V_1^{P_{1max}}}{v_s} P$$

$$P_{1min} = \frac{v_s - v_2^{P_{2max}}}{v_s} P$$

$$P_{2max} = \frac{V_2^{P_{2max}}}{v_s} P$$

$$P_{2max} = \frac{v_s - v_1^{P_{1max}}}{v_s} P \quad (8)$$

Where, v1P1max is the cell voltage with maximum possible power delivering to the load. Other variables have the same definitions. Since two DC voltages are identical, minimum/maximum powers of two cells would be equal. Assuming V1 = V2 = 125V, the following values would be obtained:

$$P_{1max} = P_{2max} = \frac{125 * 0.7797}{120} P = 0.8121P$$

$$P_{1min} = P_{2min} = \frac{120 - 125 * 0.7797}{120} P = 0.1878P \quad (9)$$

Based on the above values, it can be concluded that each cell can have a specific maximum and minimum power as a portion of the input total power. Therefore, the highest difference between two cells power would be in a situation where the Cell 1 takes P1min (or P1max) and the Cell 2 consumes P2max (or P2min). Thus, the maximum power ratio between two cells and

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International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 16, April 2017

consequently the power ratio between two DC loads can be obtained as:

$$\frac{R_2}{R_1} = \frac{P_{2max}}{P_{1min}} = 4.32 \qquad (10)$$

Due to symmetrical configuration of the HPUC rectifier, this ratio can be used for R1/R2 similarly.

III. FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC.

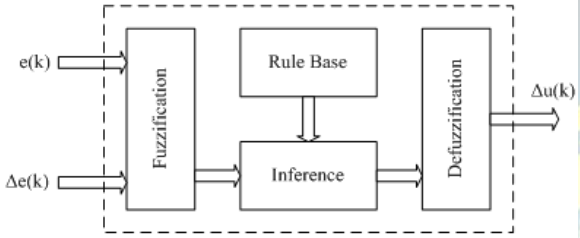

Fig.8.Fuzzy logic controller

The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method. Christo Ananth et al.[6] presented a brief outline on Electronic Devices and Circuits which forms the basis of the Clampers and Diodes.

TABLE I: Fuzzy Rules

Change in error	Error						
	NB	NM	NS	Z	PS	PM	PB
NB	PB	PB	PB	PM	PM	PS	Z
NM	PB	PB	PM	PM	PS	Z	Z
NS	PB	PM	PS	PS	Z	NM	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PM	PS	Z	NS	NM	NB	NB
PM	PS	Z	NS	NM	NM	NB	NB
PB	Z	NS	NM	NM	NB	NB	NB

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The Partition of fuzzy subsets and the shape of membership CE(k) E(k) function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor.In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}} \qquad (11)$$

$$CE(k) = E(k) - E(k\text{-}1) \qquad (12)$$

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output

The set of FC rules are derived from

$$u=-[\alpha E + (1-\alpha)*C] \qquad (13)$$

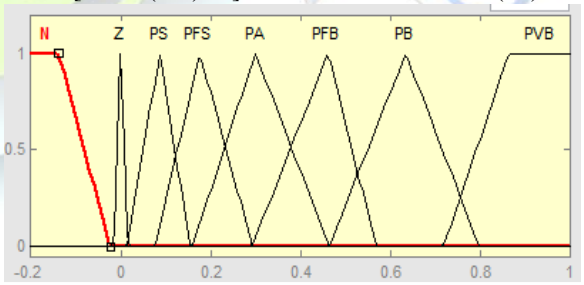

Fig 9. input error as membership functions

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International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
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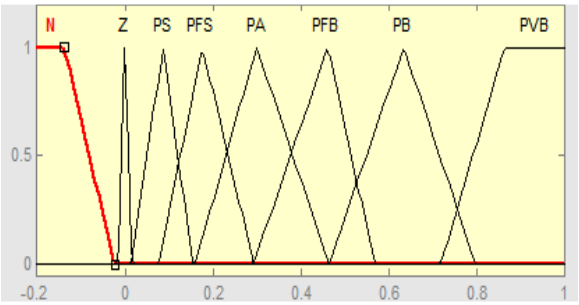


Fig 10. change as error membership functions

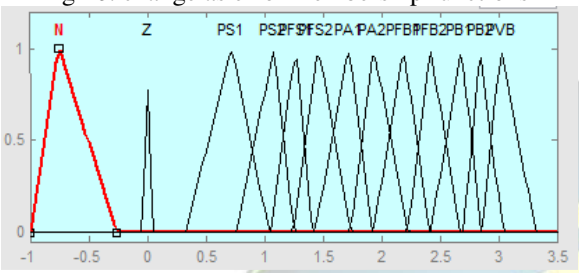


Fig.11 output variable Membership functions

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable.

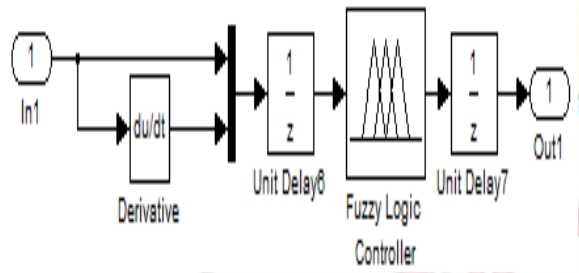


Fig 12.fuzzy logic controller in simulation.

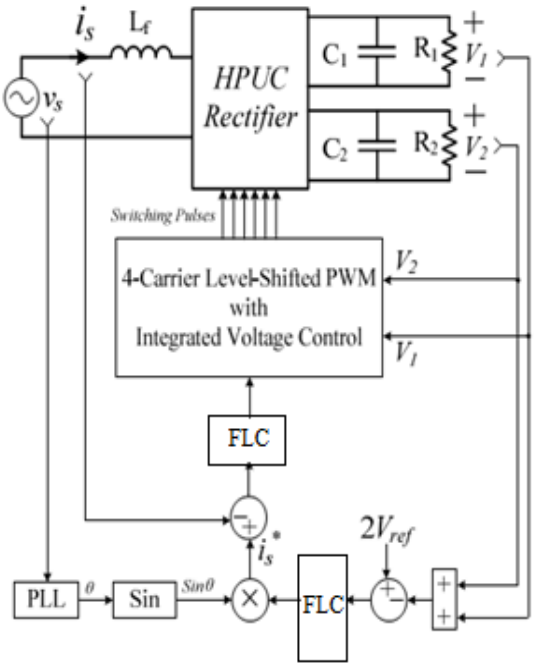
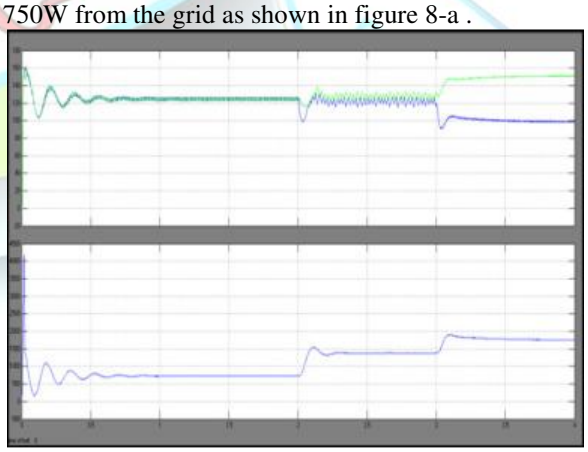


Fig. 13. Block diagram of the HPUC rectifier and proposed controller

It should be noted that all simulation parameters except loads were same as experimental ones listed in Table III. As shown in figure 8, three steps have been applied.

At first step, R1 = R2 = 43Ω so R2/R1 = 1 and rectifier works in stable mode drawing almost 750W from the grid as shown in figure 8-a .



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International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 16, April 2017

Fig.14. Stable and unstable operation of the HPUC rectifier

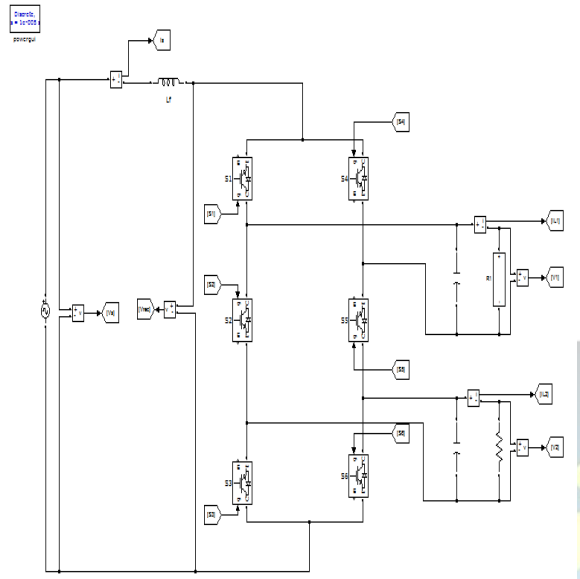

Fig.15 Simulation block diagram of proposed method

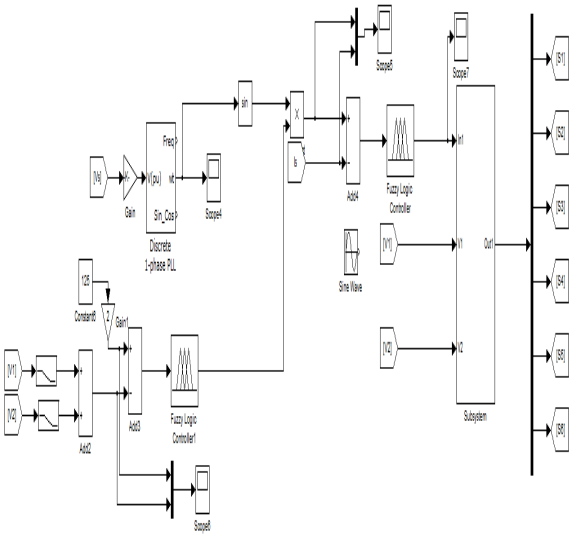

Fig.16 Control block diagram of proposed method with Fuzzy controller

TABLE III
SIMULATION SYSTEM PARAMETERS

AC Grid Voltage	120 V RMS
AC Grid Frequency	60 Hz
Interface Inductor	2.5 mH
DC voltages (V_1&V_2)	125 V
DC Capacitors (C_1&C_2)	2500 uF
DC Load 1	53Ω
DC Load 2	80Ω
Switching Frequency	2 kHz
Current Controller Gains	$k_p = 0.8$, $k_i = 0.1$
Voltage Controller Gains	$k_p = 0.01$, $k_i = 5$

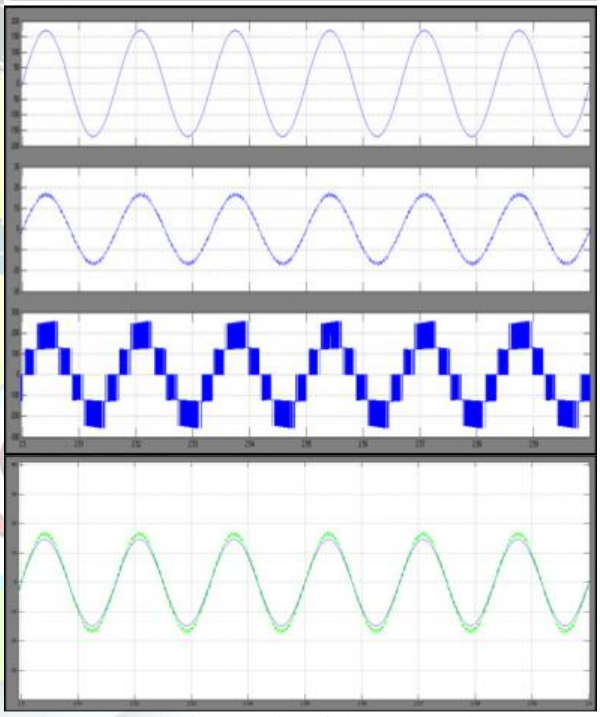

Fig. 17.Simulation results of the proposed HPUC rectifier connected to 120V RMS AC grid and supplying two DC loads at 125V DC. a) Output DC voltages regulated at 125V with grid side synchronised voltage and current b) DC loads currents with grid side synchronised voltage and current c) 5-Level voltage waveform at the input of the HPUC rectifier d) RMS and THD values of the AC side synchronised voltage and current waveforms

At first, the change has been intentionally made in Load1. As it is clear from figure 10, two output DC voltages and load2 current (il2) do not vary during change in load1. DC voltages are regulated successfully as well as DC current

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reduction in figure 10 proves the change in load1 while the second load voltage/current is not affected remarkably.

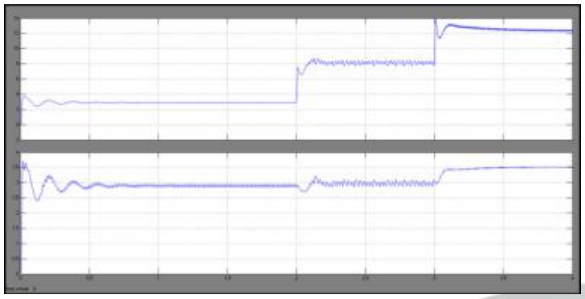

Fig.18 simulation diagram of load currents(IL1 and IL2)

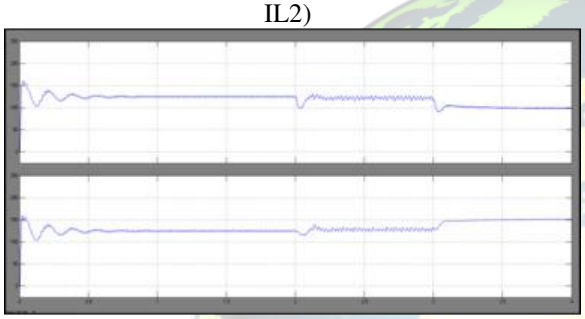

Fig.19 Simulation diagrams of Voltages(V1 and V2)

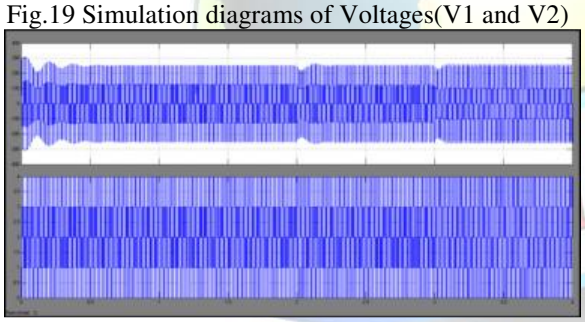

Fig.20. Supply voltage variation while the output DC voltages

Provided results in changing conditions prove the good dynamic performance of the proposed HPUC bridgeless 5- level buck PFC rectifier in generating DC voltage from AC grid. It can be concluded that the HPUC topology can operate as a universal PFC rectifier in buck mode of operation at low switching frequency results in low power losses and high efficiency interesting for industrial applications.

CONCLUSION

In this paper a 5-level rectifier operating in buck mode with fuzzy controller has been proposed, which is called HPUC as a slight modification to PUC multilevel converter. The proposed HPUC rectifier is a modification to the well known PUC converter in which the lower U-cell components are connected in reverse direction. The PUC converter was proposed as an inverter to generate seven-level voltage waveform, while using a single isolated dc source and a controlled capacitor. In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. The FLC comprises of three parts: fuzzification, interference system and defuzzification To generating multilevel waveform leads to reduced harmonic component of the voltage waveform and consequently the line current. It also aims at operating with low switching frequency and small line inductor that all in all characterizes low power losses and high efficiency of the HPUC rectifier. In this paper we are using the fuzzy controller compared to other controllers i.e. The fuzzy controller is the most suitable for the human decision-making mechanism, providing the operation of an electronic system with decisions of experts. By using the simulation results we can analyze the proposed method.

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