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SFCL WITH 5 – LEVEL INVERTER USING FOUR TYPES OF HVDC CIRCUIT BREAKERS

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ABSTRACT: In this paper, superconducting fault current limiter (SFCL) is proposed in power systems to limit the fault, SFCL is a device that utilizes superconductors to instantaneously limit or reduce transient electrical surges that may occur in distribution and transmission networks. In this paper we are increasing the levels of inverter. If we increase the level then the efficiency will be improved and also accuracy will be improved. One good solution is, combining the fault current limiting technologies with DC breaking topologies. With the utilization of resistive Superconducting Fault Current Limiter (SFCL) on different types of HVDCCB, can estimate the impact of fault current limiters on conventional DC breakers together. The simulation had done on resistive SFCL and it was applied to the DC breakers to verify both the interruption characteristics and distributed energy across HVDC CB. The major advantage is that the output waveform is more close to sinusoidal and harmonics can be reduced if higher the number of the level, approximately sin wave. Results of simulation, interruption time, fault current, energy dissipation across the HVDC CB can be decreased with SFCL. By using the simulation results we can analyze the proposed method.

Key Words — DC Fault current Interruption, HVDC Fault, HVDC Circuit Breaker, 5-level inverter, MTDC, Resistive Superconducting Fault Current Limiter.

INTRODUCTION

The utilization of SFCL in power system provide most effective way to limit the fault current and results in considerable saving from not having to utilize high capacity circuit breakers. Superconducting materials are used in Superconducting fault current limiters to limit the current directly or to supply a DC bias current that affects the level of magnetization of a saturable iron core. Recently we are step ahead in commercial application of Multi Terminal HVDC (MTDC) networks, which will considered an optimum solution for renewable energy transmission and power grid inter-connection, the reliability of HVDC systems are good [1], [2]. SFCL and Four types of DC breakers were modeled, and the fault current interruption characteristics were compared to get which type of HVDC CBs most suitable for the application of SFCL, considering the current interruption capabilities and reduction of total energy dissipation during DC fault.

Conventional HVDC systems can be sufficiently protected by mechanical circuit breakers located on the AC side [3]; however, a selective coordination protection scheme that isolates faulted lines in MTDC to prevent the blackout of the entire grid system [4]. HVDC circuit breakers (HVDC CB) are widely considered a key technology in the implementation of the MTDC system.

The common three topologies for multilevel inverters are as follows:

1) Diode clamped (neutral clamped),
2) Capacitor clamped
3) Cascaded H-bridge inverter.

A multilevel inverter is power conversion device that produces an output voltage in the needed levels by using DC voltage sources applied to input [3]. It consist capacitors are connected in series to separate the DC bus voltage in different levels. This topology is similar to that of diode-clamped multilevel inverter, but it consist capacitors instead of the diodes to clamp the voltage levels. The 5- level diode clamped multilevel inverter have switches, a single capacitor, diodes are used, so output voltage is half of the input DC.

This paper focuses on a factor for resistive type SFCL, which is useful to improve the reliability of the system, with the transient stability study based on the equal area criterion, the performances of the proposed SFCL to reduce the level of fault currents. Advantages by using multilevel inverter are: the output voltages and input currents with low THD, the reduced switching losses due to lower switching frequency, good electromagnetic compatibility owing to lower, high voltage capability due to lower voltage stress on switches.

The fault current interruption can be easily achieved by zero-current crossing. Where in AC circuit breakers can interrupt a fault current in natural zero current, artificial current zero should be implemented for DC breakers to enable fault current interruption. To achieve the zero-crossing condition of DC fault current, a forced current reduction method should be used. Various types of HVDC CB are summarized in [6], some of which have revealed prototypes and successful test results. Existing DC current breaking topologies focusing solely on methods to achieve artificial current zero should be somewhat achieved [7]. One feasible solution is fault current limiting technologies with DC breaking topologies.

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The Resistive SFCL acknowledged as an effective solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault [8]. So, the combined application of SFCL and HVDC CB could be an alternative solution capable of decreasing the dissipated fault energy and improving the performance of HVDC CBs. In order to estimate the performance of combined-application of SFCL on HVDC CBs, simulation studies were performed.

Applications of multilevel inverter

- Static var compensation
- Variable speed motor drives
- High voltage system interconnections
- High voltage DC and AC transmission lines

MODELLING OF TEST-BED, SFCL AND HVDC CBS

HVDC Test-bed Model

We are analyze the impact of SFCL on various types of HVDC CBs, a test-bed model was designed as shown in Fig. 1. The simple, symmetrical, monopole, point-to-point, 2-level, half-bridge HVDC system was utilized to get the interruption performance of the DC fault current in detail.

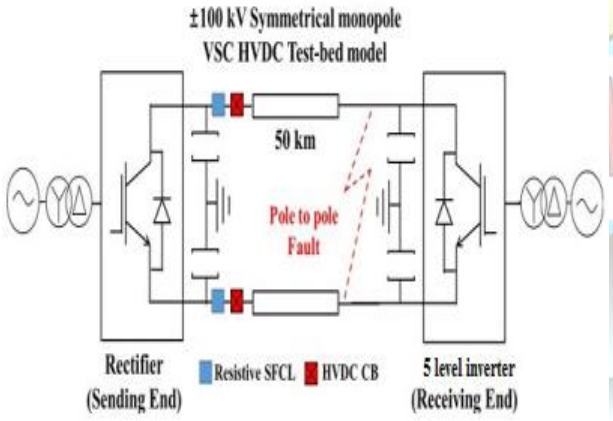

Fig.1. 2-level point-to-point HVDC test-bed model (Vac : AC voltage, Rac, Lac: system impedance of AC, Lp: Phase reactor)

Resistive Superconducting Fault Current Limiter

According to the resistive SFCL, which is depend upon the quenching phenomena of superconductors have been developed and installed in medium- and high-voltage systems [10].

Therefore the theoretical analysis of a resistive SFCL [8], the quenching phenomena of SFCL can be expressed as:

$$\begin{Bmatrix} R_{SFCL}(t) = 0 & (t < t_{quenching}) \\ R_m\left(1 - exp\left(-t/T_{SC}\right)\right) & (t_{quenching} < t) \end{Bmatrix} \quad (1)$$

Where, R_m is the maximum quenching resistance and T_{sc} is the time constant for the transition to the quenching state.

The maximum quenching resistance R_m is 10 Ω. Until now, there is no practical application of DC SFCL. Therefore, to determine the transition time, time from zero resistance to maximum quench resistance of resistive SFCL, the transition time of AC SFCL was referred. It should be determined within 1/2 cycle, and therefore the transition time of designed SFCL was assumed to 2 ms. Therefore, in order to get nearly 10 ohms of R_q (quenching resistance) within 2 ms, the value of T_{sc} was find to 0.25 ms. The quenching characteristics of the designed SFCL based on (1) are shown in Fig. 2.

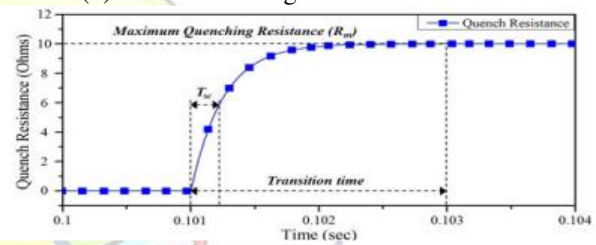

Fig.2. Quenching characteristics of the designed resistive SFCL with respect to time.

Arc Modeling

According to the HVDC CB topologies which are classified as mechanical CB (MCB), passive resonance CB (PRCB), inverse current injection CB (I-CB) and Hybrid DC CB (HDCCB) [7]. In which the arc type such as mechanical, passive resonance DC CB, the implementation of arc dynamics is a major concern in the design for an accurate simulation model. The black-box arc model, which represents the arc dynamics by calculating the differential equation of the arc conductance, was designed.

In our simulation model, the modified Mayr black-box arc model was used for MCB, which assumes arc conductance, g, arc cooling power, $P_c(g)$, and arc time constant, τ, as shown.

$$\frac{1}{g}\frac{dg}{dt} = \frac{dlng}{dt} = \frac{1}{\tau(g)}\left(\frac{ui}{P_c(g)} - 1\right) \quad (2)$$

The advantage of the modified Mayr arc model is able to determine the breaking capability of MCB by controlling $P_c(g)$. The following equations and parameters in Table I were used to determine the $P_c(g)$ and τ:

$$P_c(g) = P.P_0.g^a \quad (3)$$

$$\tau(g) = \tau_0.g^b \quad (4)$$

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While various black-box arc models already exist, they only consider the continuous model environment. Due to the complicated nature of the system, a discrete model is required to accomplish an efficient simulation. To implement the continuous black-box arc model into in discrete model, (2) was transformed into integral form as (5) and the simulation model was designed as shown in Fig. 3.

$$g = \int_0^t \frac{1}{\tau}\left(\frac{i^2}{P_c(g)} - g\right) dt \qquad (5)$$

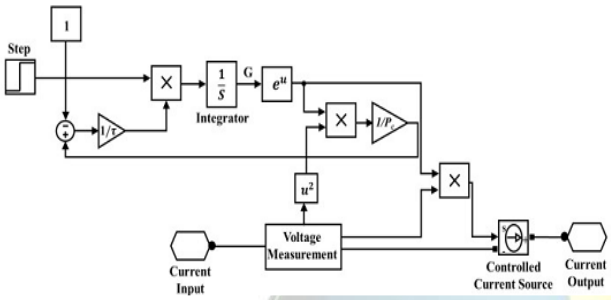

Fig. 3. The modified Mayr black-box arc model designed using Matlab/ Simulink for discrete simulation environment

Table.1
Parameters Of Designed Black-Box Arc Model

parameter	Value
P0	0.393MW
P	70 bar
A	0.25
T0	15µsec
b	0.5

Modelling Of HVDC CBs

The concepts of HVDC CB are classified in CIGRE WG. B4.52 according to the method to achieve artificial current zero to interrupt fault current [15]. The simulation models of HVDC CBs in our simulation were designed as follows;

Mechanical CB (MCB):

In MCB the DC current is reduced by increasing the arc voltage to higher value than the system voltage. By utilizing the black-box arc model, the simulation model of MCB was designed as shown in Fig. 4(a). Here assumed the delay time as 10ms for practical approach of simulation.

MCB
(Black-box arc model)

Fig.4. HVDC CB models: the (a) Mechanical CB (MCB)

Passive resonance CB (PRCB):

To dissipate the energy stress across MCB, the secondary path with a series L-C circuit is added as shown in Fig. 4(b).

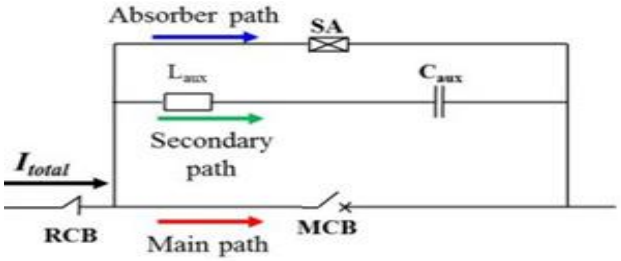

Fig. 4. HVDC CB models: (b) Passive resonance CB (PRCB),

When the fault occurred at 0.1 sec, MCB opens with 10 ms of delay considering opening delay, and then an arc forms across the contacts with increasing arc impedance. The DC current begins to commutate and resonate in the secondary path after the arc impedance exceeds the L-C impedance. When a DC current of the primary path meets zero crossing, a current through the MCB can be interrupted by the extinction of the arc. An additional parallel surge arrester (SA) circuit is supplemented to prevent voltage stress across the PRCB during arc extinction.

Inverse Current Injection CB (I-CB):

However, the pre-charged capacitor via an additional DC power source injects an inverse current into the primary path after the current commutates to secondary path as shown in Fig. 4(c). This can reduce the interruption and oscillation time when compared to that of PRCB. Before a fault, a charging switch (ACB1) and an auxiliary switch (ACB2) maintains closed state. Thereby capacitor can be charged by DC source. When a fault occurs, after an 10 ms delay, MCB and ACB1 contacts open simultaneously. Then the high discharging inverse current from capacitor is supplied to main path. The fault current is rapidly decreased and transient recovery voltage appears between the terminals of I-CB. When the voltage exceeds to the knee voltage of SA, it is triggered to restrain the voltage rise, and it absorbs the fault energy. Therefore, remaining fault energy is exclusively absorbed by SA. If the current reaches to zero, a residual circuit breaker (RCB) opens and the current interruption is complete.

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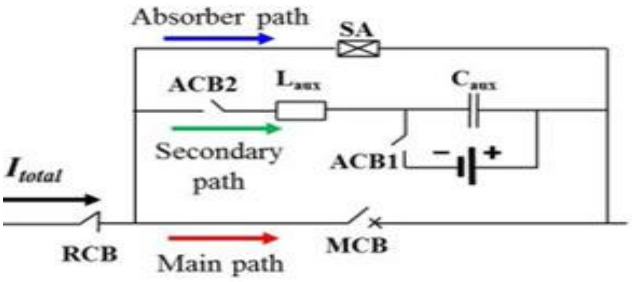


Fig. 4. HVDCCB models:(c) Inverse current injection CB (I-CB)

Hybrid DC CB (HDCCB):

According to the scheme which is widely used as the optimal concept for interrupting DC fault current, was designed as illustrated in Fig. 4(d). The delay times of IGBT was assumed as Δt IGBT = 6 μs in simulation. When a DC fault occurs, the auxiliary DC breakers (ADCB) and fast disconnector are opened sequentially, then the current starts to commutate from the main path to secondary path. After commutation, main DC circuit breakers (MDCB) in secondary path are opened, and total current is reduced because the current flows to the snubber circuit of MDCB until the parallel-connected SA trips. When the voltage across the HDCCB terminals exceed to knee voltage, the SA ignites and forces the DC fault current to zero by absorbing remaining fault energy. Finally, a RCB opens and isolates the DC fault.

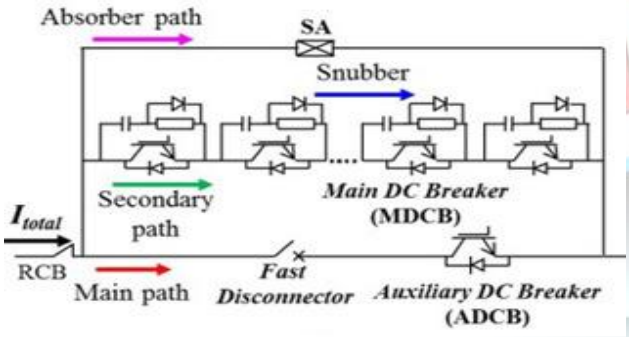


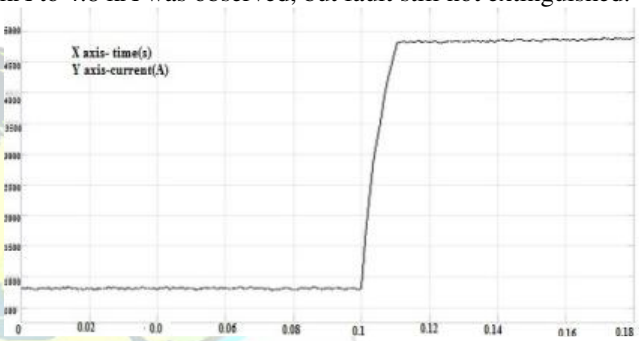
Fig. 4. HVDC CB models: (d) Hybrid DC CB (HDCCB).

SIMULATION ANALYSIS AND DISCUSSION

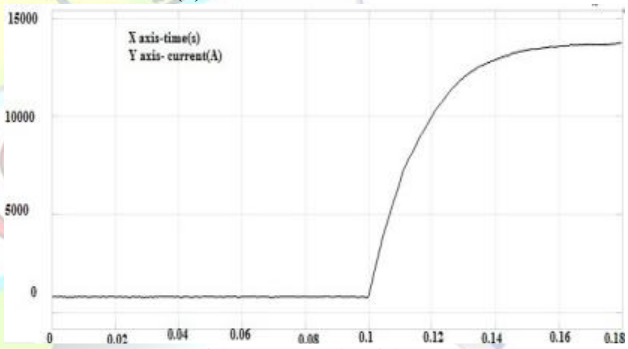
simulations were done to analyze the effects of SFCL on various HVDC CB types for transient fault. Four types of HVDC CB, both with and without SFCLs, were connected at the sending end of the test-bed. Let we consider that a pole-to-pole fault, which is severe fault in HVDC systems, was generated on the receiving end at 0.1 sec. The prospective maximum fault current without any protection devices was 14.7 kA in the designed test-bed. The rising rate of the fault current di/dt during early 10 ms was measured as 589 A/ms. Therefore needed to introduce the application of fast fault current interruption device .

Case 1: Mechanical CB (MCB)

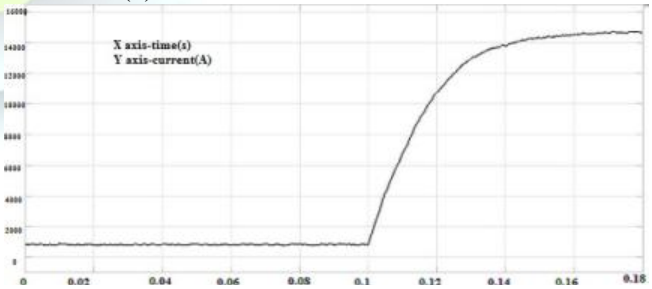
As per fig.5 shows the DC fault interruption performance of the MCB. A maximum prospective fault current was measured as 14.7 kA. Without SFCL, only with mechanical CB, fault current was reduced from 14.7 kA to 13.8 kA. Arc was not extinguished due to low cooling power, Pc(g), and a small current reduction was measured due to the generation of arc resistance. with the utilization of SFCL, a 67.3 % current reduction from 14.7 kA to 4.8 kA was observed, but fault still not extinguished.



(a) With MCB and SFCL



(b) With MCB and without SFCL



(c) Without MCB and without SFCL

Fig. 5. Interruption characteristics of MCB when SFCL was applied

The arc cooling power Pc(g) requirement is more if we use only mechanical CB for fault interruption, may have insulation problem, particularly in high-voltage

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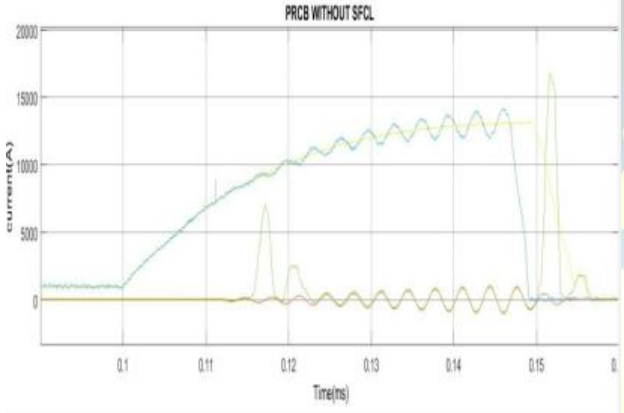
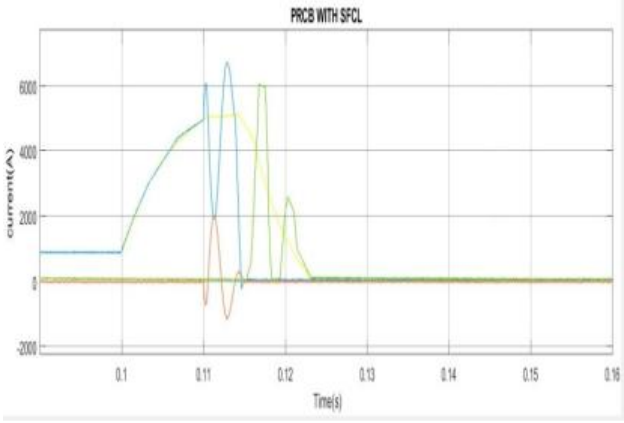
application. Therefore, DC fault interruption was not achieved without the application of SFCL. By seeing it tells about DC fault interruption through only MCB was not an appropriate solution.

Case 2: Passive Resonance CB (PRCB)

fig. 6 shows PRCB performance on DC fault interruption. Without SFCL the maximum fault current intensity (I_{total}) was measured as 13.2 kA, and the maximum current in the main path was 27.5 kA leading to oscillate due to resonance. The total interruption time was 55 ms. In this regard, considering the fast di/dt of the DC fault current, using PRCB alone was not an appropriate solution to clear fault in a short time.



(a) Without SFCL



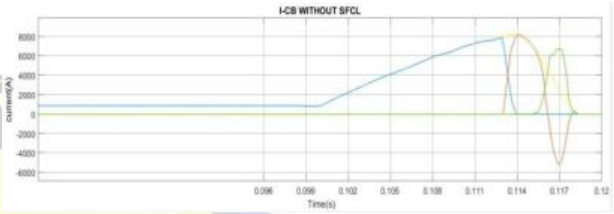
(b) With SFCL

Fig. 6. Interruption characteristics of PRCB when SFCL was applied

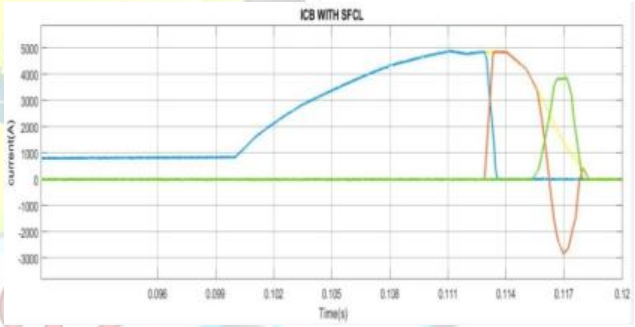
By connecting SFCL the maximum I_{total} was 5 kA, and 62.1% of the fault current was reduced. As the impedance of the main path increased via SFCL quenching, the time constant L/R of the test-bed declined, enabling the reduction of total oscillation time. Thus, fast interruption was achieved within 25 ms with less oscillation. If faster interruption time is required, increasing the quench resistance could be a solution and hence time constant of the secondary path reduced. Christo Ananth et al.[5] discussed about amplifier power relation, impedance , T π and microstripline matching networks.

Case 3: Inverse current injection CB (I-CB)

fig.7 current injection CB (I-CB) gives the interruption characteristics for DC fault. Without SFCL the maximum I_{total} was 8.2 kA, which is lower than the PRCB. No oscillation was observed in the I-CB, because pre-charged capacitor can discharge large inverse current over a short duration.



(a) Without SFCL



(b) With SFCL

Fig. 7. Interruption characteristics of the I-CB when SFCL was applied.

Observing the fig.7 fast I-CB interruption time measured at 18 ms, was achieved as compared to that of PRCB. In the case of with SFCL, the maximum I_{total} was 4.9 kA. Interruption time was equal in both the cases. There was no passive oscillation with the inverse current injection over a short duration. Therefore, L/R time constant on the secondary path did not influence on the interruption characteristics of the I-CB, unlike in PRCB.

Case 4: Hybrid DC CB (HDCCB)

The important thing with the HDCCB is it achieves fast interruption due to the response time of a semi-conductor. The maximum I_{total} found was 3.5 kA, and the interruption time was 7.8 ms, which is the lowest value depicted in Fig. 8. By applying SFCL, the maximum I_{total} = 2.9 kA, which is the lowest value with a 17.1 % reduction ratio and estimated interruption time of 7.6 ms. Due to the fast response of HDCCB, the circuit interruption has been progressed within the transition time of SFCL. Therefore, we can observe that the effect of SFCL on a HDCCB

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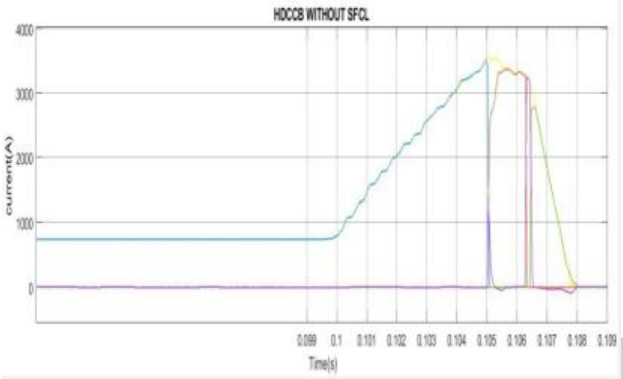
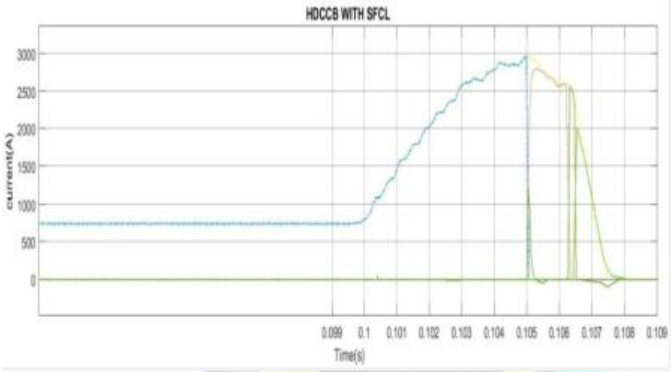
exhibits insufficient performance as compared to all types of circuit breakers.



(a) Without SFCL



(b) With SFCL

Fig. 8. Interruption characteristics of the HDCCB when SFCL was applied.

Analysis Of Energy Dissipation

Circuit breaker can be designed based on the maximum power dissipation across the circuit breaker contacts. Therefore, Energy dissipation is the primary design parameter used to determine the breaking capability of CB. Here we can calculate the didssipated energy across the SFCL and HVDC CBs. From (6), the measured current, voltage and total interruption time determine the dissipated energy across the HVDC CB:

$$E_{dissipated} = \int_{t.fault}^{t.interruption} Pdt = \int_{t.fault}^{t.interruption} V_{cb} I dt \quad (6)$$

where the Vcb is the voltage across HVDC CB during a fault interruption.

Fig.9 shows the dissipated energy across the CB for both with and without application of the SFCL. Without the SFCL, the highest energy dissipation was observed in the MCB due to interruption failure, and the lowest energy dissipation was observed in the HDCCB. By applying the SFCL, energy reduction was observed iin all types of HVDC CB. Among these, PRCB with SFCL showed the best performance with an 83.4 % energy reduction; however, the SFCL shows less effect on the HDCCB, which is considered the key concept among the various HVDC CBs.

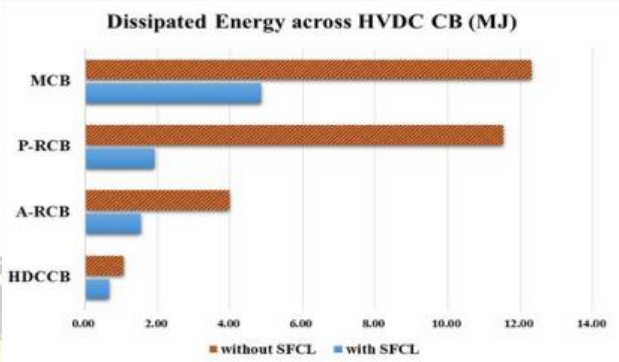


Fig. 9. Comparison of dissipated energy across the HVDC CB during a fault

To determine the optimum topology for HVDC CBs with SFCL, comparative analyses were conducted considering the interruption performance and cost, as shown in Table II. The best performance improvement was achieved via the PRCB. I-CB also have better improvement, but less than that of the PRCB.

The maintenance of I-CB is complicated due to the external power source needed to charge the auxiliary capacitor. The HDCCB, which showed the highest performance of all, has a disadvantage high cost. In addition, a few HDCCB performance improvements were observed if the SFCL was applied. Exclusive use of the HDCCB was the optimum solution to achieve DC current interruption through the HDCCB, considering cost effectiveness. PRCB, which is considered the least efficient HVDC CB concept, has shown the noticeable enhancement by applying SFCL considering the fault interruption capability and development cost.

Table II
Impact Of Resistive SFCL On Four Types Of HVDC CB

	MCB	PRCB	1-CB	HDCCB
Reduced	67.3	62.1	40	17.1
I total Reduced $\Delta t_{in}(ms)$	No interruption	30	0	0.2
Reduced $E_{fault}(\%)$	60.5	83.4	61.2	37.4
Required components	MCB(+SFCL)	MCB,LC,SA(+SFCL)	MCB, ACB(+SFCL)	IGBTs MCB, ACB,SA (+SFCL)

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CONCLUSION

This paper deals with the impact of SFCL on various types of HVDC CB. The resistive SFCL quenching characteristics and concepts of HVDC CB models including the black-box arc model, and a simple HVDC were designed. A severe DC pole-to-pole fault was imposed to analyze the interruption performance. If we increase the levels then the output waveform is more close to sinusoidal. Higher the number of the levels, more approximate is the waveform to sin wave. From the simulation results, the maximum fault current, interruption time, and dissipated energy stress on an HVDC CB could be decreased by applying an SFCL. Noticeable enhancement of the fault interruption capability was exhibited by PRCB, which showed the longest interruption time and highest maximum fault current without SFCL. When the SFCL was applied, the L/R time constant of the secondary path was decreased, and therefore fast interruption with less oscillation was observed. Consequently, SFCL installation with PRCB could be a viable, reliable, and cost-effective option to enhance DC fault current interruption.

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