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ANALYSIS OF HYBRID LOW POWER SDF-MDC FFT STRUCTURE

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Abstract: In wireless and digital communication system used orthogonal frequency division multiplexing (OFDM) for many reasons; these are reconfigurability, less hardware utilization, low power consumption and so on. OFDM is a multi carrier transmission system because it convert single data stream with higher data rate to multiple data streams with low data rate, which are orthogonal to each other. Different types of functions are present in both the transmitter and receiver of the OFDM system. Frequency transformation is the essential step of OFDM system. FFT can be classified as Radix-2, Radix-4, Mixed Radix, Split Radix etc. Based on the applications the classified FFT techniques are used. In the FFT architecture different feedback structures are widely used to convert time domain to frequency domain. The feedback structures are Single path Delay Feedback (SDF), Multipath Delay Feedback (MDF), Single path Delay Commutator (SDC) and Multipath Delay Commutator (MDC). These feedback structures are not applied at a same time, because each structure has different advantages and different drawbacks, based on the advantage the feedback structure is selected. In the VLSI system design, every feedback structure offers high speed of computation and every commutator structure offers less LUTs and slices utilization and low power consumption. If suppose a need both the advantages can combine the feedback and commutator structures. The combined architecture provides high speed, less area and low power utilization. Without the FFT/IFFT process cannotprocess the signal in the transmitter and the receiver.

Keywords- Fast Fourier Transform (FFT);Inverse Fast Fourier Transform (IFFT);Decimation in Time (DIT); Decimation In Frequency(DIF);.

I.INTRODUCTION

In a wireless communication OFDM is a key technique for high spectral efficiency and high data rate. Fast Fourier Transform (FFT) processing is one of the key processes in OFDM systems.Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) are the technique used to perform the transformation from time domain signal to frequency domain signal and frequency and vice versa. FFT processor present in the receiver of the system, likewise IFFT is present in the transmitter part. Discrete Fourier Transform (DFT) is a technique to get the frequency response of time domain signal. But it contains complexity during the frequency response analysis. So, most of case FFT is preferred for computation. Decimation in Time (DIT) and Decimation in Frequency (DIF) are the two types of FFT designs. DIT- FFT process follows the divide and conquers for computing the transformation of frequency. Likewise DIF-FFT processes follows the same divide and conquer approach for getting frequency signal from the

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time signal. Twiddle factor multiplication of both the DIT and DIF FFT can be performed after the subtraction of even and odd outputs [5]. Parallel FFT and Pipelined FFT are the types used in the system. Now a day's pipelined FFT is mostly used in the system for high speed communication. Adiono [1] proposed a 64-point Radix-4 FFT for OFDM applications. Twiddle factors values are not stored in ROM; instead of using ROM pipelined FFT can access the value directly. Radix-4 algorithm is better because it reduces the steps for reducing the butterfly structure. It is faster than radix-2 algorithm. To increases the point in the FFT structure has processes the large amount of data and provides a higher speed.

In general FFT algorithm can be developed in two ways, Decimation in Time (DIT-FFT) and Decimation in Frequency (DIF-FFT) are the methods developing the FFT algorithm. Both the methods have same complexity, and operations but only one different is the input and outputs are arranged differently. Sowjanya [2] proposed a radix-2, radix-8 and split radix algorithm. In radix-2 algorithm the computation is split into odd and even pairs. The number of stages is higher in this radix. Radix-8 FFT process is used to improve the speed of the computation. Split radix is combination of two or more radix. Split radix method provides better performance than radix-2 method like speed, LUTs and slices utilization. Split radix is preferred for High speed applications.

Yang has been proposed a new Multipath Delay Commutator (MDC) based FFT/IFFT processor for MIMO-OFDM system. In a traditional MDC structure occupy most of the area for storage. The proposed memory scheduling mechanism is to decrease the memory required for storing the twiddle factor values. The proposed architecture can use different butterfly structures at each stage. First stage is performed by radix-4 and the last stage is performed by radix-8 method, because the multiplier. MDC structures occupy less area utilization and consume low power than compared to the other feedback structures. The power saving is achieved by reduction in usage of memory element in the processor. [3] proposed a system which can achieve a higher throughput and higher energy efficiency. The S-BOX is designed by using Advanced Encryption Standard (AES). The AES is a symmetric key standard for encryption and decryption of blocks of data. In encryption, the AES accepts a plaintext input, which is limited to 128 bits, and a key that can be specified to be 128 bits to generate the Cipher text. In decryption, the cipher text is converted to original one. By using this AES technique the original text is highly secured and the information is not broken by the intruder. From that, the design of S-BOX is used to protect the message and also achieve a high throughput, high energy efficiency and occupy less area.

II. PROBLEM STATEMENT

In General the FFT is used to convert time signal to frequency signal. Normally the conversion is done in the butterfly structure based on the Radix algorithm. In the existing architecture normal Radix-2 FFT with simple SDF structure is used to perform the computations. The output response of the existing structure is not that much efficient, it generates some drawbacks along with the output. It occupies more number of LUTs and slices in the chip. It also takes high power to compute the FFT process. This problem can be identified in the existing architecture. This problem can be overcome by introducing a new architecture, named as mixed radix with combined SDF-SDC structure. Mixed radix reduces the computational steps during the time of operation. The pipelined FFT architectures can attain a high throughput and low latency which are appropriate for real-time applications. According to the dataflow scheme, the pipelined FFT architectures can be classified

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as a Single path delay feedback (SDF) and Single-path delay Commutator (SDC). The combination of two methods has some advantages. To improve the hardware efficiency, the SDF architecture is used to distribute the same delay elements between butterfly inputs and outputs, but the architecture operates at a low throughput due to the single path. The SDC architecture is used to send correct data sequence into butterfly elements by using switches (commutators). Both the combination of two structures has low latency, low power and less area utilization compared with the proposed concept. In some real-time applications such as OFDM or SDR, where high throughput is a requirement, it is important to be able to process the input samples in parallel.

III. HYBRID SDF-MDC FFT STRUCTURE

Single path Delay Feedback is a technique based on pipelined architecture. It shows in figure. 3. It provides high speed operation during the computation process. In the Radix-2 SDF architecture the input are applied serially. It is only suitable for high speed operation; it does not concentrate the area and power consumption of the processor. In the SDF structure delay elements are used to compute the feedback structure. The number of delay elements are depends on the FFT point of operation. SDF technique is more suitable for long distance communication system. Radix structure is not problem to implement the technique into the FFT; in any radix structure can easily apply the SDF structure. It consumes more power compared to the other type of structure.Clock gating technique is used to avoid the unnecessary switching activities. If one process is going on the remaining process is still disabled. This type of process is implemented in the communication systems can improve the system performance and efficiency of the data rate [5].

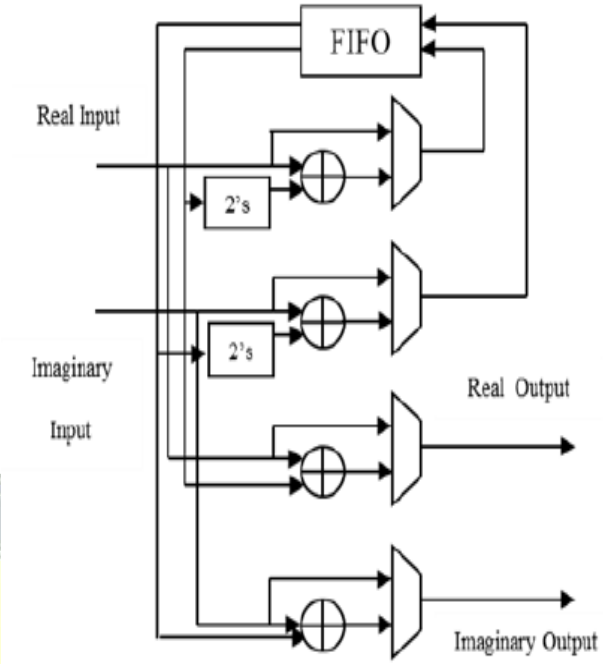

Fig-1 Block Diagram OfSDF-MDC

First stage consists of three Radix-2 butterfly units followed by twiddle factor multiplication units. Second stage has two butterfly units of Radix-4, one twiddle factor multiplication unit and two commutator units. Butterfly structure performs the signed addition and signed subtraction functions. Commutatordivision helps to modify the point of real and imaginary input data points for optimizing or reducing the hardware complexity of the circuit. The proposed mixed radix-2 and radix-4 pipeline FFT/IFFT architecture can process a continuous sequential flow of data. The proposed butterfly structures have the ability to read the both real and imaginary inputs and store both outputs in a single clockcycle.

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Table-1 Performance Evaluation of 16-point Mixed Radix-2, Radix-4 SDF-MDC FFT Structure

Parameters	Existing 16-Radix-2 SDF-MDC	Proposed 16-Radix-4 SDF-MDC
LUTs	10,542	10,317
Slices	5,863	5,732
Delay(ns)	14.625ns	14.188ns
Power(w)	7.438w	6.093w

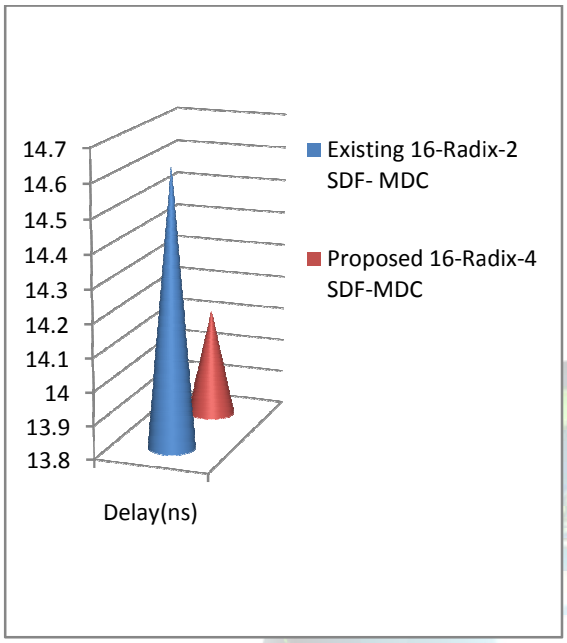

Fig. 2.Comparison graph of radix-2 and radix-4 SDF-MDC FFT

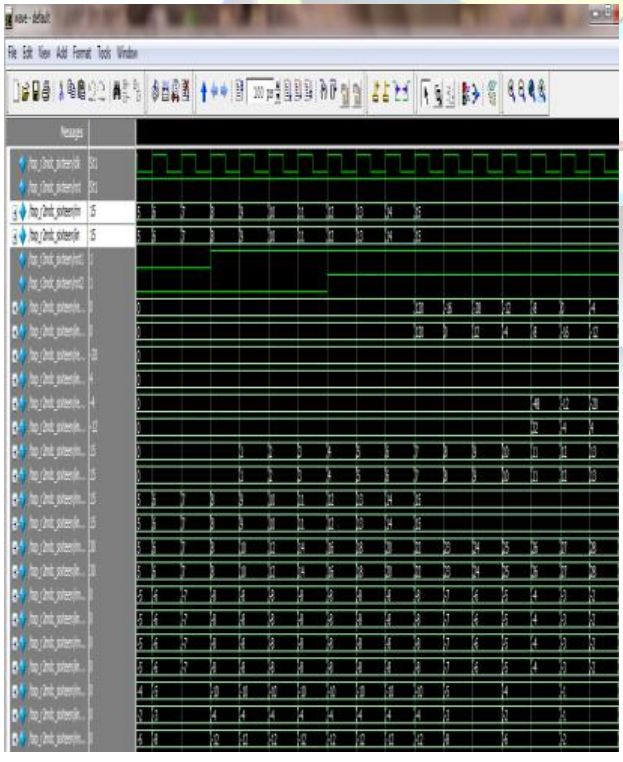

Fig.3. 16 Point Radix-4 SDF-MDC

V.CONCLUSION

In this paper discussed about the concept of 16-point pipelined mixed radix with combined SDF-MDC architecture. The main goal of the 16-point pipelined mixed architecture is to achieve a speed and low power during the computation of FFT processor. SDF structure was used to achieve a speed; likewise MDC offered the advantages like low power and less hardware utilization. The results were synthesized and evaluated by Xilinx.

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