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Monograph On Microwave Semiconductor Devices

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4.1 Microwave Bipolar Transistors (BJT)

→ The microwave bipolar transistors are planar in form and mostly Si–n–p–n operating upto 5 GH_Z.

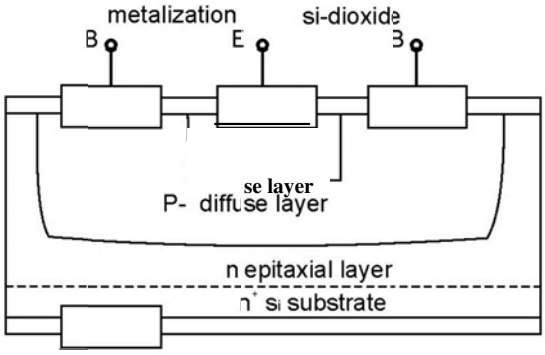


Fig. 4.1 : construction of Eipolar Transistor

→ Emitter width W is 1 micron, base thickness is 2 micron and emitter length is 25 micron.

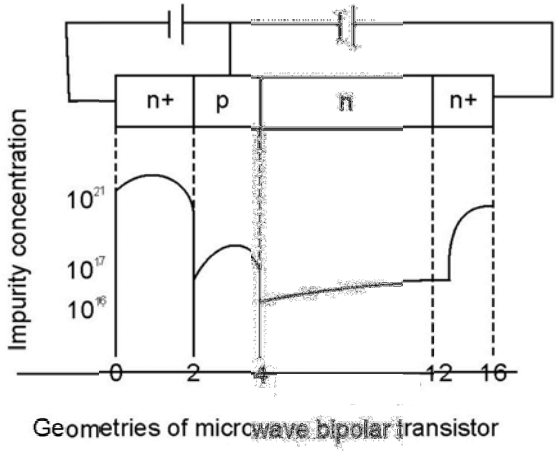


Fig. 4.2 : Distance Charge

→ For power amplification, class C-operation to minimize collector-base transit time.

→ In class 'C' both emitter-base & collector-base junctions are reverse biased so that no current flows in absence of a signal.

→ When an RF voltage of sufficient magnitude is applied to emitter-base junction for a fraction of RF cycle the junction is forward biased.

→ The electrons are injected to the base and injected carriers transit the base by a combined diffusion & drift flow processes. They are accelerated in the collector base depletion region.

Modes of operation

i) Normal (active) mode

→ Emitter junction is forward biased and collector is reverse biased.

→ In forward bias, the po itive polarity of the bias voltage is connected to the p side & negative polarity to the 'n' side for p-n junction.

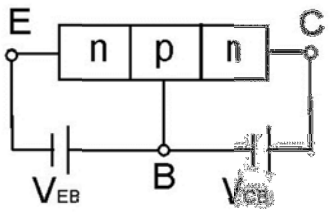


Fig. 4.3 : i) Normal (active) Mode

ii) Saturation region

→ Both transistors are forward biased with very low resistance & acts like a short circuit.

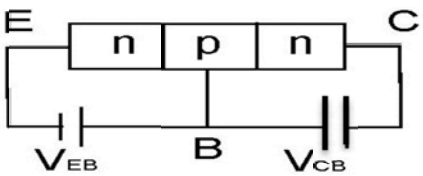


Fig. 4.4: ii) saturatrion region

iii) Cutoff mode

→ Both transistors are reverse biased as the current is cut off, transistor acts like an open circuit.

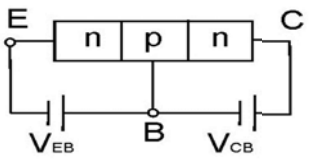


Fig. 4.5 : iii) cutoff mode :

iv) Inverse mode

→ Emitter Junction is reverse bias & collector junction is forward bias and its current gain is designated as the inverse α .

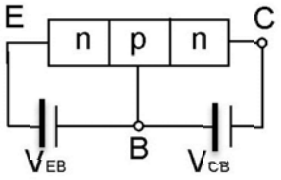


Fig. 4.6 : iv) Inverse mode

→ It is used as multi emitter transistor in the TTL logic gate.

Physical Struct re

→ All microwave transistors are now planar in form & almost all are of the silicon n-p-n type.

→ It can characterized i) inter digitated, ii) overlay, iii) Matrix

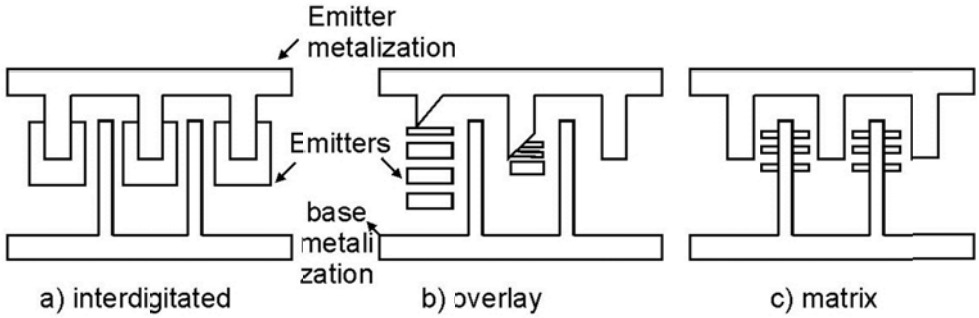


Fig. 4.7 : Surface geometries of microwave power transistor

Current flow in common base n-p-n Transistor:

→ The steady state diffusion equation for an n-p-n transistor at the low level injection is given by $I_n = Aq\, D_n \frac{dn_p}{dx}$ ------ (1)

A → Cross area, Dn → electron diffusion constant, x → distance measured from the base region.

n_p → Minority electron carrier density in p-type base layer.

The electron current which is injected from the emitter into base at x = 0 for $L_n >> W$ is given by

$$I_{nE} = \frac{-AqD}{N_a W} n_i^2 e^{V_E/V_T} \quad \text{------ (2)}$$

$L_n \rightarrow$ electron diffusion length, m $\rightarrow$ minority carrier density.

$W \rightarrow$ Base width. $V_E \rightarrow$ forward biased voltage across the emitter junction.

$V_T \rightarrow 26 \times 10^{-3}$ V at 300^0 K is the voltage equivalent of temperature.

$\rightarrow$ The electron current which the oscillator at x = W is

$$I_{nE} = \frac{-AqDn n_i^2}{N_a W} e^{V_E/V_T} \quad \text{------ (3)}$$

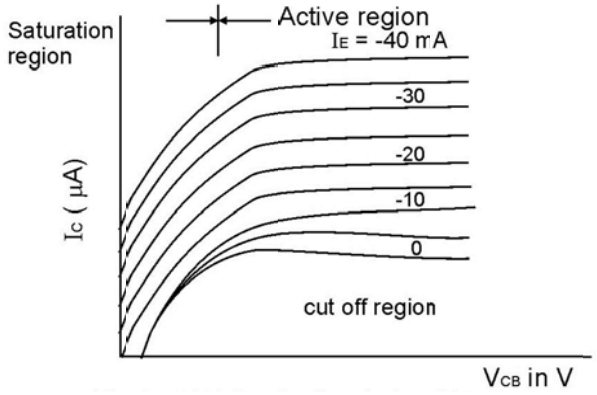
Na $\rightarrow$ acceptor energy in base region.

The current in the base terminal is

$$I_B = I_{\rho E} - (I_{nE} - I_{nC}) + I_{c0} \quad \text{----- (4)}$$

$I_{c0} \rightarrow$ collector junction reverse saturation current with zero emitter current.

V-I Characteristics



i) Active region

$\rightarrow$ Emitter junction is forward biased & collector junction is reverse biased. Ic is independent of collector voltage is depends only on I_E.

$\rightarrow$ When the I_E is zero, the collector current is equal to the reverse saturation current I_{C0}.

ii) Saturation Region

→ Both the emitter and collector junctions are forward biased.

→ The electron current flows from the n side across the collector junction to the p-type base.

iii) Cut off region

→ Both the emitter & collector junctions are reverse biased.

Power Frequency limitations Of BJT

The power frequency limitation is due to

i) Maximum velocity of charge carriers in a semiconductor. This is the saturated drift velocity Vs.
ii) Maximum Electric field Em that can be sustained in a semiconductor.
iii) The maximum current of a microwave power transistor.

First equation: Voltage frequency limitation

$$V_m f_T = \frac{E_m V_s}{2u} = \begin{cases} 2 \times 10^{11} \text{ V/s for silicon} \\ 1 \times 10^{11} \text{ V/s for germanium} \end{cases}$$

Where $f_T = \frac{1}{2u\,T}$ is the charge carrier transit time cut of frequency.

$T = \frac{L}{V}$ is the average time for a charge carrier moving at an average velocity 'V' to transverse the emitter – collector distance L.

$V_m \rightarrow E_m L_{min}$ is the maximum allowable applied voltage.

$V_S \rightarrow$ Maximum possible saturated drift velocity.

$E_m \rightarrow$ Maximum electric field.

Second equation: Current – frequency limitation

$$(I_m X_C) f_T = \frac{E_m V_s}{2u}$$

Where I_m – maximum current of the device.

$$X_C = \frac{1}{m_T C_0} = \frac{1}{2u f_T C_0}$$ is the reactive impedance.

Co = Collector base capacitance.

Third equation : Power – frequency limitation

$$(P_m X_C)^{1/2} f_T = \frac{E_m V_s}{2u}$$

The power capacity of a device must be decreased as the device, the cut-off frequency is increased.

Fourth equation: Power gain – frequency limitation

$$(G_m V_{th} V_m)^{1/2} f_T = \frac{E_m V_s}{2u}$$

Where $G_m \rightarrow$ maximum available power Gain.

$V_{th} = \frac{KT}{e}$ is the thermal voltage.

K → Boltzman's constant 1.38×10^{-23} J/^{0}K

T → Absolute temperature in degree.

e → electron charge (1.60×10^{-19} C)

The maximum available power gain of a transistor

$$G_m = \left(\frac{f_T}{f}\right)^2 \frac{Z_{out}}{Z_{in}}$$

Where Zout and Zin are the output and input impedance respectively.

→ If the electrode series resistances are assumed to be zero. The ratio of the output impedance to the input impedance can be written.

$$\frac{Z_{out}}{Z_{in}} = \frac{€_{in}}{€_{out}}$$

Where C_{in} and C_{out} are the input and output capacitors.

→ The input capacitance C_{in} and emitter diffusion capacitance C_d are related by

$$C_{in} = C_d = \frac{I_m r}{V_{th}}, \quad C_{out} = \frac{I_m r}{V_m}$$

→ Typical power gains of microwave transistor lie in the 6 to 10 dB range.

4.2 Microwave FET

→ In conventional transistor both the majority and minority carriers are involved. This type of transistors referred to as a bipolar transistor.

→ In FET, the current flow is carried by majority carriers either electrons or holes only this type is referred as a unipolar transistor.

→ It has two important characteristics that make them superior to bipolar transistors to microwave amplifiers. These are lower noise characteristics and high frequency of operation.

JFET

→ The n-type material is sandwiched between t o highly doped layers of n-type material that is designated as 'p^+'. This type of devices is called as n-channel FET.

→ In the middle part is a p-type semiconductor the device is called p-channel JFET. The direction of drain current I_d is flowing from the drain to the device.

→ For 'p' channel JFET, the polarities of two biasing voltages Vg and Vd are interchanged.

→ The n channel JFET provides higher conductivity and higher speed.

Principle of operation

→ When the gate voltage Vg is zero the I_d is also zero under normal operating conditions. The channel between the gate junctions is entirely open.

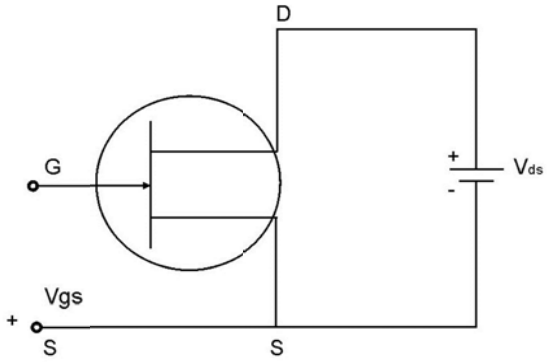


Fig. 4.9 : Circuit symbol

→ When a small drain voltage V_d is applied between the drain & source, the n-type semiconductor bar acts a simple resistors. I_d increase linearly with V_d.

→ If a reverse gate voltage V_d is applied across t e p-n gate junctions the majority of the free electrons are depleted from the channel and space charge regions are extended into the chan el.

Pinch off

As the drain voltage V_d is increases, the space charge regions expand & join together, so that all the free electrons are completely depleted in the joined region. This condition is called pinch off.

Pinch off voltage V_p

$$V_p = \frac{qN_d a^2}{2\varepsilon_s} \text{ Volts.}$$

n → Height of channel in meters

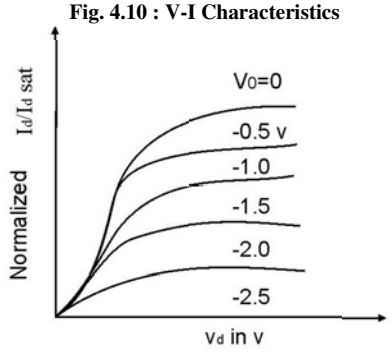
N_d → electron concentration in electrons per cubic meter

ε_s → permittivity of the material

$\varepsilon_0 \rightarrow 8.854 \times 10^{-12}$ F/m

V-I Characteristics

Fig. 4.10 : V-I Characteristics



Pinch off current

$$I_0 = \frac{\mu_0 q^2 Nd^2 Z \frac{3}{a}}{L \varepsilon_s}$$

μ_0 → electron mobility, Z → distance in z-direction.

L → length in x direction, W → depletion layer width.

a → width between two p-n junctions, q → charge in coulumb.

Pinch off region

→ When an electric field appears along the x axis between the drain & the source.

→ As the drain voltage V_d & I_d are further increased, the channel is finally pinched off.

Break down voltage

→ As the drain voltage V_d increases for a constant gate voltage V_g, the bias – voltage causes avalanche breakdown across the gate junction & the drain current I_d increases sharply

$V_b = V_d + |V_g|$

4.3 Microwave Tunnel diode

→ Tunnel diode are heavily doped p-n junction diode that have a negative resistance over a portion of V-I characteristics.

Operation

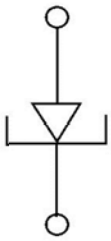


Fig. 4.11 : Sym ol

→ These diodes are used as a microwave amplifier or oscillators. Due to heavy doping the width of the depletion region becomes very thin and an overlap occurs between the conduction band on the n side and valence band level on the p-side.

→ When reverse bias is applied to the tunnel diode, the n side energy levels shift downward with respect to the p-side.

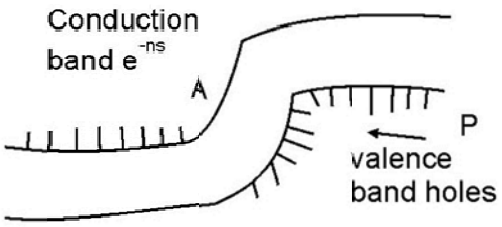
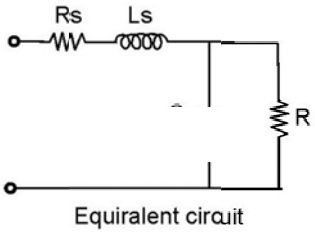


Fig. .12 : Energy Ba d diagram

→ As a result the electrons will tunnel from the p-side or the n-side giving rise in a reverse diode current. If we increase reverse bias, the reverse current also increases.

→ Under this condition, the current through the tunnel diode reaches a maximum value (V_p).

→ If the forward bias is further increased, the tunnelling current decreases and at some forward voltage the tunnelling current drops to zero.



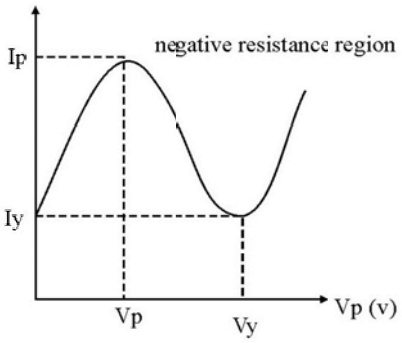


Fig. 4.13 : V-I characerstics

→ The current increases with increasing forward bias and reaches a some peak value I_P at a forward voltage V_p. If the applied voltage V is increased, beyond V_p current decreases and reach a minimum value.

→ The tunnel exhibits negative resistance characteristics between peak current & valley current (V increases, I decreases). For the forward bias voltage above valley voltage the tunnel diode behaves like an ordinary diode.

4.4 Varactor Diode

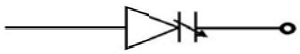


Fig. 4.14 : Symbol

→ Varactor diodes are p-n junction diode which provides a voltage variable junction capacitance in microwave circuits when reverse biased.

Operation

→ When a reverse bias is applied to a p_n junction the holes in the p-region move away from the junction and are attr cted to the positive terminal and electrons in the n-region move away from the junction and attracted to the negative terminal.

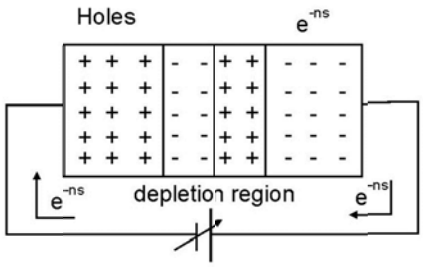


Fig. 4.15 : Pn junction

→ The flow of holes & electrons away from the junction increase depletion layer. The depletion layer is a region with no current carrier & a ts as insulator.

→ The depletion layer can be controlled using reverse bias voltage. The p & n regions act like plates of a capacitor & depletion region act a insulator.

→ The junction capacitance of the varacator diode is given as

$$C_j = C_0 \left(1 + \frac{v_R}{V_B} \right)^{-n} \qquad \text{--- (1)}$$

C_o → junction capacitance for zero bias.

V_R → Magnitude of reverse bias voltage below break down.

V_B → Barrier potential, n → constant whose values are 0.5 & 0.33 for abrupt linear graded p-n junction.

In this diode magnitude of reverse bias voltage is increased. The depletion layer width W_d will increase & the junction capacitance C_j will decreased.

$$C_j \alpha \frac{1}{W_d} \quad \text{----- (2)}$$

Equivalent Circuit

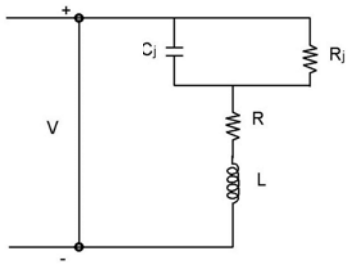


Fig. 4.16 : Equivalent circuit

$R_j \rightarrow$ Junction reverse resistance

R → Diode bulk resistance.

C-V characteristics

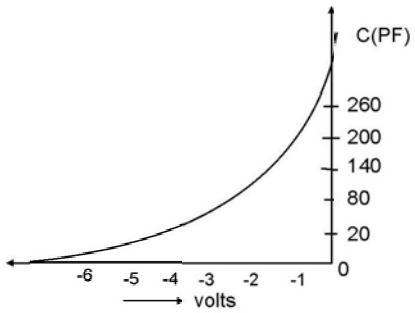


Fig. 4.17 : C-V Characterstics

The junction capacitance will decrease as the voltage across in junction increases.

4.5 Step Recovery Diode

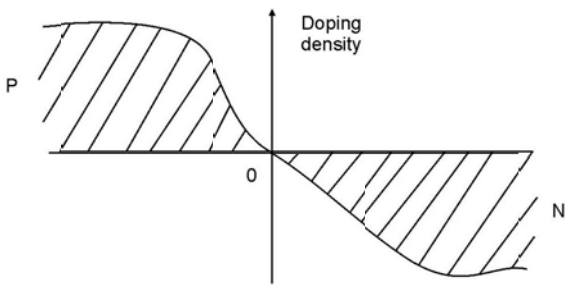


Fig. 4.18: doping profile of step recover/ diode

→ A step recovery diode also know as snap-off varactor is a silicon (or) gallium arsenide pn junction diode with a construction similar to that of varactor diode. It is an epitaxial diffused junction diode having a graded doping profile, where doping density decreases near the junction as

shown in figure designed to store charge, when it conducting under forward Bias.

→ At low frequencies, it works as an ordinary diode, conducting in the forward direction but not in the reverse direction, that is it recovers immediately from the ON state to the OFF state. However when a high frequency signal is applied to the diode does not recover immediately. Even during the negative half cycle of the input signal, it keeps conducting for a while, after which the reverse current ceases abruptly in one step.

→ This reverse conduction for a brief period is due to the fact that charges stored in the depletion region, under forward bias condition take time to drain away from the junction. Hence the diode very briefly discharges this stored energy in the form of a sharp pulse under reverse bias condition as shown in fig. 4.19. The step (or) sudden recovery from reverse current ON to reverse current OFF gives the diode its name.

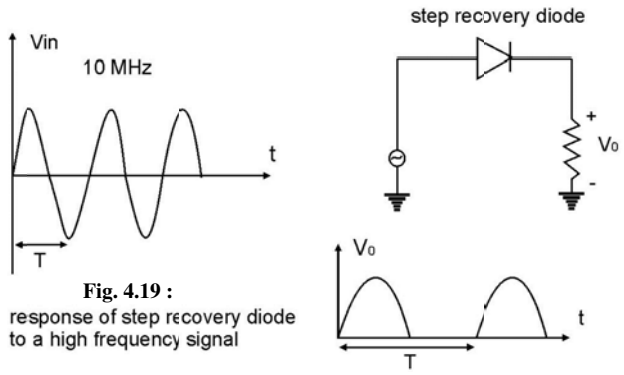


Fig. 4.19 :
response of step recovery diode to a high frequency signal

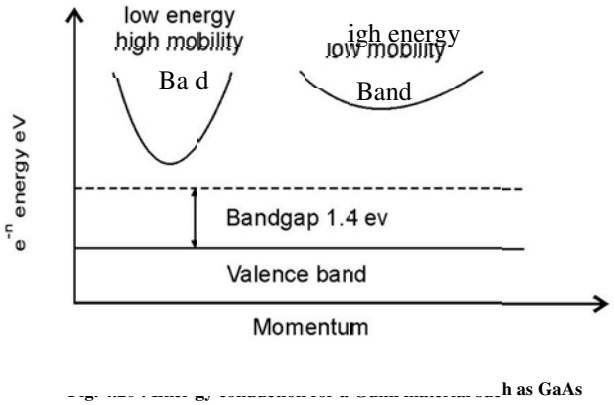
→ The sharp pulse in the reverse direction is very rich in harmonics. The duration of this pulse is 100 to 1000 ps. A tuned circuit connected at the output operated at the wanted harmonic will give a frequency multiplication depending upon the harmonic, that is selected.

Transferred Electron Devices (TEDs)

→ TED (or) Gunn diodes make use of two terminal devices based on the phenomenon known as transferred electron effect.

→ Some materials like GaAs exhibit a negative differential mobility, when biased above a threshold value of the electric field. Christo Ananth et al.[1] discussed about E-plane and H-plane patterns which forms the basis of Microwave Engineering principles.

Transferred electron effect:

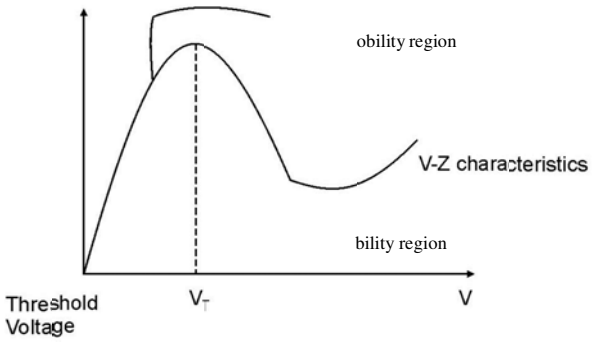


h as GaAs

→ The electrons in the lower energy band will be transferred into the higher-energy band. The behaviour is called transferred electron effect (TED) or Gunn diode and the device is called TED (or) Gunn diode.

→ In the high energy band the effective electron mass is larger & hence the electron mobility is lower than low energy band.

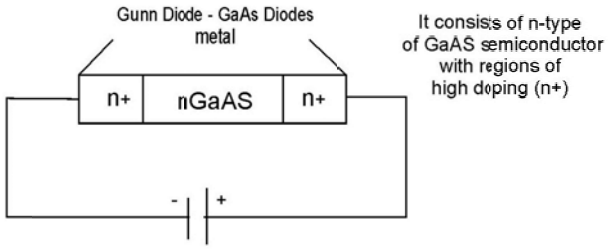
→ The conductivity is directly proportional to the mobility, the conductivity & hence the current decreases with an increase in electric field strength. Gunn diodes are negative resistance devices which are normally used as low power oscillator at microwave frequencies in transmitter & also as local oscillator in receiver.



→ The positive resistance absorb power (passive devices) whereas negative resistance generate power (active devices)

Fig. 4.21 : V-I Characteristics

Gunn Diode – GaAs diode



→ It consists of n-type GaAs semiconductor with regions of igh doping (n^+).

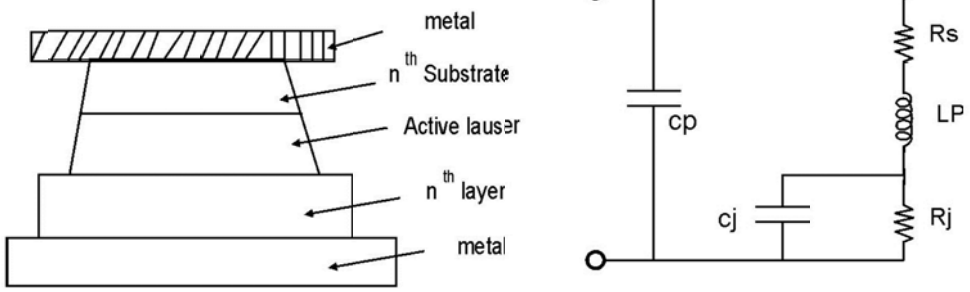
Fig. 4.22 : Simple Gunn Oscillator

→ There is no junction, this is called diode with reference to the positive end (anode) & negative end (Cathode) of the DC voltage applied across the device.

→ If a dc (or) diode voltage or an electric field at low level is applied to the GaAs an electric field is established across it. Initially the current will increase with a rise in the voltage.

→ At low Electric field in the material most of the electrons will be located in the lower energy band.

Fig. 4.23 : Construction of Gunn diode

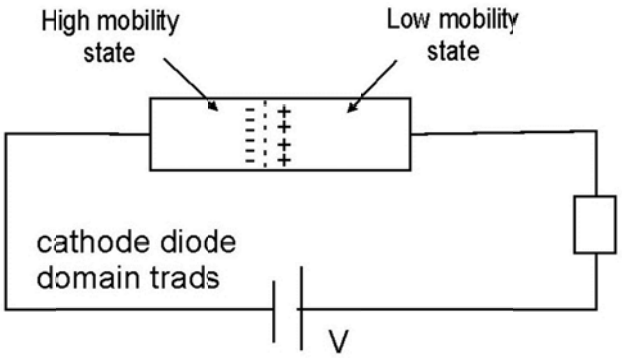


→ When the diode voltage exceeds a certain threshold value, V_{th} a high electric field is produced across the active regions and electrons are excited from their initial lower valley to the higher valley.

C_j → diode capacitance, - R_j → diode resistance

R_S → Total resistance of loads ohmic contact bulk resistance of diode

I_P → Package Inductance & C_P → Package capacitance.



→ Ga As is a poor conductor, considerable heat generated in the diode. The diode should be well banded into a heat sink. The negative resistance has a value that typically lies in the range -5 to -20 ohm.

Fig. 4. 24 : GaAs Gunn diode

Ridley – Watkins – Hilsum (RWH) Theory

1. Differential negative resistance

RWH theory is the differential negative resistance developed in a bulk solid state III-V compound. When either a voltage or a current is applied to the terminals of sample.

→ Two modes are available in the negative resistance devices.

i) Voltage controlled mode & ii) current controlled mode

i) Voltage controlled Mode:

→ The curren density can be multiva ued.

→ High field domains are formed, separating two low field regions.

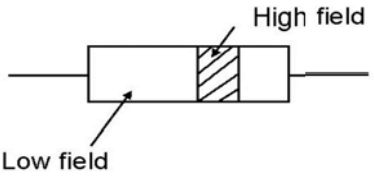


Fig. 4. 25 : High field domain

ii) Current controlled mode:

→ The voltage value can be multivalued.

→ The mode splitting the sample results in high current filaments running along the field direction.

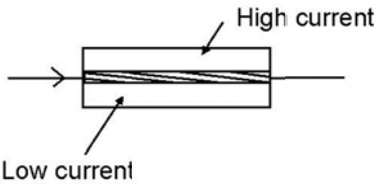


Fig. 4.26 : High current filament

The negative resistance of a sample at a particular region is

$$\text{Negative resistance} = \frac{dI}{dv} = \frac{dJ}{dE} \qquad \text{----- (1)}$$

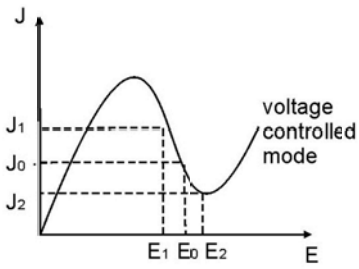
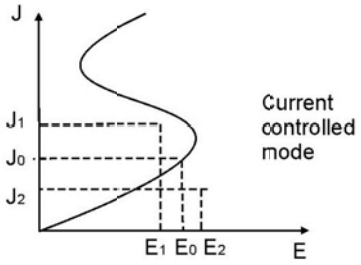


Fig. 4.27 (a) : Voltage – controlled mode



b) Current controlled mode

Explanation

→ If an electric field E_0 is applied to the sample, the current density J_0 is generated. As the applied field is increased to E_2, the current density is decreased to J_2. When the field is decreased to E_1, the current density is increased to J_1.

Two Valley Modal theory

→ According to the energy band theory of the n-type GaAs a high mobility lower valley is separated by energy of 0.36 eV from a low mobility upper valley.

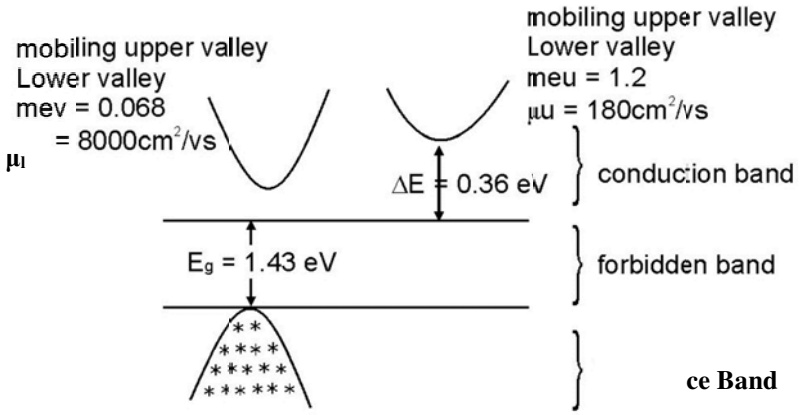


Fig. 4.28 : Two valley model for n-type GaAs

Transfer of electron densities

→ Electron ensities in the lower & upper valley remain the same under an equilibrium condition.

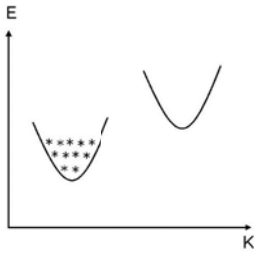
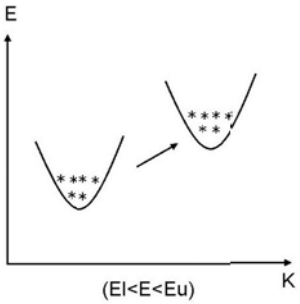


Fig. 4.29 : E < E_L

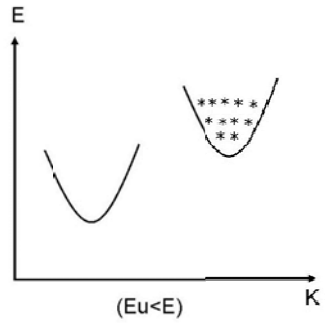
i) When the applied electric field is lower than the electric field of the lower valley ($E < E_l$), no el ctrons will transfer to the upper valley $E < E_l$.

ii)

→ When the applied field is higher than that of the lower valley & lower than that of the upper valley. ($E_l < E < E_u$) electrons will begin to transfer to the upper valley.



iii)



→ When the applied electric field is higher than that of the upper valley ($E_U < E$) all electrons will transfer to the upper valley.

→ If electron densities in the lower & upper valleys are n_l and n_u, the conductivity of the n-type GaAs is given by

$$\sigma = e(\mu_l n_l + \mu_u n_u) \qquad \text{----- (2)}$$

e → electron charge, μ → electron mobility, n → $n_l + n_u$ is electron density.

→ The electron density n & mobility μ are both function of electric field E. diff. w. r. to E

$$\frac{do}{dt} = e\left(\mu_l \frac{dn_l}{dE} + n_u \frac{dn_u}{dE}\right) + e\left(n_l \frac{d\mu_l}{dE} + n_u \frac{d\mu_u}{dE}\right) \qquad \text{------ (3)}$$

If the total electron density. $n = n_l + n_u$ ----- (4)

It is assumed that μ_l & μ_u are proportional to E^p where p is constant, then

$$\frac{d(n_l + n_u)}{dE} - \frac{d_n}{dE} = 0 \qquad \text{----- (5)}$$

$$\frac{dn_l}{dE} = \frac{-dn_u}{dE} \qquad \text{----- (6)}$$

$$\frac{d\mu}{dE} \sim \frac{dE^P}{dE} = PE^{P-1} = \frac{PE^P}{E} \propto \frac{P\mu}{E} = \frac{P\mu}{E} \qquad \text{----- (7)}$$

Substitute equation (5) to (7) into equation (3)

$$\frac{dn_u}{dE} = \frac{-dn_l}{dE} \quad , \quad \frac{d\mu}{dE} = \frac{P\mu}{E}$$

$$\frac{d\mu_l}{dE} = \frac{\mu_l . P}{E} \quad \text{------ (8)}$$

$$\frac{do}{dE} = e\left(\mu_l \frac{dn_l}{dE} + \mu_u \frac{dn_u}{dE}\right) + e\left(n_l \frac{d\mu_l}{dE} + n_u \frac{d\mu_u}{dE}\right) \quad \text{----- (8a)}$$

Substitute equation (6) & (8) in equation 8(a), we get

$$= e\mu_l \frac{dn_l}{dE} - e\mu_u \frac{dn_l}{dE} + en_l \mu_l \frac{P}{E} + en_u \mu_u \frac{P}{E}$$

$$= e(\mu_l - \mu_u) \frac{dn_l}{dE} + e(n_l - \mu_l + n_u \mu_u) \frac{P}{E} \quad \text{----- (9)}$$

Ohm's law $J = \sigma E$ ---- (10)

$$\frac{dJ}{dE} = \sigma + E \frac{d\sigma}{dE} \quad \text{------ (11)}$$

Equation (11) can be written

$$\frac{\frac{dJ}{dE}}{o} = 1 + \frac{E}{o} \frac{d\sigma}{dt}$$

$$\frac{1}{o} \frac{dJ}{dE} = 1 + \frac{\frac{do}{dE}}{\frac{o}{E}} \quad \text{----- (12)}$$

For negative resistance, the current density J must be decrease with increasing field E (or) the ratio of $\frac{dJ}{dE}$ must be negative.

The condition for negative resistance is given by

$$\frac{\frac{do}{dE}}{\frac{o}{E}} > 1 \quad \text{----- (13)}$$

From equation (9)

$$\frac{\frac{do}{dE}}{\frac{o}{E}} = \frac{e(\mu_l - \mu_u) \frac{dn_l}{dE}}{\frac{o}{E}} + \frac{e(\mu_l n_l + n_u \mu_u) \frac{P}{E}}{\frac{o}{E}}$$

$$= \frac{Ee}{o}(\mu_l - \mu_u) \frac{dn_l}{dE} + \frac{EeP}{\sigma E}(\mu_l n_l + n_u \mu_u) \quad \text{----- (14)}$$

Substitute equation (2) in equation (14)

$$= \frac{Ee}{o}\left[\frac{\mu_l - \mu_u}{\mu_l n_l + \mu_u n_u}\right]\frac{dn_l}{dE} \perp \frac{eP}{e}\left[\frac{n_l \mu_l + n_u \mu_u}{n_l \mu_l + n_u \mu_u}\right]$$

$$= E\frac{dn_l}{dE}\left[\frac{\mu_l - \mu_u}{\mu_l n_l + \mu_u n_u}\right] + P \qquad \text{----- (15)}$$

Substitute $f = \frac{n_u}{n_l}$ in eqn (15)

$$= E\frac{dn_l}{dE}\left[\frac{\mu_l - \mu_u}{\mu_l n_l + \mu_u n_u}\right] + P$$

$$\frac{\frac{do}{dE}}{\frac{o}{E}} = E\frac{dn_l}{dE} \cdot\cdot \frac{1}{n_l}\left[\frac{\mu_l - \mu_u}{\mu_l + \mu_u f}\right] + P \qquad \text{----- (16)}$$

Substitute equation (16) in (13)

$$\frac{\frac{-dE}{dE}}{\frac{o}{E}} > 1 \quad \& \left[\left(\frac{\mu_l - \mu_u}{\mu + \mu_u f}\right)\left(\frac{E}{n1}\frac{dn_l}{dE}\right) - P\right] > 1 \qquad \text{----- (17)}$$

→ The separation energy between the bottom of the lower valley and bottom of the upper valley must be several times larger than the thermal energy at room temperature. This means that $\Delta E > KT$ or $\Delta E > 0.026$ eV.

→ The separation energy between the valleys must be smaller than the gap energy between the conduction & valence bands. This means that $\Delta E < Eg$. Otherwise the semiconductor will break down & become highly conductive.

→ Electrons in the lower valley must have high mobility, small effective mass & a low density of state.

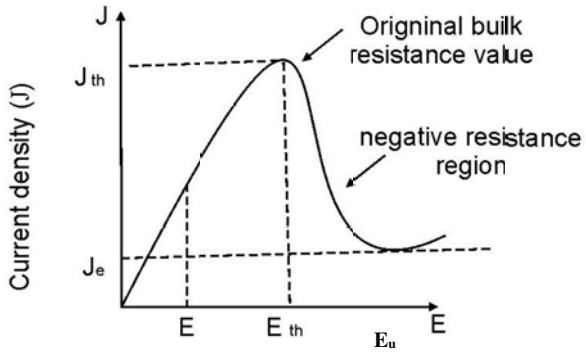


Fig. 4.30 : Current versus field characteristic of a tw valley semiconductor

→ Where as those in the upper valley must have low mobility, large effective mass & a high density of state.

→ From electric field theory the magnitude of the current density in a semiconductor is given by

$J = q\,nv$ ------ (18)

q → Electric charge, n → electron density, V → average electron velocity

differentiation of equation (18) with respect to electric field E.

$$\frac{dJ}{dE} = qn \frac{dV}{dE} \qquad \text{------ (19)}$$

The condition for negative differential conductance

$$\frac{dV_d}{dE} = \mu_0 < 0 \qquad \text{----- (20)}$$

μ_0 → negative mobility.

Modes of operation

i) Gunn oscillation mode

→ This mode is defined in the region when the product of frequency multiplied by length is about 10^7 cm/s and the product of doping multiplied by length is greater tha 10^{12} cm^2.

→ When the voltage applied across n^+ n. n^+ GaAs crystal exceeds a threshold level, elect ons are transferred from low energy to higher energy band.

→ These heavier electrons bunch together to form a electric field dipole domain near the cathode.

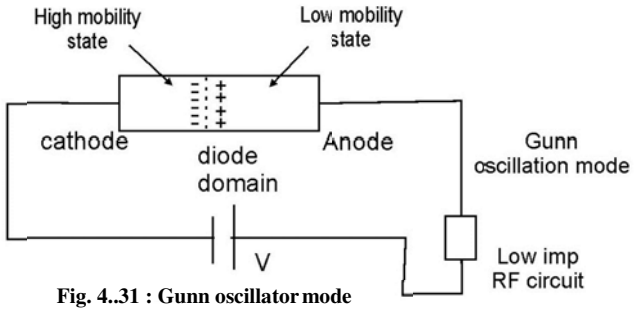


Fig. 4..31 : Gunn oscillator mode

→ The applied voltage remain constant, the electric field across the domain is greater than the average electric field. The consequent electric field remains below the threshold level across rest of the crystal. This prevents the formation of further domains.

ii) Stable amplification mode

It is defined in the region where the product of frequency times length is about 10^7 cm/s and the product of doping time length is between 10^{11} & 10^{12}/cm^3.

iii) LSA oscillation mode

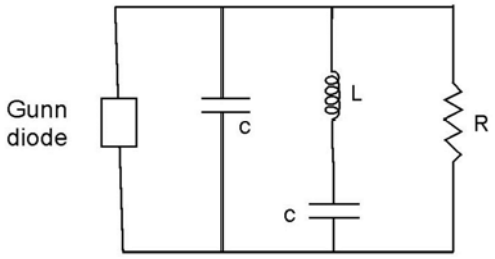


Fig. 4.32 : Gunn o cillator operating in LSA mode

→ It is defined in the region, where the product of frequency time length is above 10^7 cm/s and the quotient of doping divided b frequency is between 2 x 10^4 & 2 x 10^5.

iv) Bias-circuit oscillation mode

This mode occurs only when there is either Gunn (or) LSA oscillation and it usually at the region where the product of frequency time length is too small.

Criterion for classifying the modes of operation

→ The Gunn effect diodes are basically mode from an n-type GaAs with the concentration of free electrons ran ing from 10^{14} to 10^{17} per cubic centimeter at room temperature.

→ Its typical dimensions are 150 x 150 μm in cross section & 30μm long.

→ During the early stages of space-charge accumulation the time rate of growth of space charge layers.

$$Q(X, t) = Q(X - Vt, O) \exp\left(\frac{t}{\tau_d}\right) \qquad \text{------ (1)}$$

Where,

$\tau_d = \frac{s}{\sigma} = \frac{s}{en_O|\mu_n|}$ is the magnitude of negative dielectric relaxation time.

$\varepsilon \rightarrow$ semiconductor dielectric permittivity, $n_o \rightarrow$ doping concentration

$\mu_0 \rightarrow$ negative mobility, e → electron charge, $\sigma \rightarrow$ conductivity.

The layer start at the cathode at t = 0, X= 0

and arrive at the anode at $E = \frac{L}{V}$ & X = L

→ The factor of maximum growth the entire transit time of the space charge layer is given by

$$\text{Growth factor} = \frac{Q\left(L, \frac{L}{V}\right)}{Q(0,0)} = \exp\left[\frac{L}{V r_d}\right]$$

$$= \exp\left[\frac{L n_0 e |\mu_n|}{s V}\right] \quad \text{------ (2)}$$

For a large space – charge growth this factor must be larger than unity

$$n_o L > \frac{s V}{e |\mu_n|} \quad \text{----- (3)}$$

Gunn oscillation Modes

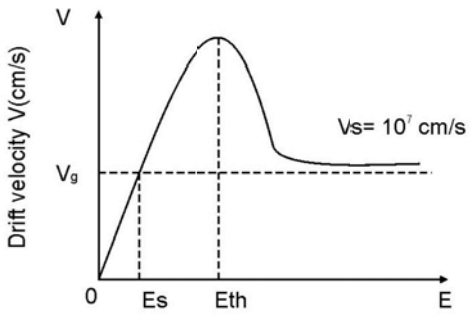
→ Most Gunn – effect diodes have the product of doping & length (n_0L) greater than $10^{12}/cm^2$.

→ When the product of n L is greater than $10^{12}/cm^2$ in GaAs, the space-charge perturbations in the specimen increase exponentially in space & time.

→ The frequency of oscillation $f = \frac{Vdom}{L_{eft}}$

Vdom → dominant velocity

L_{eff} → effective length.



→ The normal Gunn domain mode is operated with the electric field greater than the threshold region ($E > E_{th}$)

→ There are three possible domain model for the x.

Fig. 4.33 : Electron drift velocity versus electric field

- **Transit – time domain mode ($f_l = 10^7$ cm/s)**

→ When the electron drift velocity Vo is equal to the sustaining velocity V is the high-field domain is stable.

→ The electron drift velocity is $V_d = V_s = f_L \simeq 10^7$ cm/s. The oscillation period is equal to transit time $\tau_0 = \tau_1$. The time taken by the dipole domain to travel from cathode to anode is the transit time of the device.

→ The efficiency is below 10% because the current is controlled only when the domain arrives at the anode.

- **Delayed domain mode [10^6 cm/s < f_l < 10^7 cm/s]**

→ The oscillation field is greater than the transit time. This delayed mode is called inhibited mode. The ŋ is 20%.

- **Quenched mode [$f_l > 2 \times 10^7$ cm/s]**

→ In this mode, if the bias field drops below the sustaining field E_s during the negative half cycle, the domain collapsed before it reaches the anode.

- **Limited space charge Accumulation (LSA) mode [$f_l > 2 \times 10^7$ cm/s]**

→ The internal electric field would be uniform & proportional to the applied voltage. The current in the devices is then proportional to the drift velocity at this field. At low frequency limit the drift velocity.

$$V_l = f_l = 5 \times 10^6 \text{ cm/s} \qquad \text{----- (6)}$$

$$\text{Ratio of } n_0L \text{ to } fL = \frac{no}{f} = 2 \times 10^5 \qquad \text{----- (7)}$$

At the upper frequency limit the drift velocity.

$$Vu = f_l = 5 \times 10^7 \text{ cm/s} \qquad \text{----- (8)}$$

$$\text{Ratio of } n_0L \text{ to } f_l, \frac{no}{f} = 2 \times 10^4 \qquad \text{----- (9)}$$

- **Stable Amplification mode ($n_0L < 10^{12}/ cm^2$)**

→ When the n_0L of the device is less than about $10^{12}/cm^2$ the device exhibits amplification at the transit time frequency rather than spontaneous oscillation. Christo Ananth et al. [2] discussed about Improved Particle Swarm Optimization. The fuzzy filter based on particle swarm optimization is used to remove the high density image impulse noise, which occur during the transmission, data acquisition and processing. The proposed system has a fuzzy filter which has the parallel fuzzy inference mechanism, fuzzy mean process, and a fuzzy composition process.

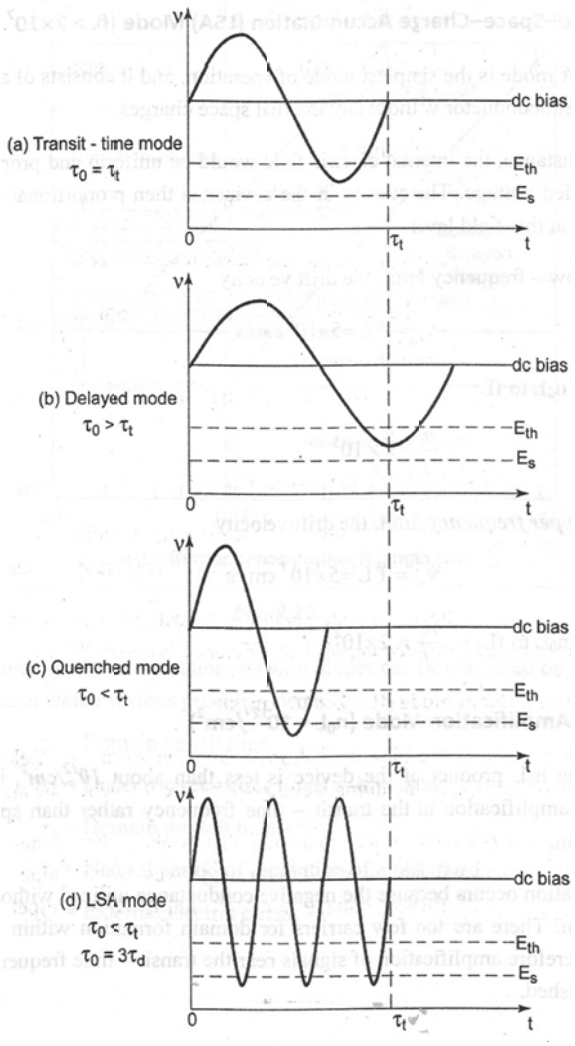


Fig. 4.34 : Gunn domain modes

Avalanche Transit Time Devices

→ They are p-n junction diode with the highly doped p and n regions. They could produce negative resistance in microwave frequencies by using a carrier impact ionization avalanche breakdown & carriers drift in the high field intensity region under reverse biased condition.

→ There are three distinct modes of avalanche oscillators.

i) IMPATT, ii) TRAPATT & iii) BARITT

Read Diode

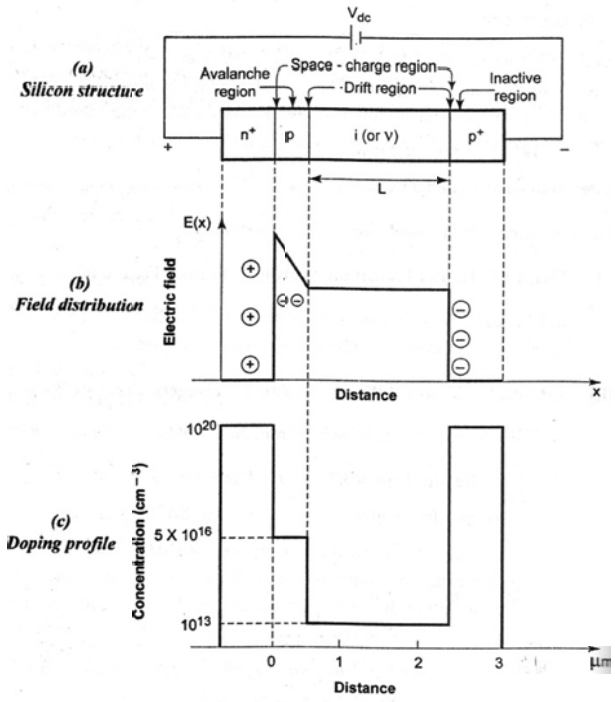


Fig. 4.35 : Gunn domain mod s

→ The thin p region at which avalanche multiplication occur. This region is also called the high field region (or) avalanche region.

→ The I or V region through which generated holes must drift in moving to the P^+ contact. T is region is also called the intrinsic (or) drift region.

→ The space between the n^+ -p junction & i -p^+ junction is called the space charge region.

→ Read diode oscillator consists of n^+ - p – i - p^+ diode biased in reverse and mounted in a microwave cavity.

→ The device can produce a negative ac resistance that delivers power from the dc bias to the oscillation.

Avalanche Multiplication

1. When the reverse biased voltage is well above the punch through (or) breakdown voltage. The space charge region always extends from the n^+ - p junction through the p and I regions to the I –p+ junction.

2. Carriers (holes) in the high field near the n^+ - p junction acquire energy to knock valence electrons into the conduction band, thus producing hole-electron pairs. The rate of production (or) AM is a sensitive nonlinear function of the field.

3. The transit time of a hole across the drift i-region L.

$$\tau = \frac{L}{V_d}$$

4. The avalanche Multiplication factor

$$M = \frac{1}{1-\left(\frac{V}{V_b}\right)^n}$$

$V \rightarrow$ applied voltage

$V_b \rightarrow$ avalanche breakdown voltage.

$n \rightarrow 3$ - 6 for Si is a numerical factor.

The breakdown voltage for a Si p^+ - n junction

$$|V_b| = \frac{q_n \mu_n s_S |E\ max|_b^2}{2}$$

$\rho_n \rightarrow$ Resistivity

$\mu_n \rightarrow$ electron mobility

$\varepsilon_s \rightarrow$ semiconductor permittivity, $E_{max} \rightarrow$ maximum electric field.

Carrier current $I_0(t)$ & External current $I_e(t)$

→ If the field is above the breakdown voltage and the carrier current $_0(t)$ generated at the $_{n^+}$ - p junction by the avalanche multiplication grows exponentially with time while the field is above the critical value.

→ During the negative half cycle, when the field is below the breakdown voltage, the carrier current $I_0(t)$ del ys exponentially to a small steady state value.

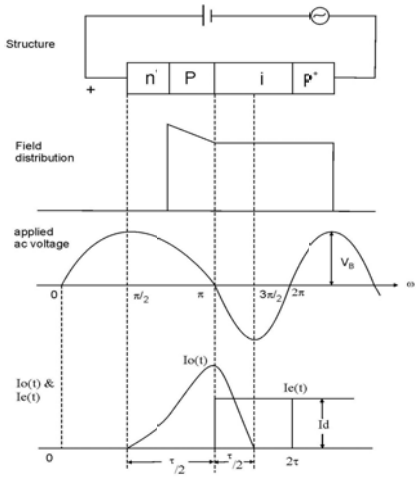


Fig. 4.36 : Fielld, "oltages & currents in Read liode

→ $Ie(t) = \frac{Q}{r} = \frac{Q \cdot V_d}{L}$

The applied ac Voltage & the external current Ie (t) are out of phase by 180^0 negative conductance occurs & the Read diode can be used for microwave oscillation & amplification.

Output power & quality factor Q

→ If Va is the amplitude of the ac voltage the ac power delivered is

$$P = 0.707\ V_a I_a \qquad \frac{W}{\text{unit area}}$$

The Q Factor

$$Q = \omega \frac{\text{Maximum stored energy}}{\text{Average dissipated power}}$$

4.7.2 IMPATT Diodes (Impact Ionization Avalanche Transit Time)

→ It has man forms, $n^+ P i P^+$ (or) $P^+ n i n^+$ read devices, $P^+ n n^+$ abrupt junction & $P^+ i n^+$ diode.

→ These diodes exhibit a differential negative resistance by two effects.

i) The impact ionization avalanche effect, which causes the carrier current $I_0(t)$ & the ac voltage to be out of phase by 90^0.

ii) The transit time effect, which further delays the external current $I_e(t)$ relative to the AC voltage by 90^0.

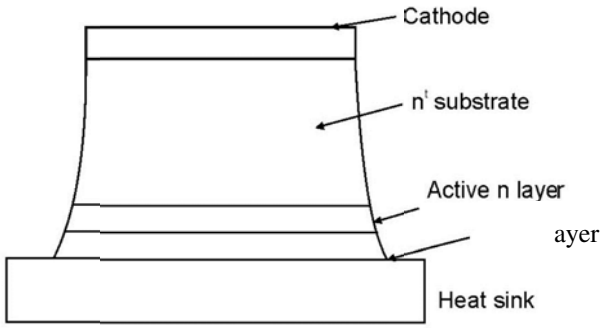


Fig.4.37 : Construction & Package of $P^+ n n^+$ IMPATT diode

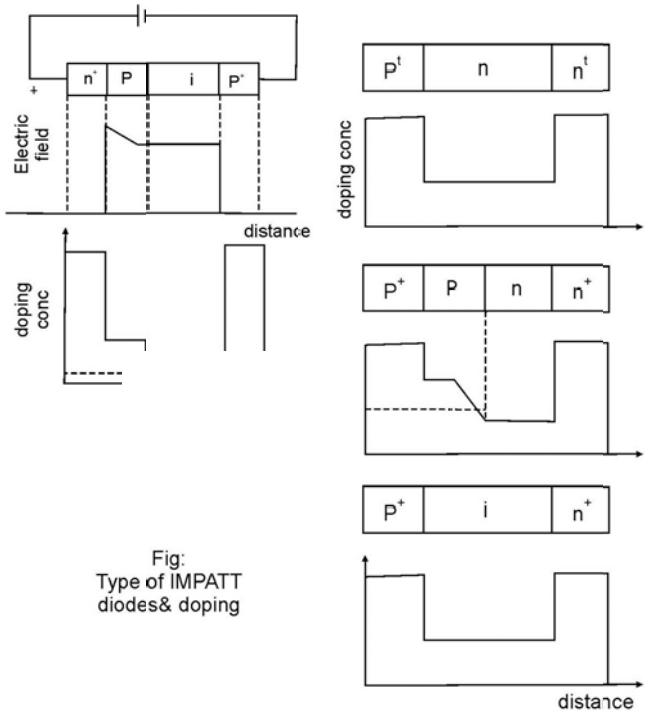


Fig:
Type of IMPATT
diodes& doping

Fig. 4.38 : Type of IMPATT diodes & doping profile

→ Many IMPATT diode consist of a high doping avalanching region followed by a drift region where the field is low enough that the carriers can traverse through it without avalanching.

→ It can be manufactured from Ge, Si, GaAs or InP. GaAs provides the highest efficiency, the highest operating frequency & least noise figure. But the fabrication process is more difficult & is more expensive than Si.

Negative Resistance

→ From the small analysis of a Read diode the real part of the diode terminal impedance is given by

$$R = R_S + \frac{2L^2}{V_d s_S A} \quad \frac{1}{1-\frac{m^2}{m_r^2}} \quad \frac{1-\cos 8}{0}$$

------ (1)

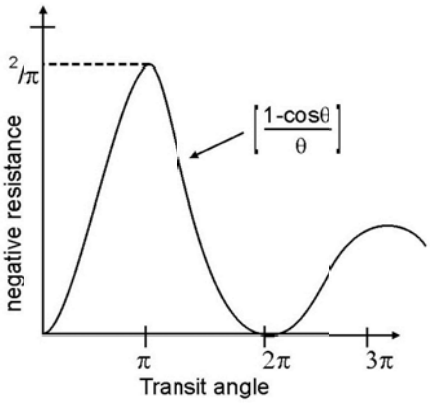


Fig.4. 9 : Negative resistance versus transit angle

Where Rs → Passive resistance of the inactive regions.

V_d → Carrier drift velocity,

L → length of the drift space charge region.

A → Diode Cross section, ε_S → semiconductor dielectric permittivity.

θ is the transit angle & it is given as

$$\theta = \omega \tau = \omega \frac{L}{V_d} \quad \text{----- (2)}$$

Wr → avalanche resonats frequency

$$\omega_r = \left[\frac{2 \alpha^F V_d I_o}{s_S A}\right]^{1/2} \quad \text{----- (3)}$$

Where α' → derivative of Ionization coefficient with respect to the Electric field.

→ The peak value of the negative resistance occurs near θ = π, for transit angles larger than π, the negative resistance of diode decreases rapidly.

→ Resonant frequency $f = \frac{1}{2r} = \frac{V_d}{2L}$ ----- (4)

Power Output & Efficiency

→ For a uniform avalanche the maximum voltage applied to the diode. Vm = EmL. ------ (5)

L - length of the depletion, region & E_m - maximum electric field.

This maximum applied voltage is limited by the breakdown voltage.

→ Maximum current $I_m = J_m.A = \sigma E_m A$.

$$= \frac{s_S}{r} E_m A = \frac{V_d s_S E_m A}{L} \quad \text{------ (6)}$$

The upper limit of the power output

$$P_m = I_m . V_m = E_m^2 \varepsilon_S V_d . A \quad \text{------ (7)}$$

The capacitance across the space charge region

$$C = \frac{s_S A}{L} \quad \text{----- (8)}$$

The efficiency of IMPATT diode is given by

$$\eta = \frac{P_{ac}}{P_{dc}} = \frac{\text{RF power output}}{\text{dc input power}} = \left(\frac{Va}{Vd}\right)\left(\frac{Ia}{Id}\right)$$

Va & Ia - ac voltage & current V_d & I_d dc - Voltage and current.

Performance characteristics

→ Theortical η = 30% (< 30% in practical) & 15% for Si, 23% for Ga As.

GaAs IMPATT have higher power & η in 40 to 60 GH_Z region Si IMPATT are produced with higher reliability & yield in the same frequency region.

4.7.3 TRAPATT Diode

→ TRAPATT stand for trapped plasma Avalenche triggered transit mode.

→ They are manufactured from Si, and have P^+ n n^+ (or) n^+ P P^+ structures with the n-type depletion region with the n-type depletion region width varying from 2.5 to 12.5 μm.

→ The p-n junction is reverse biased beyond the breakdown region so that the current density is higher. This causes the electric field in the space charge region to be decreased and the carrier transit time is increased.

Principles of operation

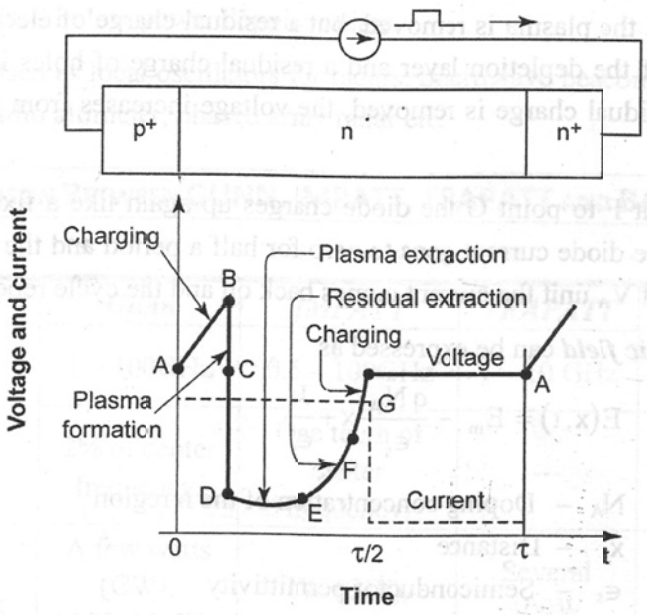


Fig. 4.40 : Voltage & current wave forms of TRAPATT diode

→ High field avalanche zone propagates through the diode & fills the depletion layer with a dense plasma of electrons & holes that become trapped in the low-field region behind the zone.

→ At point 'A' the electric field is uniform throughout the sample and its magnitude is large but less than the value required for avalanche breakdown.

→ The current density expressed by $J = \varepsilon_S \frac{dE}{dt}$

ε_S → semiconductor dielectric permittivity of diode.

→ At point A the current is turned on. At this instant the only charge carriers present are due to thermal generation.

→ The diode initially charges like a capacitor and magnitude of the electric field reaches above the breakdown voltage.

→ When a sufficient number of carriers are generated the particle current exceeds the external current and electric field is depressed throughout the depletion region causing the voltage to decrease. This portion of the cycle shown by the curve from point B to C & The voltage decreases to point P.

→ At point E the plasma is removed but charge of electrons remains in one end of the depletion layer & residual charge of holes in the other end. As the residual charge is removed, the voltage increases from point E to F.

→ From point F to G the diode charges up again like a fixed capacitor. At point G the diode current goes to zero for half a period and the voltage remains constant at V_A. unit the current comes back on & the cycle repeats.

→ The electric field can be expressed as

$$E(x, t) = E_m - \frac{q N_A}{\varepsilon_S} x + \frac{J t}{s_S} \qquad \text{---- (1)}$$

where

N_A → Doping concentration of n region. X → distance, ε_S → semiconductor permittivity E_m → Electric field &

$$t = \left(\frac{q N_A}{J}\right) x \qquad \text{-----(2)}$$

Differentiating above equation w. r. to 't' we get V_z avalanche – zone velocity

$$V_z = \frac{dx}{dt} = \frac{J}{q N_A} \quad \text{---- (3)}$$

The transit time of the carrier is given by

$$\tau_S = \frac{L}{V_s} \quad \text{---- (4)}$$

$V_s \rightarrow$ saturated carrier drift velocity.

4.8 Parametric Devices

→ A parametric device uses linear reactance, or a time varying reactance. Parametric excitation can be subdivided into parametric amplification & oscillation.

4.8.1 Non-linear Reactance

Reactance → It is defined as a circuit element that stores and releases electromagnetic energy as opposed to a resistance, which dissipates energy.

Capacitive → If the stored energy is predominantly in the electric field, the reactance is said to be capacitive.

Inductive → If the stored energy is predominantly in the magnetic field, the reactance is said to be inductive.

→ A capacitive reactance is a circuit element for which capacitance is the ratio of charge on the capacitor over voltage across the capacitor.

$$C = \frac{Q}{V} \quad \text{------ (1)}$$

If the ratio is non-linear, the capacitive reactance is said to be non-linear. A nonlinear capacitance is defined as the partial derivative of charge with respect to voltage.

$$C(V) = \frac{6Q}{6V} \quad \text{----- (2)}$$

Nonlinear Inductance

$$L(i) = \frac{6\emptyset}{6i} \quad \text{----- (3)}$$

Small signal method

→ It is assumed that the signal voltage V_s is much smaller than the pumping voltage Vp (Vs << Vp) and the total voltage across the non-linear capacitance C(t) is given by, $v = v_s + v_p$

$$= Vs \cos(\omega_{st}) + Vp \cos(\omega_{pt}) \quad \text{------ (4)}$$

The charge on the capacitor can be expanded in a Taylor series, where Vs = 0.

$$Q(V) = Q(V_1 + V_P) = Q(V_P) + \left.\frac{d\,Q(V_P)}{dV}\right| Vs = 0 \quad \text{----- (5)}$$

For convenience, it is assumed that

$$C(V_P) = \frac{d\,Q(V_P)}{dV} = C(t) \quad \text{------ (6)}$$

(C (Vp) is periodic with a fundamental frequency of ω_p.

If the capacitance C (Vp) is expanded in a Fourier series

$$C(V_P) = \sum_{n=0}^{\alpha} C_n \cos(n.\,\omega_P t) \quad \text{------ (7)}$$

V_P is a function of time, the capacitance C (V_P) is also function of time,

$$C(t) = \sum_{n=0}^{\alpha} C_n \cos(n\,\omega_P t) \quad \text{------ (8)}$$

The co-efficient C_n are the magnitude of each harmonic of the time varying capacitance, c_n are not linear functions of the ac pumping voltage v_p. Therefore the junction capacitance (c(t)) of a parametric diode is a not linear capacitance.

The current through the capacitance (C(t))

$$i = \frac{dQ}{dt} = \frac{dQ(V)}{d(t)} = \frac{d}{dt}\left[Q(V_P) + C(t)\,V_S\right]$$

$$= \frac{d}{dt}\,Q(V_P) + \frac{d}{dt}\,(C(t))\,V_S \quad \text{------ (9)}$$

This non-linear capacitance behaves like a time-varying linear capacitance for signals with amplitudes that are much smaller than the amplitude of the pumping voltage.

Large signal method

If the signal voltage is not small compared with the pumping voltage, the Taylor series can be expanded about a dc bias voltage V_0 in a junction diode. The capacitance C is proportional to the $(\phi_0 - V)^{-½} = V_0^{-½}$

$\phi_0 \rightarrow$ Junction barrier potential,

$V \rightarrow$ negative voltage supply.

The capacitance C(t) can be expressed as

$(C(t)) = C_0 [1 + 2\gamma \cos(\omega_P t)]$ for Vp << Vs.

→ The parameter γ is proportional to the pumping voltage V_P & indicates the coupling effect between the voltages at the signal frequency fs & the output frequency fo.

4.8.2 Manley – Rowe power relations

→ Manley derived a set of general energy relations one signal generator and one pump generator at their respective frequencies fs & fp, together with associated series resistances and band pass filters are applied to a non-linear reactance C(t).

→ In the presence of two applied frequencies fs & fp an infinite nunber of resonant frequencies of $mf_p \pm nf_s$ are generated where m & n are any integers.

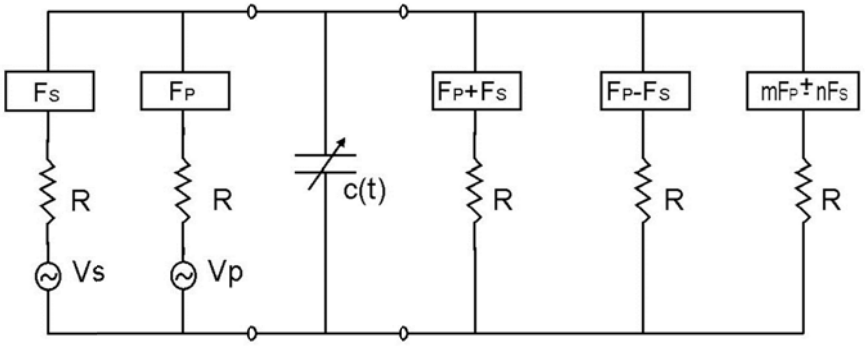


Fig. 4.41 : Equivalent circuit for manley –rowe derivation

→ Voltage across the non linear capacitor (C(t)) in exponential form.

$$V = V_P + V_S = \frac{V_p}{2}(e^{jm_p t} + e^{-jm_p t}) + \frac{V_s}{2}(e^{jm_s t} + e^{jm_s t}) \quad \text{----- (11)}$$

The charge Q deposited on the capacitor

$$Q = \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} Q_{m,n} e^{j(mm_p t + nm_s t)} \quad \text{------ (12)}$$

The charge Q to be real

$$Q_{m,n} = Q^*_{-m-n} \quad \text{----- (13)}$$

The total voltage V can be expressed as a function of the charge Q,

$$V = \sum_{m=-\alpha}^{\alpha} \sum_{n=-\alpha}^{\alpha} V_{m,n} e^{j(mm_p t + nm_s t)} \quad \text{------ (14)}$$

The voltage to be real,

$$V_{m,n} = V^*_{-m-n} \quad \text{------ (15)}$$

The current flowing through C(t) is the total derivative of Q with respect to time.

$$I = \frac{dQ}{dt} = \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} j(m\omega_p + n\omega_s) Q_{m,n} e^{j(mm_p t + nm_s t)}$$

$$= \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} I_{m,n} e^{j(mm_p t + nm_s t)} \quad \text{------ (16)}$$

Where $I_{m,n} = j^{(m\omega p + n\omega s)} Q_{m,n}$ & $I_{m,n} = I^*_{-m-n}$.

The capacitance C(t) is assumed to be pure reactance, the average power at the frequencies mfp + nfs is

$$P_{m,n} = [V_{m,n} I^*_{m,n} + V^*_{m,n} I_{m,n}]$$

$$= [V_{*-m-n} I_{-m-n} + V_{-m-n} I_{*-m,-n}] = P_{-m,-n} \quad \text{----- (17)}$$

The conservation of power can be written as

$$\sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} P_{m,n} = 0 \quad \text{----- (18)}$$

Multiply the factor $\frac{(mm_p+nm_s)}{(mm_p+nm_s)}$

$$\sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} P_{m,n} \frac{(mm_p+nm_s)}{(mm_p+nm_s)} = 0$$

$$\omega p \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \frac{mP_{m,n}}{mm_p+nm_s} + \omega s \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \frac{mP_{m,n}}{mm_p+nm_s} = 0 \quad \text{----- (19)}$$

The charges $Q_{m,n}$ are then also unchanged, since they are functions of the voltages $V_{m,n}$.

$$\sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \frac{mP_{m,n}}{mm_p+nm_s} = 0 \quad \text{----- (20)}$$

Similarly $$\sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \frac{mP_{m,n}}{mm_p+nm_s} = 0 \quad \text{----- (21)}$$

Equation (20) can be expressed as two terms

$$\sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \frac{mP_{m,n}}{mm_p+nm_s} + \sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \frac{-mP_{m,n}}{-mm_p+nm_s} = 0 \quad \text{----- (22)}$$

Where n & m replaced by –n & -m

$P_{m,n} = P_{-m,-n}$ two parts are equal.

$$\sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \frac{mP_{m,n}}{mf_p+nf_s} = 0 \quad \text{------ (23)}$$

Similarly $$\sum_{m=-\infty}^{\infty} \sum_{n=-\infty}^{\infty} \frac{mP_{m,n}}{mf_p+nf_s} = 0 \quad \text{----- (24)}$$

ω_P & ω_S have been replaced by f_P & f_S. Equations (22) & (23) are the standard forms for the Manley Rowe power relations.

Under these restrictions n = 0, m = ± 1 and n = ± 1, m = 0 and n = m = ± 1 then equations (23) & (24) reduce to

$$\frac{P_{1,0}}{f_P} + \frac{P_{1,0}}{fp+fs} = 0 \qquad \text{------ (25)}$$

$$\frac{P_{1,0}}{f_s} + \frac{P_{1,0}}{fp+fs} = 0 \qquad \text{----- (26)}$$

$P_{1,0}$ & $P_{0,1}$ are the power supplied by the two generators at the frequencies f_P & f_S and they are considered positive.

→ $P_{1,1}$ flowing from the reactance into the resistive load at a frequency of $f_P + f_S$ is considered negative.

Power Gain

- **Up converter**

→ It is defined as "the ratio of the power delivered by the capacitor at a frequency of $f_P + f_S$ to that absorbed by the capacitor at a frequency of f_S".

$$\text{Gain} = \frac{fp+fs}{fs} = \frac{f_0}{f_S} \quad \text{(for modulator)} \qquad \text{----- (27)}$$

Where $f_P + f_S = f_0$ & $(f_P + f_S) > f_0 > f_S$.

This type of parametric device is called the sum frequency parametric amplifier (or) up converter.

Down converter

→ If the signal frequency is the sum of the pump frequency & the output frequency.

$$\text{Gain} = \frac{fs}{fp+fs} \quad \text{(for demodulator)} \qquad \text{----- (28)}$$

where $fs = fp + f_0 \Rightarrow f_0 = fs - fp$

Negative resistance parametric amplifier

$fp = fs + f_0$

The power $P_{1,1}$ supplied at f_P is negative. Both $P_{1,0}$ & $P_{0,1}$ are negative.

4.9 Parametric Amplifiers

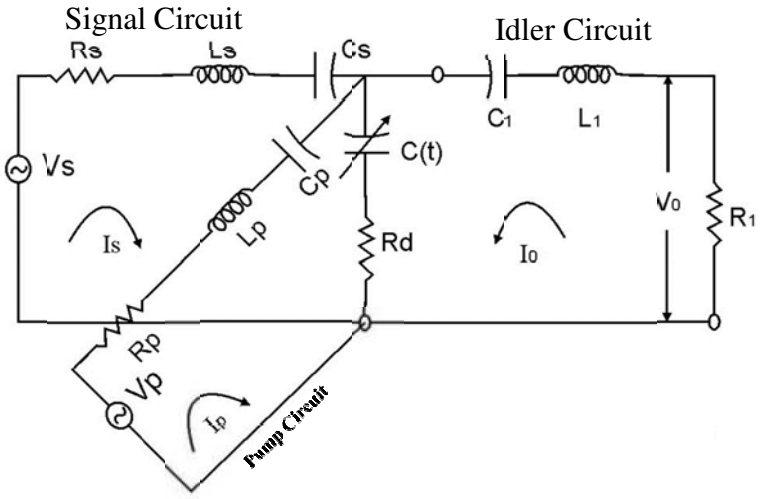


Fig. 4.42 : Equivalent circuit for a parametric amplifier

In a parametric amplifier the local oscillator is replaced by a pumping generator such as a reflex klystron & the nonlinear element by a time, capacitor such as varactor diode (or) Inductor.

→ The signal Frequency fs & pump frequency fp are mixed in a non-linear capacitor (C(t)) to generate voltages at fundamental frequencies fp & fs as well as the sum & different frequencies mfp $\pm$ nfs across (C(t)).

→ An output voltage at fo is obtained across load esistance R_L.

Idler circuit

→ It is a output circuit which does not require external excitation. The output frequency (or Idler) fo is expressed as the sum & difference frequencies of the signal frequency fs & pump frequency fp.

$$f_o = mfp \pm nfs \qquad \text{----- (29)}$$

Where m, n → positive integers from 0 to α.

If fo > fs → Parametric up converter. Fo < fs → Parametric down converter.

Parametric Up Converter (PUC)

Properties of PUC

i) The output frequency is equal to the sum of the signal frequency & the pump frequency.
ii) There is no power flow in the parametric device at frequencies other than the signal, pump and output frequencies.

Parameters

1) Power Gain

$$\text{Maximum power gain} = \frac{f_0}{f_s} \frac{x}{(1+\sqrt{1+s})^2}$$

$$\text{where } fo = fp + fs \;\&\; x = \frac{f_s}{f_0} (\gamma Q)^2, \; Q = \frac{1}{2u f_s C R_d}$$

$R_d \rightarrow$ series resistance of a p-n junction diode &

$\gamma Q \rightarrow$ figure of merit, $\frac{x}{(1+\sqrt{1+s})^2}$ = gain degradation factor.

2) Noise figure

$$F = 1 + \frac{2T_d}{T_0} \left(\frac{1}{\gamma Q} + \frac{1}{(\gamma Q)^2} \right)$$

$T_d \rightarrow$ diode temperature in degree kelvin degrees

$T_0 \rightarrow$ Ambient Temperature (300^0 k) &

$\gamma Q \rightarrow$ figure of merit

Bandwidth

$$BW = 2\gamma \sqrt{\frac{f_0}{f_s}}$$

Parametric Down Converter (PDC)

$$\text{Gain} = \frac{f_s}{f_0} \frac{x}{(1+\sqrt{1+s})^2}$$

Negative Resistance Parametric Amplifier

Power Gain

$$\text{Gain} = \frac{4f_i}{f_s} \quad \frac{R_g R_i}{R_{TS}\, R_{Ti}} \quad \frac{a}{(1-a)^2}$$

where fi = fp – fs, Rg → output resistance of signal generator, Ri → output resistance of idler generator, R_{TS} → Total series resistance at f_s. R_{Ti} → Total series resistance ax fi.

$a = \frac{R}{R_{TS}}$, $R = \frac{y^2}{(m_s m_i € R_{Ti})}$ is equivalent negative resistances.

Noise figure:

$$F = 1 + 2\frac{T_d}{T_0}\left[\frac{1}{\gamma Q} + \frac{1}{(\gamma Q)^2}\right]$$

Bandwidth:

$$BW = \frac{y}{2}\sqrt{\frac{f_i}{f_s \text{ gain}}}$$

Degenerate parametric Amplifier (or) Oscillator

→ It is defined as a negative resistant amplifier with the signal frequency equal to idler frequency.

$f_i = f_p - f_s$, $f_s = f_p - f_i$ & $f_p = 2f_s$, $\boxed{f_s = \frac{fp}{2}}$

If $f_p \neq 2\, f_s$ it is called a non –degenerate power amplifier.

Power Gain & Bandwidth

→ They are exactly same as for PUC.

→ With fs = fi & fp = 2fs the power transferred from pump to signal frequency is equal to the power transferred from pump to Idler frequency.

Noise figure

$$F_{SSB} = 2 + 2\frac{\overline{T_d}}{T_O}\frac{R_d}{R_g}, \qquad F_{DSB} = 1 + \frac{\overline{T_d}}{T_O}\frac{R_d}{R_g}$$

F_{SSB} : Single side band noise figure F_{DSB} : double side band noise figure.

$\overline{T_d}$ → Average diode temperature in degrees kelvin To = 300^0K.

R_d → Diode series resistance, in ohms

Rg → External output resistance of signal generator in ohms.

4.10 Fabrication Process of Microwave Monolithic Integrated Circuit (MMIC)

Manufacturing of IC's

Various steps involved in manufacturing of IC's using silicon planar technology are given below.

a) Silicon wafer or substrate preparation
b) Epitaxial growth
c) Oxidation
d) Photolithography
e) Diffusion and Ion Implementation
f) Isolation
g) Metalization

a. Silicon Wafer or substrate preparation

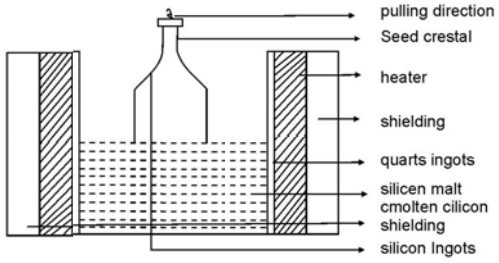


Fig. 4.43 : Czochralski process

Basic raw material used in manufacturing of IC's is wafer. It's other name is disk of silicon. Wafer is obtained from silicon ingots are obtained using czochralski method.

Czochralski process

- Malten silicon (melt) is contained in a quartz rucible.
- It is surrounded by a graphite radiator.
- Graphite is heated by radio frequency induction. The temperature is maintained above 1425^0C.
- Seed crystal is dipped into the melt to initiate single-crystal growth.

- Controlled amount of impurity is added to melt, to provide required electrical properties.
- Initially, the seed is dipped into melt, then seed is gradually withdrawn vertically from melt while simultaneously seed is rotated.
- During the crystal pulling process, the seed crystal and crucible are rotated in opposite direction to produce the ingots with circular cross – section.
- The diameter of the ingot is controlled by the pulling rate, melting temperature and seed rotation rate.
- Diameter of wafer is varied from 75 mm to 250 mm.
- Thickness of wafer is usually 1 mm.
- Wafer is prepared from ingots by using interval cutting edge diamond blades.
- After slicing the ingot into various wafers, one face of wafer is polished to a flat surface like mirror.

b) Epitaxial growth

'Epitaxy' means arranging atoms in single crystal fashion upon a single crystal substrate.

Epitaxial growth means growing a single crystal film on Si surface. At that time, wafer (Substrate) is subjected to above 800^0C temperature. These epitaxial films are required with specific impurity concentration.

It is done by introducing PH_3 impurity to get n-type B_2H_6. Impurity is introduced for p-type doping. This process is carried out in the reaction chamber. Christo Ananth et al.[3] presented a short overview on two port RF networks. They widely used microwave and RF applications and the denomination of frequency bands. The monograph start outs with an illustrative case on wave propagation which will introduce fundamental aspects of high frequency technology.

c) Oxidation

In this process, SiO_2 layer grows equally above wafer is vertical direction. There are two types of oxidation process available.

1. Wet oxidation

This is the Rapid process. In this process, oxidation atmosphere contains water vapour 900^0C – 1000^0C temperature is maintained.

2. Dry oxidation

In this process, oxidating atmosphere is pure oxygen. 1200^0C temperature is maintained in this process.

d. Photolithography

By using this more than 10,000 transistors can be fabricated within 1 x 1 cm chip.

Techniques used in photolithography:

Two techniques are used in photolithography.

a) UV light exposure technique.
b) X-ray (or) EBL (Electron Beam lithographic) technique.

Process involved in lithography

i. Masking process
ii. Photo etching process

Masking Process

Masking process is used to identify the place in which ion implanted should not be occurred. Photoresists, polysilicon, SiO_2 – SiN are mostly used as masking materials.

Christo Ananth et al. [4] discussed about RF Transistor Amplifier Design and Matching Networks, amplifier power relation, impedance , T π and microstripline matching networks. The figure shows that wafer is coated with photo resists. Above this, masking pattern is placed. Then, it is exposed to UV rays. The figure shows the technique of UV radiation. This UV rays removes photoresists material in masking area. It is shown in fig. After completing the masking process etching process will be started.

Photo Etching

It has two types, namely wet etching and dry etching (plasma etching). In wet etching process, chip is immersed in the etching solution. It removes the SiO_2 from the areas which are not protected by photo resist film.

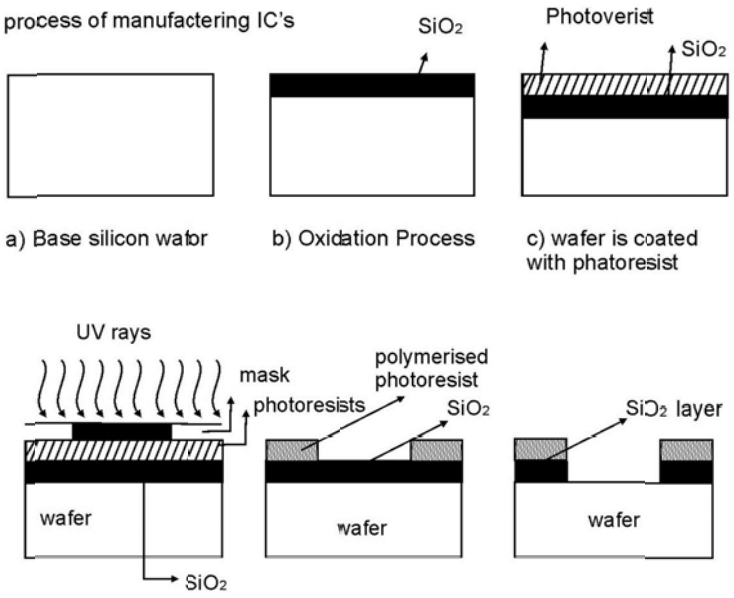


Fig. 4.44 : d) wafer with mask is exposed to UV rays e) wafer before etching f) wafer after etching

e) Diffusion and Ion-Implantation

Diffusion is the important process in the fabrication of IC's. In this process, impurities are diffused into the silicon chip, 1000^0C temperature is maintained in this process. Normally B_2O_3 and P_2O_3 are used as impurities. Dry oxygen or Nitrogen is used to sweep the impurities to the high temperature zone. Diffusion process usually takes two hours. It is explained in the N-MOSFET Fabrication process.

Ion – Implantation is other technique used to introduce impurities into the wafer. It is performed at low temperature.

f) Isolation

This process is necessary to provide electrical isolation between different components and interconnections. Mostly two techniques are used which are given below,

i) PN junction isolation
ii) Dielectric isolatio n

Christo Ananth et al.[5] analyzed Microwave Passive Components, microwave waveguides such as microwave T junctions , circulators, attenuators and Isolators.

g) Metallization

This process is used to produce thin film layer to make interconnections of various components on the chip. Aluminum is used for this purpose.

Above steps are followed to manufacture any IC using silicon planar technology.

Fabrciation of n-channel MOSFET

Steps involved in the fabrication process

Generally polysilicon is used as gate electrode of n-MOSFET.

Step 1 :

Generally two types of oxide coating done in this fabrication process. Si_3N_4 is first coated on entire surface of p-substrate (wafer). It is shown in figure.

Step 2:

By using masking process gate, source, drain area are defined. These portions are etched from the oxide layer. It is shown in figure.

Step 3:

After that, this oxide layer is deposited above p-substrate. It is shown in figure.

Step 4:

Polysilicon layer is deposited above oxide layer, gate portion is defined by mask, and remaining portion is etched. It is shown in figure.

Step 5:

n^+ source region and n^+ drain region are formed by ion implantation technique. The area below the polysilicon gate will not be affected by ion implantation. It is shown is figure.

Step 6:

SiO_2 layer is deposited above substrate. Now entire wafer is protected by SiO_2 layer. It is shown in figure.

Step 7:

Finally, c ntact areas are defined by using photolithography process for gate, source, drain.

Fabrication of n-MOSFET:

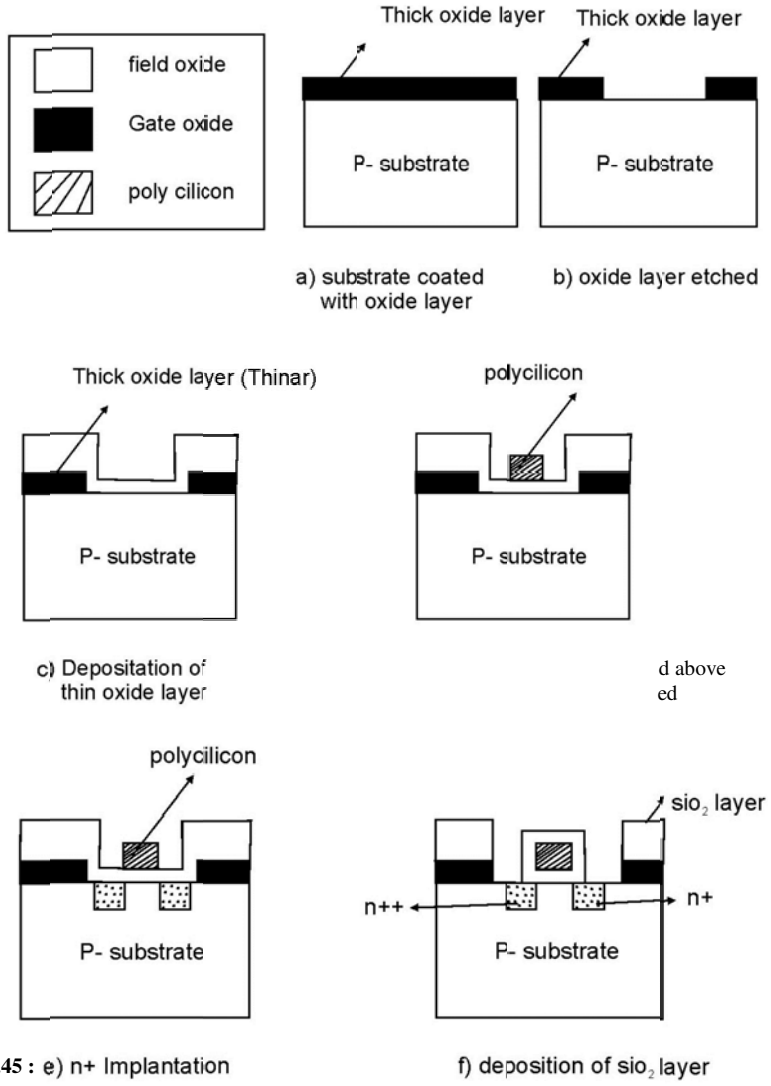


Fig. 4.45 :

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Problems :

1. A GaAs MESFET has the following parameters

   $R_g = 3\Omega$, $R_i = 25\ \Omega$, $g_m = 50\mho$

   $R_d = 450\ \Omega$, $R_s = 2.5\ \Omega$, $C_{gs} = 0.60$ pf

   Find (i) Cutoff frequency

   (ii) Maximum operating frequency

Solution:

(i) $fC_0 = \frac{gm}{2\ u\ C_{gs}}$

$= \frac{50 \times 10^{-3}}{2u \times 0.60 \times 10^{-12}}$

$fC_0 = 13.26\ GH_Z$

(ii) $f_{max} = \frac{f€_o}{2} \left(\frac{Rd}{R_S + R_g + R_i} \right)^{1/2}$

$f_{max} = 49.73\ GH_Z$

2. An n-type GaAs g_{unn} diode has the following parameter electron drift velocity $Vd = 2.5 \times 10^5$ m/s negative electron mobility $|\mu_n| = 0.015\ m^2/V$ sec. Relative dielectric constant $\varepsilon_r = 13.1$. Find the criterion for classifying the modes of operation.

Solution:

The criterion is $\frac{sVd}{e\,|\,\mu_n\,|} = \frac{s_O\ s_r\ V_d}{e\,|\,\mu_n\,|}$

$\frac{sVd}{e\,|\,\mu_n\,|} = 8.854 \times 10^{-2} \times 13.1 \times 2.5 \times 10^5$

$= 1.2 \times 10^6\ m^2$ or $1.2 \times 10^{12}\ cm^2$

The product of doping concentration and the device length must be,

$n_0 L > 1.2 \times 10^{12}/cm.$

3. The IMPATT diode has the following parameters carrier drift velocity $V_d = 2 \times 10^{-1}$ cm/s. Drift region length L = 6μm. Maximum operating voltage Vmax = 100V, Maximum operating current Imax = 200 mA. Efficiency $\eta = 15\%$. Breakdown voltage $V_{bd} = 90$ V. Find

(i) Maximum output power output

(ii) Resonant frequency.

Solution:

(i) Maximum output power in watt

$$P = \eta I_{dC} = 15 \times 200 \times 10^{-3} = 3w$$

(ii) Resonant frequency

$$f = \frac{Vd}{2L} = \frac{2 \times 10^{-1}}{2 \times 6 \times 10^{-6}}$$

$$f = 16.67 \text{ GHz}$$

4. A TRAPATT diode has the following parameters

Doping concentration $N_A = 2 \times 10^{15}$ cm^{-3}

Current density J = 20 KA/cm^2

Calculate the avalanche zone velocity.

Solution:

$$Vz = \frac{J}{q N_A} = \frac{20 \times 10^3}{1.6 \times 10^{-19} \times 2 \times 10^{15}}$$

$Vz = 6.25 \times 10^7$ Cm/s

5. A Ga As MESFET has channel height A = 0.1 μm Electron concentration $N_d = 8 \times 10^{17}$ cm^{-3}. Relative dielectric constant $\varepsilon_r = 13.10$. Find the pinchof/voltage.

Solution :

$$Vp = \frac{q N_d a^2}{2 s_r s_O}$$

N_d = $8 \times 10^{17}\ cm^{-3} = 8 \times 10^{17}/cm^3 = 8 \times 10^{17} \times 10^6$

= $8 \times 10^{23} m$

$$V_p = \frac{1.6 \times 10^{-19} \times 8 \times 10^{23} \times (0.1 \times 10^{-6})}{2 \times 13.10 \times 8.854 \times 10^{-12}}$$

$V_p = 6V$

For $\varepsilon_r = 11.80$

$$V_P = \frac{1.6 \times 10^{-19} \times 8 \times 10^{23} \times (0.1 \times 10^{-16})^2}{2 \times 11.80 \times 8.854 \times 10^{-12}}$$

Vp = 6.6 V

6. Conductivity of an n-type GaAs g_{unn} diode has electron density n = $10^{18}\ cm^{-3}$, electron density at lower valley $n_l = 10^{10}\ cm^{-3}$, electron density as upper valley $10^8\ cm^{-2}$, Temperature t = 300 k. Find the conductivity of gunn diode.

Solution:

$\sigma = e(\mu_l n_l + \mu_u n_u)$

$\sigma = 1.6 \times 10^{-19} [(8000 \times 10^{-4} \times 10^{10} \times 10^6) + (180 \times 10^{-4} \times 10^8 \times 10^8)]$

(. . refer two valley model theory)

σ . = 1.28×10^{-3} mhos

σ = 1.28 m mhos

7. An n-type GaAs Gunn diode has the following parameters threshold field Eth = 2800 V/cm. Applied Field E = 3200 V/cm. Device length L = 10 μm, Doping concentration $n_0 = 2 \times 10^{14}\ cm^{-2}$. Operating frequency f = 10 GHz

Calculate,

(i) Electron drift velocity

(ii) Current density

(iii) Negative electron mobility

Solution:

(i) Vd = fL = $10 \times 10^9 \times 10 \times 10^{-6}$

Vd = 10^5 m/s (or) 10^7 cm/s

(ii) J = qnV

$= 1.6 \times 10^{-19} \times 2 \times 10^{14} \times 10^{6} \times 10^{5}$

$J = 3.2 \times 10^{6}\ A/m^2$ (or) $320\ A/cm^2$

(iii) $\mu n = \frac{Vd}{E} = \frac{10^{7}}{3200}$

$Mn = -3100\ cm^2 / V\text{-sec}.$

8. An up-converter parameter Amplifier has the following parameters.

Ratio of output frequency over signal frequency = 25

Figure of merit $\gamma Q = 10$

Factor of merit figure $\gamma = 0.4$

Diode temperature id = 350 k.

Calculate (i) power gain m dB

(ii) Noise figure

(iii) Bandwidth

Solution:

(i) Power gain $= \frac{f_0}{f_s} \frac{x}{(1+\sqrt{1+s})^2}$

$x = \frac{f_0}{f_s} (y_Q)^2 = \frac{1}{25 \times 10^2} = \frac{1}{25 \times 100}$

$x = 4$

Power gain $= -25 \frac{4}{(1+\sqrt{5})^2}$

$= 25 \frac{4}{1+5+2\sqrt{5}} = 9.549$

Power gain in dB = 10 log 9.55

$= 9.80$ dB

(ii) Noise figure $F = 1 + \frac{Td}{To} \left[\frac{1}{y_Q} + \frac{1}{(y_Q)^2}\right]$

To = 300 k

$F = 1 + \frac{350}{300} \left[\frac{1}{10} + \frac{1}{10^2}\right]$

$= 1 + 1.16667\ (0.1 + 0.01)$

F = 1.256

F m dB = 10 log F = 0.99 = 1 dB

(iii) $\text{Bandwidth} = 2\gamma \int_{f_s}^{f_0} = 2 \text{ x } 0.4 \text{ x } \sqrt{25} = 0.8 \text{ x } 5 = 4$

Bandwidth = 4

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