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POWER QUALITY IMPROVEMENT USING TRANSFORMERLESS HYBRID POWER FILTER WITH NSTL INVERTER

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Abstract: The most important power quality problem is associated to generation of current harmonics by nonlinear loads like thyristor and diode front-end rectifiers. Presently, some methods based on dual-inverter configurations are to be very attractive, where the APF (Active Power Filter) HPF (hybrid power filter) must deal with high nonlinear loads having greater value of di/dt and supplies the reactive power together with harmonic mitigation. The drawback of dual inverter is the more number of switching devices. Hence, we proposes a Transformerless Hybrid Power Filter based on a new "nine-switch three leg inverter" with an improved harmonic mitigation. Apart from presenting a less number of switches when differentiate with dual topologies, the proposed method is capable of providing full compensation even for loads with higher harmonic content. Simulation and Experimental results are presented for a Hybrid Power Filter inverter is compared with, D-STATCOM, UPQC, DVR FACTS devices in order to show that the harmonic mitigation performance meets the IEEE 519 standard.

Keywords: Active power filters (APFs), diode rectifiers, harmonics, hybrid power filters (HPFs).Nine switch three leg inverter (NSTL),

I.INTRODUCTION

In recent days, the higher number of computers and some sensitive electrical Loads connected to the power grid are directly affected by power quality issues [1]. The most important is associated to generation of current harmonics by nonlinear loads like thyristor and diode front-end rectifiers. Resulting, these harmonics can cause voltage disturbance, additional loss in the power system, and breakdown of sensitive electronic equipment. For this reason, harmonic mitigation standards, such as IEEE 519[2], has been recommended to bind the harmonic currents injected to the grid by nonlinear loads. Shunt passive filter, consisting of tuned *LC* filter and high pass filter, have been conventionally used as a simple and cheap solution to compensate current harmonics. Although, their performance firmly rely on the grid impedance and it may possibly cause the unwanted parallel resonance phenomena with the grid. In the previous decades, the increasing of power semiconductor devices has encouraged the development of power electronics solutions to the issues of harmonic flow into the grid.

The shunt active power filter, which essentially consists of voltage source converter with a larger capacitor on the DC link, is considered a proven solution to limit [3]-[4].current harmonics over conventional limits.

Another method, known as a hybrid power filter, mixing a low-level active filter source with a passive filter, focusing on cost reduction [14]. The inverter used in the hybrid power filter generally requires 5% to 8% of the kV ampere ratings, which is considerably lower than the rated power of the conventional active filter, which makes hybrid power filter systems to agreeable and cost effective.

The principle of operation of these inverters is based on improving the filtering characteristics of passive filter and avoid unwanted resonances with the grid.

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Regrettably, most of these hybrid power filter topologies have a common problem, the greater number of passive components and transformer directly influence the weight and size of these filters [14]-[22]. On the other hand, there has been more effort to reduce the number of components in the hybrid power filters. Feeding the hybrid filter comprising a three-phase source of less power converter connected to the load at the common coupling point through a passive LC filter without matching transformer is provided [23]. The LC filter absorbs the harmonic currents generated by the non-linear load, while the active filter improves the filtering characteristics of the LC filter.

A reduced hybrid power filter without transformer operation has been proposed [24]. This was done by taking a one phase leg switches to rearrange the third leg phase of the middle point of split Dc-link capacitor. This is possible because the filter capacitors LC block the DC components created by the connection of one phase to the negative terminal of the DC link. An advantage, reducing switching topologies are more efficient, have a cheap cost and complexity. The main advantage of this topology is the compensation capability. Not only an improved compensation performance but also a reduction in costs,
this features a transformerless hybrid power filter based on a new nine-switch three leg inverter(NSTL) derived from twelve switches. Inverter with two sets of three-phase outputs using only nine switches. This feedback control uses a more direct control of each front NSTL inverter unit and also controls the DC link voltage.

II.HYBRID POWER FILTER

Since the nine switch inverter is a latest topology, the proposed hybrid power filter PF (fig.1) has some unusual that should be noted. First of all, the problem of direct current flow normally occurring in parallel inverters (inverters connected to the same side of the DC link and the Point of Common Coupling from the AC side) it also happens in nine switch inverters[27][28], if the passive LC filters are not present. By way of example, if the switches SA and SR are closed (open SAR), the output phase A would be connected to the positive DC rail and the negative DC rail of output phase R. Since the two output terminals would be connected to the same phase in the AC section (no passive LC filters), a short circuit in the intermediate circuit current and a destructor current will occur. Fortunately, in the proposed topology, the passive LC filter capacitors (CFTOP and CFBOT) share the DC link voltage and block the DC current, avoiding any possible short circuit between the inverter units. Secondly, since the two units share the DC link, the nine switch inverter require a minimum DC link voltage equal to the sum of the output line voltages of the upper and lower units (to simplify , Consider that both units are in series and connected to the DC link). This would also be a problem in APF applications where invertors synthesize not only the harmonic frequency components but also the fundamental frequency voltage network, making the high DC link voltage requirement of Voltage source inverter doubled in nine switch Invertor. Providentially, in HPF applications, passive filters manage the fundamental frequency voltage of the grid (filter capacitors are responsible), leaving, for the invertor only the synthesis of the harmonic frequency components. Therefore, the DC link voltage requirement HPF is much lower than in the conventional APF (typically one tenth). For this reason, doubling the DC link voltage binding requirement is not a problem in the topology implemented. In this section, the nine switch inverter is analyzed and a specific modulation technique is presented. Subsequently, the design guidelines of passive LC filters are followed.

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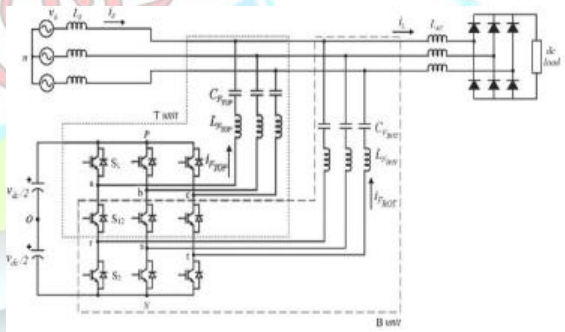

Fig. 1. Proposed transformerless HPF based on a nine switch inverter.

[Sj, Sk] switch states for the T and B units

[Vjo, Vko] output voltages for the T and B units

[Vdc] nine switch inverter dc link voltage

[Tsw] nine switch inverter switching period

[Djtop, Dkbot] duty cycles for the T and B switches

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[LFTOP, LFBOT] inductances for the T and B LC filters

[CFTOP, CFBOT] capacitances for the T and B LC filters

[VCFTOP, VCFBOT] capacitor voltages for the T and B LC filters

[QLC] total reactive power supplied by the T and B LC filters

[ω1] fundamental angular frequency of the grid

[VPCC] amplitude of the grid phase voltages at the PCC

[iαβ , idq] current space vectors in stationary αβ and in rotating dq reference frames

[VαβTOP ,VαβBOT] feedback reference voltage space vectors for the top and bottom inverter units

[kTOP, kBOT] feedback proportional gain for the T and B units

[iSαβ] harmonic components of the grid current space vector

[VFαβ5,V Fαβ11] feedforward reference voltage space vectors for the T and B inverter units

[ZFTOP 5, ZFBOT 11] top and bottom LC filter impedances for the 5^{th} and 11^{th} harmonic components.

[_iLαβ5,iLαβ11] load current space vectors for the 5^{th} and 11^{th} harmonic components

[iαβ, dc] reference current space vector for the dc-link voltage control 13^{th}.

III.NINE SWITCH THREE LEG INVERTER

In the nine switch inverter, shown in Fig.1, each leg is composed by three switches and two available output terminals. This methodology results in a dual inverter with two power units, named T(Top) and B(Bottom) inverter units, with two sets of three phase output terminals (abc and rst) which are connected in series and parallel.

The middle switch in each leg is shared by both inverter units. As can be seen in Fig.1, there are eight conceivable switching combinations for each leg of the nine-switch inverter, but only three of them are effective switching states, i.e., always one switch is open and the other two are closed. Dependent on the switching state, two different voltage levels can be imposed at each inverter output terminal. The valid switching states and the matching output voltages for the inverter leg 'ar' are described in Table 1.Focusing only on the inverter leg 'ar' and considering Table 1, it is potential to find that the switch Sj , where j = {a, b or c}, controls the output voltage *v*jo as follows:

$$Vjo = (2Sj - 1)\, Vdc/2, \qquad (1)$$

Where, Sj= 0 and Sj= 1 denotes switch open and closed, correspondingly. The duty cycle Dj of switch Sj in the top inverter unit can be firmed taking the average value of (1) over a switching period (Tsw),

$$Dj = 1/2 + (V^*jo\ /Vdc), \qquad (2)$$

where V*jo is the reference voltage enacted at the output terminal j, which is equal to Vjo(average value over Tsw).Likewise, observing Table 1, it is potential to note that the switch Sk, where k = {r, s or t}, controls the output voltage Vko through the following expression:

$$Vko = (1 - 2Sk)\, Vdc\ /\ 2, \qquad (3)$$

Where, Sk = 0 and Sk = 1 denotes switch open and closed, respectively. Taking the average value of (3) over Tsw, it is probable to find the duty cycle Dk of switch Sk as

$$Dk = 1/2 - V^*ko\ /Vdc\ , \qquad (4)$$

where V*ko is the reference voltage enacted at the output terminal k, which is equal to Vko(average value over Tsw).It can be noted that switches Sj and Sk in the same leg have contradictory behaviour : for example, while Vao is positive when S1= 1, Vro is positive when S2= 0, and vice-versa. For this reason, the duty cycle Dk presents an opposite sign when compared with Dj. Besides, in Table 1, it is potential to find that Vjo≥ Vko for all conceivable switching states. Since the average value over Tsw, it is found that Vjo≥ Vko and, therefore, the following inequalities should always be valued, for j and k in the same inverter leg:

$$V^*jo \geq V^*ko \Leftrightarrow Dj \geq 1 - Dk = Dk. \qquad (5)$$

Where Dk is the balancing duty cycle of Dk. Based on (5), it is difficult for the nine-switch inverter to produce two pure sinusoidal voltages at the outputs j and k,

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since at some point the sinusoidal voltage at terminal k would become larger than the one at terminal j. However, this constraint can be overwhelmed by scaling and shifting the duty cycle expressions of both inverter units, such that Dj≥ Dk, which confirms that the duty cycle spanning range of both inverter units are always disconnection. As significance, there is a natural drop of the modulation index range and a dc-link voltage allocation for both units. Nevertheless, as mentioned before, this is not an issue, since HPF applications require low level output voltages and, subsequently, low level dc-link voltages.

TABLE 1

Switching states and output voltages for inverter leg 'ar'.

SWITCHING STATE	S1	S12	S2	Vao	Vro
1	ON	ON	OFF	+*V*dc/2	+*V*dc/2
2	ON	OFF	ON	+*V*dc/2	-*V*dc/2
3	OFF	ON	ON	-*V*dc/2	-*V*dc/2

As the particular case where both inverter units sharing the dc link voltage in the same way, the duty cycles of the top unit switches should be scaled and shifted as follows:

$$Djtop = Dj/2 + 1/2, \quad (6)$$

Where, Djtop are the finale duty cycles of the top unit switches Sj.

Substituting (2) in (6), gives

$$Djtop = 3/4 + V^*jotop /Vdc , \quad (7)$$

Where $V^*jotop = V^*jo/2$, i.e., the extreme output voltage produced by the top inverter unit is half of the one produced by a VSI. Consistently, the corresponding duty cycles for the bottom unit switches are scaled as follows:

$$Dkbot = Dk /2, \quad (8)$$

Where, Dkbot are the final resultant duty cycles of the bottom unit switches Sk. Substituting (4) in (8) and considering Dk= 1 – Dk, yields

$$Dkbot = 1/4 + V^*kobot /Vdc, \quad (9)$$

Where, $V^*kobot = V^*ko/2$, henceforth the bottom inverter unit has the similar output voltage restraint of the top unit. Replacing
(7) and (9) in the restraint given by (5), gives

$$3/4\ V^*jotop/Vdc \geq 1/4 + V^*kobot/Vdc. \quad (10)$$

If the conditions $|V^*jotop| \leq Vdc/4$ and $|V^*kobot| \leq Vdc/4$ are valued, the inequality in (10) always holds exact. Hence, the duty cycles Djtop and Dkbot produce the reference voltages V*jotop and V*kobot, individually, respecting the nine-switch inverter limitations. It is significant to mention that (7) and (9) present simply the duty cycles for the bottom and top switches of the nine- switch inverter. Based on Table 1, the states of the mid switches are defined as the Special OR of the bottom and top switches states of the same inverter leg, i.e., Sjk= XOR(Sj, Sk).

IV.PASSIVE FILTERS DESIGN

The design features of the passive LC filters, i.e. the resonant frequency and quality issue, have an vital effect on the mitigation performance of the HPF. Usually, the filter inductance and capacitance are defined by the resulting general strategies:

1. The filter resonant frequency, $\omega res = 1/\sqrt{LFCF}$, is chosen nearby to the frequencies of main harmonic components to be mitigated. Thus, the passive filter only is able to somewhat absorb the anticipated harmonic components.

2.In order to assurance low impedance values for the harmonic components in the vicinity of the resonant frequency, the filter quality factor, QF = (1/RF)($\sqrt{LF/CF}$), where RF signifies the resistance of the inductor, has to be as small as possible. Since the value of RF should be low to decrease the losses in the HPF, the purpose is to decrease the ratio LF/CF.

3. In order to limit the reactive power delivered by the passive filter at the fundamental frequency, the filter capacitance should be constrained.

The core idea of the suggested topology is to tune the top unit passive filter at the 5th or 7th harmonic component, whereas the bottom passive filter tuned

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at the 11th or 13th harmonic component, subsequently those are the most shared harmonic components generated by nonlinear loads. Regrettably, the above strategies do not define which harmonic component should be selected for each filter. Besides, similar mitigation performance is attained for both choices. For this purpose, a modest and practical principle, described in [11], is accepted: the filter resonant frequency for the top unit is tuned around the 7th harmonic component, due to the statement that a LC filter tuned at the 7th harmonic is less huge and less costly than the one tuned at the 5th harmonic. Not with standing, the mitigation of the 5th harmonic component is not ignored, since it is attained by a proper feedforward control in the HPF. Using the same principle, the filter resonant frequency for the bottom unit is tuned around the 13th harmonic, whereas a feedforward control is used to increase the mitigation of the 11th harmonic component. These strategies can be used to design any dual HPF system.

V.SIMULATION RESULTS AND DISCUSSION

Electrical power systems are mixtures of electrical circuits and electromechanical devices like motors and generators. Engineers working in this discipline are regularly enlightening the performance of the systems. Requirements for significantly increased effectiveness have enforced power system designers to use power electronic devices and refined control system concepts that tax out-dated analysis tools and techniques. A common characteristic of these systems is their use of power electronics and control systems to attain their performance. The suggested control strategy is simulated in MATLAB /SIMULINK environment to check the performance of the control strategy in improving the system performance.

DVR

The main principle of the dynamic voltage restorer is to inject a voltage of essential magnitude and frequency, so that it can return the load side voltage to the wanted amplitude and waveform even when the source voltage is unstable or distorted. Normally, it works a gate turn off thyristor solid state power electronic switches in a pulse width modulated inverter structure. The DVR can generate or absorb individually controllable real and reactive power at the load side. In further words, the DVR is made of a switching power converter solid state DC to AC that injects a set of three phase AC output voltages in series and coordinate with the distribution and transmission line voltages.

The source of the injected voltage is the commutation process for an energy source for the real power demand and reactive power demand. The energy source may differ according to the design and maker of the DVR. Some samples of energy sources functional are DC capacitors, batteries and that drawn from the line through a rectifier.

In standard conditions, the dynamic voltage restorer operates in stand-by mode. Though, in disturbances, nominal system voltage will be compared to the voltage variation. This is to get the differential voltage that should be added by the DVR in order to sustain supply voltage to the load within limits.The amplitude and phase angle of the injected voltages are variable, thereby permitting control of the real and reactive power exchange between the DVR and the distribution system. The DC input terminal of a dynamic voltage restorer is connected to an energy storage device of suitable capacity.

As stated, the reactive power exchange between the dynamic voltage restorer and the distribution system is internally generated by the dynamic voltage restorer without AC passive reactive components. The real power exchanged at the DVR output AC terminal is provided by the DVR input DC terminals by an external energy source or energy storage system.

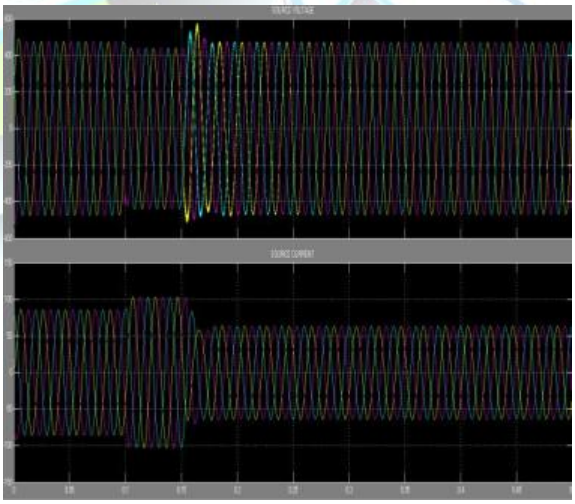

Fig.2 DVR- voltage and current showing mitigation of sag

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Static Synchronous Compensator (STATCOM)

Amongst the presented FACTS devices, the Unified Power Flow Controller (UPFC) is the most useful one that can be used to increase transient stability, steady state stability and dynamic stability .The UPFC is capable of both delivering and absorbing real and reactive power and it involves two ac/dc converters. One of the two converters is connected parallel with the line through a shunt transformer other in series with the transmission line through a series transformer. The dc side of the two converters is connected through a mutual capacitor, which offers dc voltage for the converter operation. The power balance between the series and shunt converters is a essential to sustain a constant voltage across the dc capacitor.

As the series branch of the UPFC injects a voltage of adjustable magnitude and phase angle, it can exchange real power with the transmission line and thus increases the power flow ability of the line as well as its transient stability limit. The shunt converter exchanges a current of governable magnitude and power factor angle with the power system. It is generally controlled to balance the real power absorbed from or injected into the power system by the series converter plus the loss by regulating the dc bus voltage at a anticipated value.

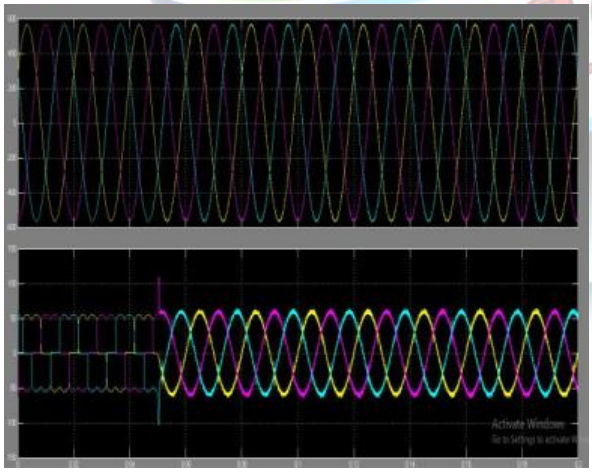

Fig. 3 D-STATCOM voltage and current showing mitigation of harmonics

UPQC

The establishment of both DVR and DSTATCOM can control the power quality of the load bus voltage and the source current. In adding, if the STATCOM and DVR are connected on the DC side, the DC bus voltage can be controlled by the shunt connected DSTATCOM while the DVR deliveries the required energy to the load in case of the transient disturbances in source voltage. The arrangement of such a device (termed as (UPQC) Unified Power Quality Conditioner). This is a adaptable device similar to a UPFC. Though, the control purposes of a UPQC are quite different from that of a UPFC.

The shunt connected converter has the following control objectives

1. To stable the source currents by injecting negative and zero sequence components required by the load
2. The required harmonic currents is injected to compensate for the harmonics in the load current
3. Injecting the required reactive current (at fundamental frequency) to control the power factor.
4. To regulate the DC bus voltage.

The series connected converter has the following control objectives:

1. To balance the voltages at the load bus by injecting negative and zero sequence voltages to compensate for those present in the source.
2. To separate the load bus from harmonics present in the source voltages, by injecting the harmonic voltages
3. To adjust the magnitude of the load bus voltage by injecting the required active and reactive components (at fundamental frequency) depending on the power factor on the source side
4. To regulate the power factor at the input port of the UPQC (where the source is connected. Note that the power factor at the output port of the UPQC (connected to the load) is controlled by the shunt converter.

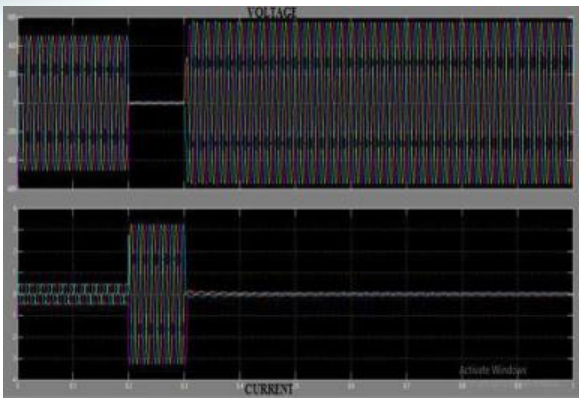

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Fig.4 UPQC – (Voltage and current) mitigation of sag and harmonics
Nine switch three leg (NSTL) INVERTER

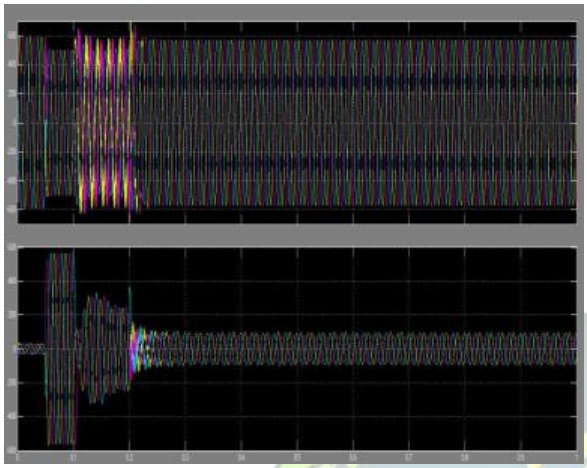

Fig.5 (voltage and current) mitigation of sag and harmonics

According to IEEE 519 standard the value of THD (Total Harmonic Distortion) value should be ≤ 5 %.By comparing the NSTL inverter with the Facts device we can know the performance of the implemented method. THD value determined by FFT analysis (Fast Fourier transform) in MATLAB simulation.

TABLE 2
Comparison of THD value of various device

DEVICE	BEFORE COMPENSATION (THD)	AFTER COMPENSATION (THD)
DVR	-	-
D-STATCOM	26.68%	3.69%
UPQC	26.68%	2.60%
NSTL INVERTER	26.68%	1.88%

From above table 2, Since the DVR is series compensation which concentrate on voltage injection in series to the line and does not compensate the current. So, it can mitigate sag and swell. Hence harmonics does not play a part in DVR FACTS device.

D-STATCOM is shunt compensation which concentrate on current injection in shunt to the line. Harmonics plays role in this device which can be mitigated.

The DVR and D-STATCOM are series and shunt compensation device which concentrates voltage and current separately. To overcome this disadvantage both are combined to get a device called UPQC.UPQC is both series and shunt compensation device concentrated on both voltage and current.So, it can be used to mitigate major power quality problems like sag, swell and harmonics which increases the performance of the system. Further improving the efficiency of the system is to reduce the cost, switching time, heat produce by the inverter. The UPQC contains two inverter part connected series and parallel having common DC-link.

The implemented NSTL inverter reduces the 12 switch inverter from the UPQC to 9 switch inverter having common DC-link which reduces the cost, switching time, heat and improve the efficiency that shown in the table 2. Christo Ananth et al.[5] discussed about E-plane and H-plane patterns which forms the basis of Microwave Engineering principles.

VI.HARDWARE SETUP

The hardware setup designed for this topic is shown in the figure below.

The hardware Setup consists of 4 parts:

1. Driver circuit
2. Inverter Circuit
3. Controller Unit
4. Power supply Unit

The Inverter component is given supply through a separate transformer while the driver circuit is power-driven by a group of 12V transformers.

The idea behindhand the hardware setup is that the three phase supply is rectified by a bridge rectifier and the ripples are removed using a capacitive filter circuit. The output of this operation is a single phase parameter.

This single phase output is given to the inverter component which over converts it to a three phase value. The inverter component is made up of nine MOSFET switches with each of pair correspond to a phase of the three phase of the output. The MOSFETs are triggered by the Driver circuit which consists of an Opto Isolator, transistors and

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MOSFET drivers. The Power MOSFET switch IRF840 is used. A Power MOSFET is a specific type of metal oxide semiconductor field effect transistor (MOSFET) designed to handle important power levels. Associated to the other power semiconductor devices (IGBT, Thyristor...), its main benefits are high. Commutation speed and good effectiveness at low voltages. It shares with the IGBT an isolated gate that makes it easy to drive.

Fig 6.Hardware Setup

1. Driver Circuit:

Mosfet driver TL250 like other MOSFET drivers have output stage and input stage. It also have power supply configuration. TLP250 is more suitable for MOSFET and IGBT. The main difference between TLP250 and other MOSFET drivers is that TLP250 MOSFET driver is optically out-of-the-way. Its mean input and output of TLP250 mosfet driver is out-of-the-way from each other. Its works like a opt coupler.

Input stage have a light emitting diode and output stage have photo diode. Every time input stage LED light falls on output stage photo detector diode, output befits high.16 pin IC. The opto receptor is connected between the 2nd and the 4th pin. The output to the MOSFET is taken from the 5th and the 7th pin.

2. Controller unit

PIC microcontroller was used in this scheme to obtain the gate signal of the inverter switches using SPWM. PIC 16F877A was used to produce the Modified Sine Wave gate signals and PIC 16F887 was used to produce Sine Wave gate signals. Both have 40 pins with dissimilar functions. Two PICs were programmed in order to drive switches for Modified Sine Wave and Sine Wave inverter. Program MPLAB was used to write the PICs codes.

MICROCONTROLLER SETUP FOR PWM OPERATION:

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 pre scale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation. 40- PIN DIP package.

Two Capture, Compare, PWM modules
Capture is 16-bit, max. resolution is 12.5 ns
Compare is 16-bit, max. resolution is 200 ns
Timer0: 8-bit timer/counter with 8-bit pre scaler
Timer1: 16-bit timer/counter with pre scaler, can be incremented during Sleep via external crystal/clock
Timer2: 8-bit timer/counter with 8-bit period register, pre scaler and post scaler

CCP1 Module:

Capture/Compare/PWM Register 1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. The special event triggers is produced by a compare match and will reset Timer1.

CCP2 Module:

Capture/Compare/PWM Register 2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. The special event trigger is produced by a compare match and will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

VII.HARDWARE RESULTS

Fig.6 Before sag ---- rms value 400v (230v single phase)

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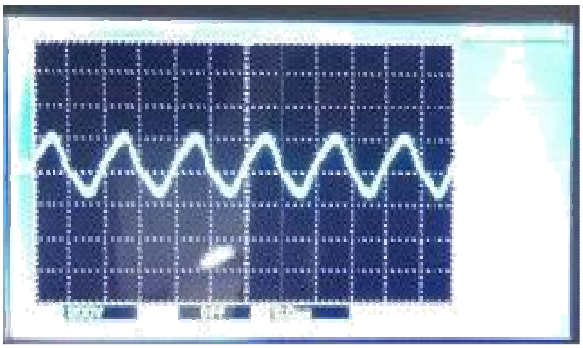
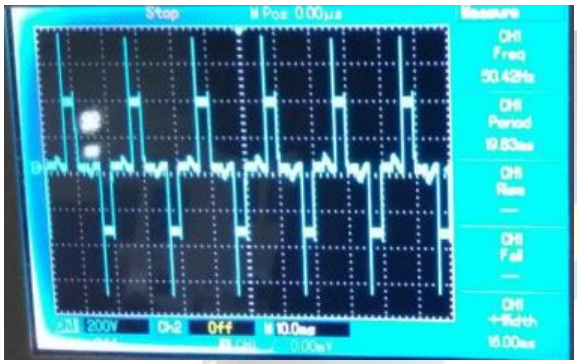


fig .7 During sag condition ---- rms value 200v (115v single phase)



Elimination of sag with some sorts of disturbance due to inverter switches mosfet 400v rms value

VIII.CONCLUSION

This proposes a transformerless HPF topology based on a novel NSTL inverter. The proposed inverter, which is divided in two units, is connected in series and parallel with two passive *LC* filters tuned in different harmonic frequencies of interest, aiming an enhancement in the harmonic mitigation performance with a less number of switches when compared with other dual topologies. A complete analysis of both inverter and passive filters, including the strategies necessary to design the HPF, was presented. Experimental tests were carried out, including the individual response of each inverter and the overall response of the proposed system, proving its feasibility. Proving that the NSTL inverter efficiency is better than compared FACTS devices.

REFERENCES

[1] R. C. Dugan, M. F. McGranagham, S. Santoso, and H. W. Beaty, Electrical Power Systems Quality, 2nd Ed. New York, NY, USA: McGraw-Hill, 2002.

[2] IEEE Recommended Practices and Requirements for Harmonic Control In Electrical Power Systems, IEEE STD 519-1992, 1993.

[3] H. Akagi, "Active harmonic filters," Proc. IEEE, vol. 93, no. 12, pp. 2128– 2141, Dec. 2005.

[4] R. Bojoi et al., "Current control strategy for power conditioners using sinusoidal Signal integrators in synchronous reference frame," IEEE Trans. Power Electron. vol. 20, no. 6, pp. 1402– 1412, Nov. 2005.

[5] Christo Ananth, S.Esakki Rajavel, S.Allwin Devaraj, M.Suresh Chinnathampy. "RF and Microwave Engineering (Microwave Engineering).", ACES Publishers, Tirunelveli, India, ISBN: 978-81-910-747-5-8, Volume 1,June 2014, pp:1-300.

[6] P. Kanjiya, V. Khadkikar, and H. H. Zeineldin, "A noniterative optimized Algorithm for shunt active power filter under distorted and unbalanced Supply voltages," IEEE Trans. Ind. Electron., vol. 60, no. 12, pp. 5376– 5390, Dec. 2013.

[7] Q. Liu et al., "A novel design and optimization method of an LCL filter For a shunt active power filter," IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 4000–4010, Aug. 2014.

[8] M. Angulo, D. A. Ruiz-Caballero, J. Lago, M. L. Heldwein, and S. A. Mussa, "Active power filter control strategy with implicit closedloop Current control and resonant controller," IEEE Trans. Ind. Electron. vol. 60, no. 7, pp. 2721–2730, Jul. 2013.

[9] M. Qasim, P. Kanjiya, and V. Khadkikar, "Artificial-neural-network based Phase-locking scheme for active power filters," IEEE Trans. Ind. Electron. vol. 61, no. 8, pp. 3857–3866, Aug. 2014.

[10] H. Hu, W. Shi, Y. Lu, and Y. Xing, "Design considerations for dsp controlled 400 Hz shunt active power filter in an aircraft power System," IEEE Trans. Ind. Electron., vol. 59, no. 9, pp. 3624–3634, Sep. 2012.

[11] G. Buticchi, L. Consolini, and E. Lorenzani, "Active filter for the removal of the dc current component for single-phase power lines," IEEE Trans. Ind. Electron, vol. 60, no. 10, pp. 4403– 4414, Oct. 2013.

[12] J. Liu, P. Zanchetta, M. Degano, and E. Lavopa, "Control design and Implementation for high performance shunt active filters in aircraft power grids," IEEE Trans. Ind. Electron., vol. 59, no. 9, pp. 3604–3603, Sep. 2012.

[13] Y. Tang et al., "Generalized design of high performance shunt active Power filter with output LCL filter," IEEE Trans. Ind. Electron., vol. 59, No. 3, pp. 1443– 1452, Mar. 2012.

[14] H. Fujita and H. Akagi, "A new approach to harmonic compensation in Power systems—a combined system of shunt passive and series active filters," IEEE Trans. Ind. Appl., vol. 26, no. 6, pp. 983–990, Nov./Dec. 1990.

[15] D. Detjen, J. Jacobs, R. W. De Doncker, and H. G. Mall, "A new hybrid

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Filter to dampen resonances and compensate harmonic currents in industrial
Power systems with power factor correction equipment," IEEE Trans. Power Electron. vol. 16, no. 6, pp. 821– 827, Nov. 2001.

[16] A. Luo et al., "A novel three-phase hybrid active power filter with a series Resonance circuit tuned at the fundamental frequency," IEEE Trans. Ind.
Electron. vol. 56, no. 7, pp. 2431–2440, Jul. 2009.

[17] A. Luo, Z. Shuai, Z. J. Shen, W. Zhu, and X. Xu, "Design considerations
For maintaining DC-side voltage of hybrid active power filter with
Injection circuit," IEEE Trans. Power Electron., vol. 24, no. 1, pp. 75–84,
Jan. 2009.

[18] H. Akagi, E. Watanabe, and M. Aredes, Instantaneous Power Theory and Applications to Power

[19] F. Z. Peng, "Harmonic sources and filtering approaches," IEEE Ind. Appl. Mag., vol. 7, no. 4, pp. 18–25, Jul. /Aug. 2001.

[20] A. Luo, Z. Shuai, W. Zhu, Z. J. Shen, and C. Tu, "Design and application of a hybrid active power filter with injection circuit," IET Power Electron.,
vol. 3, no. 1, pp. 54–64, Jan. 2010.

[21] Z. Shuai, A. Luo, W. Zhu, R. Fan, and K. Zhou, "Study on a novel hybrid
Active power filter applied to a high-voltage grid," IEEE Trans. Power
Del., vol. 24, no. 4, pp. 2344–2352, Oct. 2009.

[22] A. Luo, Z. Shuai, W. Zhu, R. Fan, and
C. Tu, "Development of hybrid
Active power filter based on the adaptive fuzzy dividing frequency-control method," IEEE Trans. Power Del., vol. 24, no. 1, pp. 424–432, Jan. 2009.

[23] S. Srianthumrong and H. Akagi, "A medium-voltage transformerless
AC/DC power conversion system consisting of a diode rectifier and a shunt hybrid filter," IEEE Trans. Ind. Appl., vol. 39, no. 3, pp. 874–882, May/Jun. 2003.

[24] J.-C. Wu et al., "Novel circuit topology for three-phase active power Filter," IEEE Trans. Power Del., vol. 22, no. 1, pp. 444–449, Jan. 2007.

[25] A. Bhattacharya, C. Chakraborty, and S. Bhattacharya, "Parallel connected Shunt hybrid active power filters operating at different switching frequencies for improved performance,"
IEEE Trans. Ind. Electron.
vol. 59, no. 11, pp. 4007–4019, Nov. 2012.

[26] L. Asiminoaei, C. Lascu, F.
Blaabjerg, and I. Boldea, "Performance improvement of shunt active power filter with dual parallel topology," IEEE Trans. Power Electron. vol. 22, no. 1, pp. 247–259, Jan. 2007.

[27] C. Liu, B. Wu, N. R. Zargari, D. Xu, and J. Wang, "A novel three phase three-leg AC/AC converter using nine IGBTs," IEEE Trans. Power
Electron., vol. 24, no. 5, pp. 1151–1160, May 2009.

[28] L. Zhang, P. C. Loh, and F. Gao, "An integrated nine-switch power conditioner for power quality enhancement and voltage sag mitigation," IEEE
Trans. Power Electron., vol. 27, no. 3, pp. 1177–1190, Mar. 2012.

[29] W. Tangtheerajaroon wong, T.
Hatada, K. Wada, and H. Akagi, "Design and performance of a transformerless shunt hybrid filter integrated into a Three-phase diode rectifier," IEEE Trans. Power Electron., vol. 22, no. 5, pp. 1882–1889, Sep. 2007.