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DESIGN OF STATE RETENTION USING CLOCK GATED VERIFICATION

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***Abstract*— The idea of reducing the area and power consumption in low power VLSI design is considered here for discussion. A new selective approach for State Retention Clock Gating (SPCG) based on Module checking verification techniques is, so it is called as Selective SRCG (SSRCG).In this proposed approach, Retention registers are special low leakage flip-flops used to hold the data of main register of the clock gated block. Thus internal state of the block during power down mode can be retained and loaded back to it when the block is reactivated .Clock gating logic enables AND gate when the clock signal along with the enable signal is given, provides the clock gated output.CG also reduces SKEW.**

Index terms—Formal verification, Low power design,Cllock gating, State retntion,Skew

I. INTRODUCTION

A variety of techniques are used to reduce the power consumption. Power gating method is used to reduce the Static Power Consumption. In PG the power supply I s disconnected, during Stand-by mode. It gave the Higher Efficiency. However this leads to complete loss of the system, which is the main disadvantage of the PG approach.

To overcome that SRPG (State Retention Power Gating) was developed. This SRPG technique uses special low leakage state retention memory cells are connected to each Flip-flop to retain their values during Stand-by mode. The main disadvantage of the SRPG approach is Area overhead, when compared to PG.

Then SSRPG (Selective State Retention Power Gating) method was developed. This approach is only developed for reducing the total number of required retention cellsAffects the design architecture. Increases the time delay.Difficult to present the flip-flop equations in a BDD representation. Area overhead. Power consumption is increased.

An advanced Selective State Retention Clock Gating approach aims at reducing the number of required of retention flip-flops, the low leakage flip-flop used as a retention registers for holding the data. Here the Clock gating logic is used instead using Multiplexers.

A. Selective state retention power gating based on gate level analysis

This work presents a novel approach based o Gate level analysis for implementing selective state retention power gating (SPRG).a selective SPRG approach mitigates the area and power overhead of the conventional SPRG approach were published. To implement the new approach, an automatic algorithm, which is performed on a gate-level net list has been developed .this algorithm enables the extraction of a subset of flip-flops is sufficient for a proper state retention power gating. Unique selective SPRG criteria have been defined to support the proposal algorithm. These criteria are used to reduce the total amount of required retention flip-flops.

B. Selective state retention power gating based on formal verification

In this paper new selective SPRG based on module checking formal verification techniques was presented which follows unique criteria for automatically selecting the reduced set of retention flip-flops. This criteria are represented as a set of

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formal properties using propositionals formulas to analyze the flip-flops input equations. Those properties are expressed in temporal logic formalisim, specifically, in computation tree logic (CTL).the extraction of the essential flip flops is carried out using common formal verification techniques.

C. Asub wakeup time power gatingtechnique with bypass powerline for rush curren support

For low-power SOCs ,we developed a sub-wakeup time power gating technique, which uses a bypass line separated from the main power line .bypass switches connected to the bypass power line are controlles using a dedicated sequence. The area overhead of the bypass resource was less than1% of the total die area the supply voltage fluctuation was reduced by 87.5%.the technique enabled a 240ns wake-up time on a 2M gate circuit with a supply voltage fluctuation of only 2.5mV. [4] discussed about a system, a low power area reduced and speed improved serial type daisy chain memory register also known as shift Register is proposed by using modified clock generator circuit and SSASPL (Static differential Sense Amplifier based Shared Pulsed Latch). This latch based shift register consumes low area and low power than other latches. There is a modified complementary pass logic based 4 bit clock pulse generator with low power and low area is proposed that generates small clock pulses with small pulse width. These pulses are given to the conventional shift register that results high speed.

II. STATE RETENTION USING CLOCK GATED VERIFICATION

In the SSRCG system, we are designing the state retention using clock gated verification method. Retention registers are special low leakage flip-flops used to hold the data of main register of the clock gated block. Thus internal state of the block during power down mode can be retained and loaded back to it when the block is reactivated. Clock gating is the low power saving technique in use for a long time. In this it gates the clock signals with the enable signal thus providing clock gated output. Here, the latch based clock gating logic is typically used to avoid any glitches even during entry and exit from/to sleep mode. The validity of the enable signal at wakeup, which is typically provided by the restored states in the registers propagating through cloud of logic to the clock gating latches. It uses some kind of state retention during the clock gating latches, which retains the internal state of block when powered down. Clock tree consume more than 50 % of dynamic power. It is also used to reduce the complex in BDD representation, which leads to the circuitry is simple. This is the main advantage of the SSRCG approach.

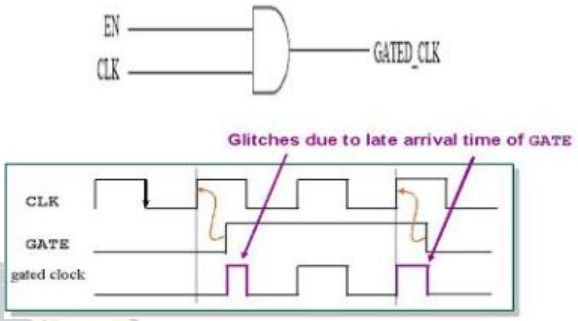

Fig 1: Clock gated method

III System Model

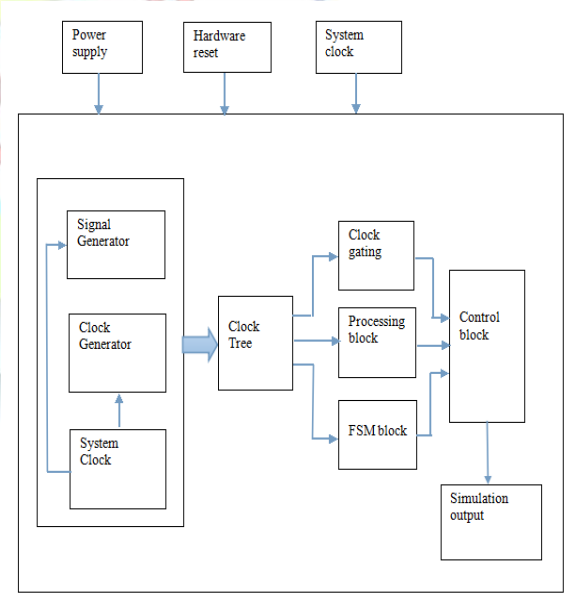

Fig 2: Block Diagram of Clock gate Verification

The components of this power are:

1) Power consumed by combinatorial logic whose values are changing on each clock edge

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2) Power consumed by flip-flops and 3) The power consumed by the clock buffer tree in the design.

It is good design idea to turn off the clock when it is not needed. Automatic clock gating is supported by modern EDA tools. They identify the circuits where clock gating can be inserted. RTL clock gating works by identifying groups of flip-flops which share a common enable control signal. Traditional methodologies use this enable term to control the select on a multiplexer connected to the D port of the flip-flop or to control the clock enable pin on a flip-flop with clock enable capabilities. RTL clock gating uses this enable signal to control a clock gating circuit which is connected to the clock ports of all of the flip-flops with the common enable term. Therefore, if a bank of flip-flops which share a common enable term have RTL clock gating implemented, the flip-flops will consume zero dynamic power as long as this enable signal is false.

A.HARDWARE
FPGA

FPGA provide the next generation in the programmable logic devices. The word Field in the name refers to the ability of the gate arrays to be programmed for a specific function by the user instead of by the manufacturer of the device. The word Array is used to indicate a series of columns and rows of gates that can be programmed by the end user.
As compared to standard gate arrays, the field programmable gate arrays are larger devices. The basic cell structure for FPGA is somewhat complicated than the basic cell structure of standard gate array. Increase system performance with efficient, dual-register 6-input LUT (look-up-table) logic structure Implement PCI Express with integrated endpoint blocks. Get connected with up to 8 low power (150 mW per) 3.2Gbps GTP serial transceivers. Support access rates of up to 800Mbps using integrated memory controllers. Build DSP applications using low-power 390MHz DSP48A1
Use multi-voltage, multi-standard Select IO banks with low cost HSTL and SSTL memory interfaces. Clock management tiles, each consisting of 2 DCMs and 1 PLL.1000MHz clocking

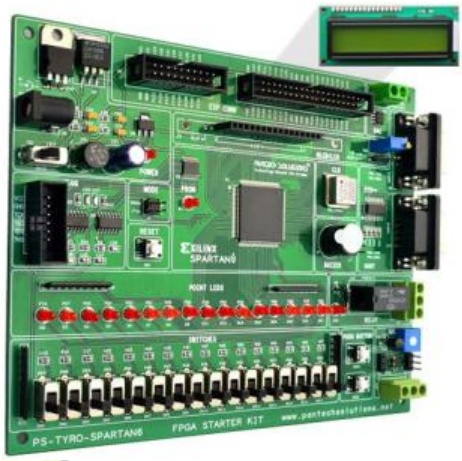

Fig 3: FPGA Kit

IV METHOD OF IMPLEMENTATION

This mealy model is the output is depends on both the present input and past output.MEALY model leads to reduction in number of states but is complicated whwn compare to MOOREE.MEALY is faster because output will change as soon as input changes but it leads to asynchoronous outputs leading to metastability.

MEALY state retention method is used.

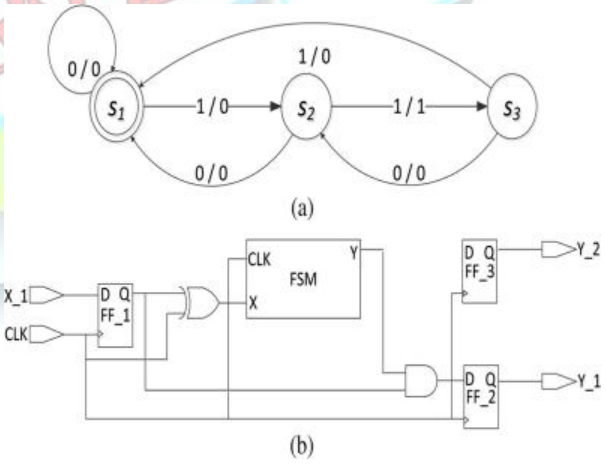

Fig 4: Pulse detection circuit-A simple design example (a) State transition diagram (b) Block diagram

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V Results & Discussion

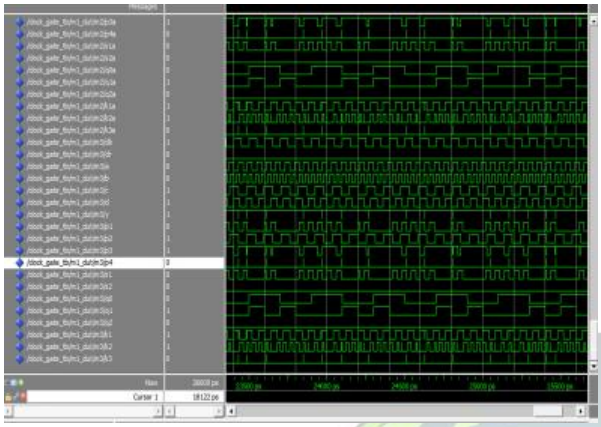

Fig 5: Simulated Output

We have presented the simulated result for SPRCG using **modelsim software** as shown in fig 5. In this simulation practical implementation and the performance of SPRCG is obtained. In this simulation power consumption is clearly obtained. From this simulation we can clearly understand that the SKEW also reduced.

VI CONCLUSION

Thus the power consumption is achieved. The number of retention flip-flops are reduced so that power consumption, skew is reduced which is observed from the practical implementation by using Xilinx ISE 10.1.

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