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Active Power Factor Correction Based Improved Power Quality Switched Mode Power Supply

Priyanka M. J.
M.Tech, Power System & Control
Govt. Engineering College, Barton Hill, Thiruvananthapuram
Kerala, India

Remya Mol N.
Assistant Professor
Govt. Engineering College, Barton Hill, Thiruvananthapuram,
Kerala, India

Lekshmi Sree
Lecturer
Govt. Engineering College, Barton Hill, Thiruvananthapuram,
Kerala, India

***Abstract*—In this paper active power factor correction technique based on modified zeta converter is proposed for power quality improvement in switched mode power supply (SMPS). The conventional AC-DC converters without power factor correction (PFC) has low power factor and high total harmonic distortion (THD). Using PFC at the front end of a SMPS, the disadvantages of conventional SMPS are overcome and the power quality indices are brought in line with the standards set by international standards such as IEC 61000-3-2. In the proposed system, to improve the power quality a PFC bridgeless zeta converter operating in discontinuous mode is presented. In addition to improving the power quality parameters the proposed system eliminates the use of diode bridge rectifier (DBR) present in conventional system and thereby reduce conduction losses and improve efficiency. It provides a regulated voltage at the output which is fed to an isolated converter to produce multiple low voltage dc outputs. The performance of the system is evaluated for varying input voltages in MATLAB/Simulink.**

***Index Terms*— PFC, THD, zeta converter**

I. INTRODUCTION

In conventional single-phase AC–DC rectification the analysis shows that [1] the input line current is pulsating and nonsinusoidal. This implies high harmonic contents and a low power factor. The former produces electromagnetic interferences and the latter gives rise to low-power transfer efficiency. It is therefore imperative to reshape, by some means, the input current such that not only is it in phase with the rectified source voltage but also sinusoidal in its time-domain profile with low harmonic distortion. That is the essence of power-factor correction, (PFC).

To meet the limits on power quality set by various international standards such as International Electrotechnical Commmission (IEC) 61000-3-2 [2-3], efforts are made to develop power factor corrected converters (PFC). An ideal PFC converter must emulate a resistor when seen from the supply side besides maintaining a fairly regulated output voltage. The improvement in power quality can be observed from the improved power factor and lowered THD even at varying input voltage conditions and fluctuating loads. PFC converters can be classified as passive and active. In the old days, the objective was met by passive means, adding huge capacitor banks to the AC line. In contrast, modern techniques approach it through active means, employing a switch-mode converter and forcing line current to match the line voltage. In this paper active PFC converter employed SMPS are given attention.

Among the three basic topologies-buck, boost and buckboost; only the boost and the buckboost are suitable for PFC applications. The buck (step-down) configuration is excluded because of the limited output range [4]. Similarly when a wide input voltage range is to be taken care of boost converter cannot be used as boost converter can function properly only when output is greater than input. In the case of a buck-boost converter above said limitations do not pose any problem as it can step up and step down voltages. However the polarity at the output is reversed which give rise to various design issues. To eliminate the above mentioned issues zeta converter, a fourth order dc-dc converter is proposed in literature [6]. Zeta converter can provide continuous output current with a low ripple output voltage which is highly recommendable for applications like PC's. In the systems described so far DBR is used before the PFC converter, which increases the conduction losses and can degrade efficiency. So researches are ongoing with

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bridgeless topologies based SMPS.

In this paper bridgeless zeta converter is proposed as a candidate for power quality improvement. This paper compares the conventional zeta converter and bridgeless zeta converter. The converters are designed and simulated in MATLAB/Simulink platform to validate the design.

The organization of the paper is as follows. Section II deals with the conventional zeta converter based AC-DC converter. Proposed bridgeless zeta PFC is given in section III. The design procedure is detailed in section IV. Simulation results of conventional zeta and bridgeless zeta configurations are given in section V. Section VI compares the performance of the conventional and proposed system. Section VII concludes the paper.

II. Conventional PFC Zeta Converter Based SMPS

Fig. 1. represents the SMPS topology based on PFC zeta converter. The configuration consists of a DBR with filter connected to non-isolated zeta converter. Zeta converter has two inductors –input inductor Lz1 and output inductor Lz2, intermediate capacitor C1, one high frequency switch S and one diode D.

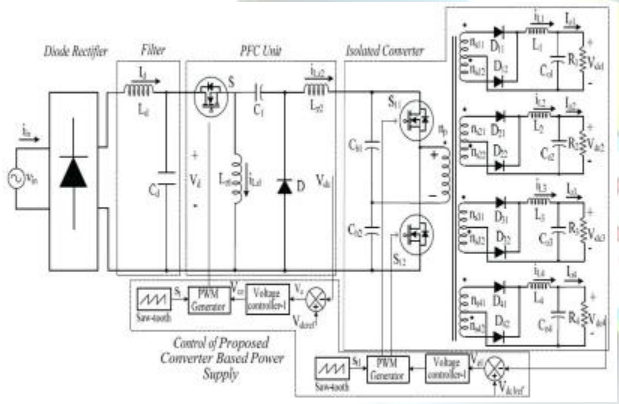

Fig. 1. PFC zeta converter based SMPS

By employing discontinuous conduction mode (DCM) operation the control is made simple. In DCM operation the key waveforms are illustrated in Fig. 2. DCM has inherent power factor correction capability [7] and hence no additional sensors are required to provide the reference signal to force the input current to follow input voltage**.** The DCM working PFC converter draws input current at unity power factor without any additional control and also regulates the output dc voltage. A PI voltage controller is used for regulating the output voltage of the PFC. The regulated dc voltage is fed to the isolated converter which is a half bridge converter here. Half bridge converter is selected on the basis of power handling capacity [8]. The isolated converter consists of two capacitors C_{h1} and C_{h2}, two switches, one high frequency transformer (HFT) and filters for multiple secondary outputs. The output voltages are regulated using PI controller based control. Only one of the output voltage is sensed and the other outputs are controlled by the duty cycle of isolated converter. The isolated converter operates in continuous conduction mode (CCM) to reduce current stress.

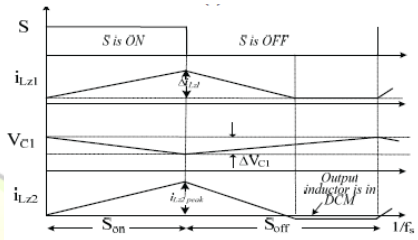

Fig. 2. Waveforms of various components in one switching cycle

III. Bridgeless PFC Zeta Converter Based SMPS

The distinguishing characteristic of a bridgeless PFC converter is that it eliminates the need for a diode bridge at the input. This reduces power losses that normally occur in a diode bridge and, as a result, improves overall system efficiency. By operating the stages alternatively during the positive and negative half cycles of the AC mains voltage, the proposed bridgeless system implements both the AC-to-DC rectification as well as power factor control.

The bridgeless converter proposed here is represented in Fig. 3. It has two sets of zeta converter-upper one for operation during positive half and the lower one for operation during negative half of AC mains.

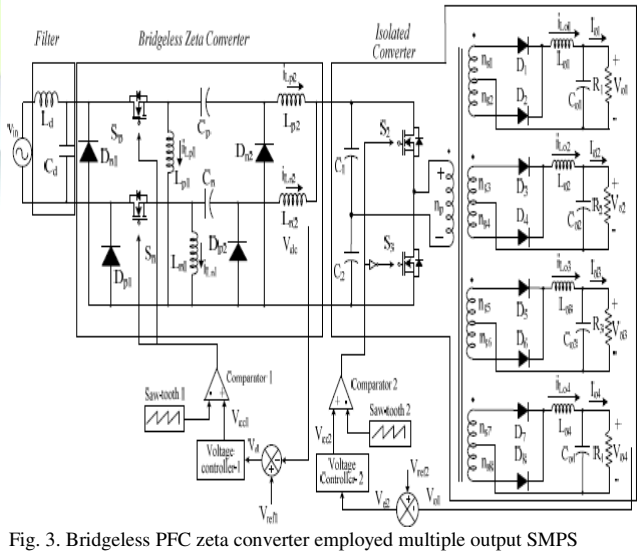

Fig. 3. Bridgeless PFC zeta converter employed multiple output SMPS

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The upper set converter consists of one high frequency switch Sp which is operated at 20kHz, two inductors-Lp1 and Lp2, one intermediate capacitor Cp. Similarly, the lower set has the same number of components as the upper one and are represented using the suffix 'n' to denote their working during the negative half of supply. The positive and negative half cycle operated zeta converter is demonstrated in Fig. 4.

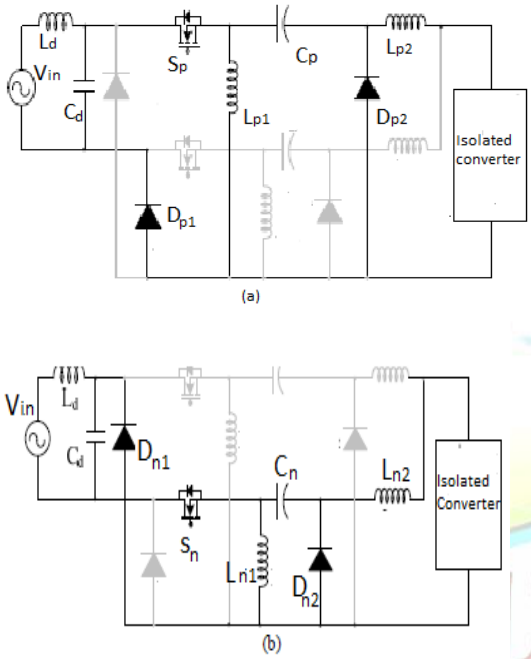

Fig. 4. (a)Positive half cycle operated zeta converter and (b) negative half cycle operated zeta converter

During each switching cycle, the zeta converter operates in three modes. The three modes for the positive half operation are explained below:

A. Mode 1

In the first mode switch Sp turns on and current flows through two paths-through Lp1 and through Cp-Lp2-load. During this mode the inductor charges linearly and capacitor Cp discharges. This mode is called inductor charging mode.

B. Mode 2

In the second mode called inductor discharging mode, the switch Sp turns off and the inductors start discharging through diode Dp2. The inductor Lp2 is designed to operate in DCM mode and hence discharges to zero.

C. Mode 3

In the last mode the inductor currents remain constant till the next switching cycle begins.

The same happens with the lower set zeta converter during negative half operation of AC mains voltage.

The PFC also regulates the output voltage but with appreciable ripple. As post regulator stage using an isolated DC-DC converter is present tight regulation is not a concern. Here a half bridge converter is used as isolated converter. Since the topology is half bridge the dc link capacitor is constituted by two capacitors of equal values connected in series. The half bridge converter has two high frequency switches, one high frequency transformer and four secondary winding with filters. Christo Ananth et al.[5] presented a brief outline on Electronic Devices and Circuits which forms the basis of the Clampers and Diodes.

The control implemented is PI voltage controller based pulse width modulated (PWM) control. The highest rating DC output is sensed and is compared with the reference voltage. The error so produced is fed to a voltage controller which is then compared with a saw tooth waveform of high frequency. The frequency of the saw tooth wave determines the switching frequency. The resulting PWM pulses controls the duty ratio of the two switches. The two switches should conduct alternatively and it should be ensured that sufficient dead time is provided to avoid shoot through.

IV. DESIGN

The design of the bridgeless PFC zeta converter is carried out in this section. The system is designed to deliver 350 W. The zeta converter volt-sec balance will give the relation between input and output voltage as given in (1)

$$\frac{V_{dc}}{V_{in}} = \frac{D}{1-D} \tag{1}$$

Therefore the duty cycle can be expressed as

$$D = \frac{V_{dc}}{[V_{in} + V_{dc}]} \tag{2}$$

where V_{dc} is the dc link voltage or output of PFC converter which is regulated to 300V with 100 Hz frequency ripples. These ripples cannot be completely eliminated without distorting the input current. The PFC is designed for operation in varying input voltage range 170V -270V. The switching frequency is selected as 20kHz. The input and output inductor can be designed using the following

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equations:

$$L_{p1} = L_{n1} = \frac{D.T.V_{in}}{\Delta i_{in}} = \frac{V_{in}.T.V_{dc}}{\Delta i_{in}[V_{dc} + V_{in}]} \quad (3)$$

$$L_{p2} = L_{n2} = \frac{(1-D)T.V_{dc}}{2I_{dc}} = \frac{V_{dc}DT}{2I_{in}} = \frac{R_{in}V_{dc}DT}{2V_{in}} = \frac{V_d^2 TV_{dc}}{2V_{in}P_{in}}\frac{[V_{dc}]}{[V_{dc}+V_{in}]} \quad (4)$$

where I_{dc} is the dc link current. The input inductor value is selected as 5mH to ensure continuous conduction mode operation (CCM) during varying input voltages and the output inductor is selected as 0.7mH to ensure DCM operation during the varying input condition. The intermediate capacitor value is selected as 470nF.The dc link capacitor value is obtained as 660µF.

The half bridge converter provides regulated multiple DC outputs- 12V/12.5A,5V/23A,3.3V/16A, and 12V/0.8A.The secondary windings has filtering circuits consisting of an inductor and a capacitor to produce smooth DC outputs. The design for the filter inductor of one secondary winding is as given

$$L_{01} = \frac{V_{o1}(0.5-D)T}{\Delta i_{L1}} \quad (5)$$

V. SIMULATION RESULTS

The conventional zeta converter and the proposed bridgeless zeta converter is simulated in MATLAB and its simulink model is shown in Fig. 5. and Fig. 6. respectively. The conditions of DCM and CCM operation of the conventional and proposed system are ensured using the simulation results shown in Fig. 7.In both cases the input voltage and input current are sinusoidal and in phase conforming unity power factor as shown in Fig. 8. The multiple dc outputs obtained at the half bridge converter secondary is shown in Fig. 9. THD below 4% is obtained from the simulation and is shown in Fig. 10

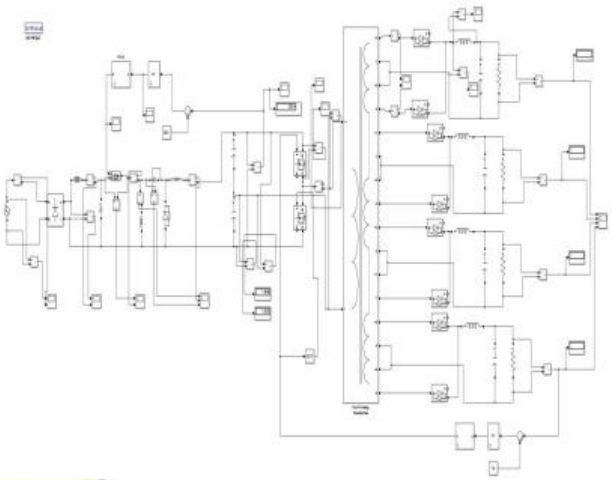

Fig. 5. Simulink model of PFC zeta converter based SMPS

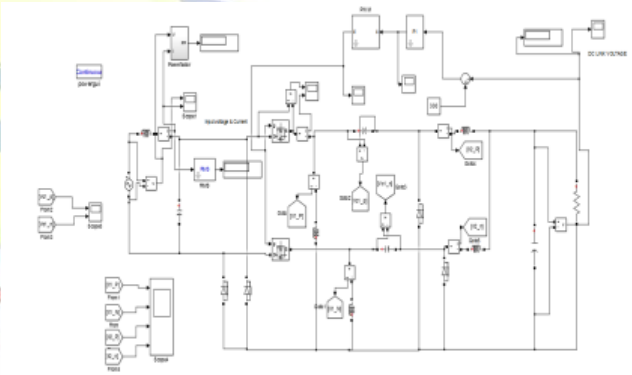

Fig. 6. Simulink model of bridgeless PFC zeta converter

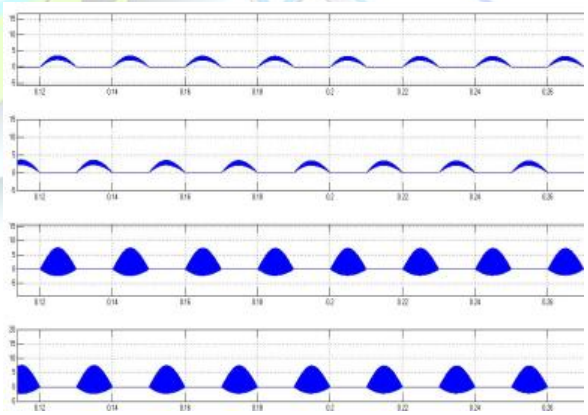

Fig. 7. Simulation of bridgeless zeta converter showing CCM and DCM operation of input inductor and output inductor

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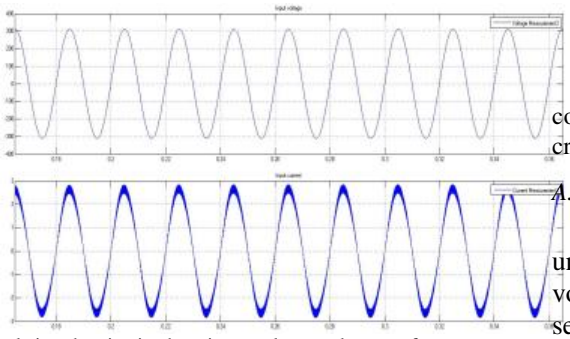

Fig. 8. Simulation showing in phase input voltage and current for bridgeless PFC zeta converter based SMPS

MODE	Voltage (V)	THD (%)	DPF (Kd)	DF (Kp)	PF
L2 in DCM	260	3.92	0.9992	1	0.9992
	220	3.63	0.9993	1	0.9993
	170	3.28	0.9995	1	0.9995

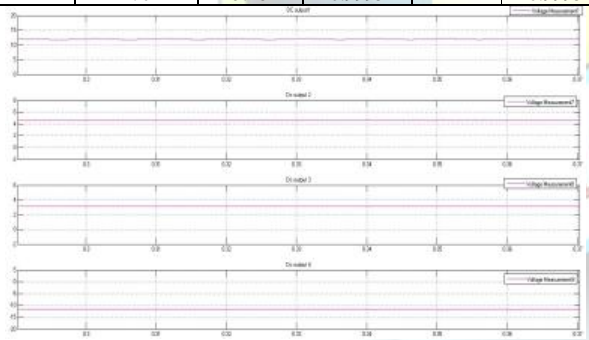

Fig. 9.Regulated multiple dc outputs of half bridge converter

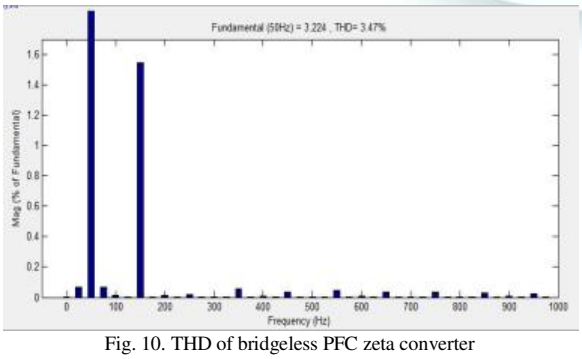

Fig. 10. THD of bridgeless PFC zeta converter

VI. Comparison Between Conventional PFC Zeta and Bridgeless PFC Zeta Converter.

The comparison between the proposed system and conventional PFC zeta is made under the following criterions:

A. Performance under varying input condition

The proposed system was designed for operation under varying input voltage conditions. The minimum voltage was selected as 170V and maximum voltage selected was 270V.The analysis of simulation results shows that the performance of proposed system and conventional system satisfies the international standards for power quality parameters. In that bridgeless shows slightly lower distortion of input current when compared to conventional system for the different input voltages selected. The observations are tabulated separately for proposed system in Table I and conventional system based on zeta converter in Table II.

TABLE I
Performance of bridgeless zeta converter under varying input voltage

MODE	Voltage (V)	THD (%)	DPF (Kd)	DF (Kp)	PF
L2 in DCM	260	3.70%	0.9993	1	0.9993
	220	3.48%	0.9994	1	0.9994
	170	3.17%	0.9995	1	0.9995

Table II
Performance of conventional zeta converter under varying input voltage

B. Component Count

The component count was more in bridgeless zeta as two sets of conventional zeta converter constitutes the bridgeless zeta..But the number of components conducting during each mode was less for bridgeless due to elimination of diode bridge. The number of components used in both systems are tabulated in Table III.

TABLE III
Number of components used by each system

Component	Bridgeless PFC Zeta	Conventional PFC Zeta
Switch	2	1
Diode	4	5
Inductor	4	2
Capacitor	2	1

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The number of inductors used is more which is a disadvantage but it can be overcome by using coupled inductors.

C. *Efficiency*

The efficiency was slightly greater for bridgeless due to reduced conduction losses through the elimination of diode bridge. But when compared with conventional SMPS both the conventional zeta and bridgeless zeta had lower efficiency.

VII. CONCLUSION

A bridgeless PFC zeta converter was designed, simulated and analysed in this paper. The simulation results of the system showed THD below 5% in the input voltage range selected for analysis. The power factor obtained is 0.999.Hence the system conforms to standards set by IEEE and IEC. The system is capable to mitigate the power quality issues caused by a conventional SMPS.

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