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Single Stage Boosting Inverter with High DC Gain

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***Abstract*—This paper proposes a single stage microinverter for PV applications. In the proposed scheme a coupled inductor is used in the boosting stage, which enables obtaining high dc gain . Increased value of dc link voltage help in reduction of dc link capacitance and increase life of inverter. Simulation of the proposed scheme using PWM technique was done and results were obtained. Results show high input boosting, good DC-AC decoupling, low THD output waveform.**

***Index Terms*—microinverter**

I. INTRODUCTION

Due to increased use of fossil fuels for energy production its amount is decreasing day by day, Hence we have to switch to the usage of renewable sources .Of the available renewables PV is gaining more importance .With its growth single stage microinverter topologies are becoming an interest area. Microinverter topologies are of the single-stage, the two-stage and the multi-stage types[1]. The multi-stage micro-inverters are usually comprised of a step-up DC-DC converter front stage with Maximum Power Point Tracking control, an intermediate high frequency DC-DC converter stage, used to attain a rectified-sine waveform, and a low frequency unfolding stage to interconnect to the grid . But the multi-stage topology with associated high component count results in a costly product . The two-stage micro-inverter can be designed cascading a MPPT controlled step-up DC-DC converter and a grid tied high frequency inverter.The single-stage topology performs the voltage step-up, the MPP tracking, and the DC-AC inversion functions all in one stage.

Two major problems associated with single stage topology is low dc-dc gain and large decoupling capacitance value. The value of the decoupling capacitor depends on the rated power, P_{dc}, the line frequency, f, the average voltage across the capacitor, V_{dc}, and the allowed peak-to-peak ripple, $\triangle v$,

$$Cdc = \frac{Pdc}{2\Pi fVdc\Delta v} \qquad (1)$$

The two-stage or the multi-stage micro-inverters decoupling capacitor is placed on the high voltage DC link, and, according to (1), helps in attaining lower value of the decoupling capacitor [2].Some single stage micro-inverters may require placing the decoupling capacitor at the PV module terminals. The low panel voltage, V_{dc}, and the desired low ripple, $\triangle v$, see (1), result in an increased decoupling capacitor value and size . Large electrolytic capacitors have short life and effects system's reliability. Therefore, the power decoupling problem becomes one of major concerns in micro-inverter design. Application of small non electrolytic capacitors is strongly desired.

In [3], a dual boost inverter was suggested. Here the load is connected differentially between the outputs of two bidirectional boost converters, The demerits of this approach are the limited DC step-up gain; circulating currents, which impair the efficiency; and somewhat complicated control. Another single stage solution [5] . Compared to [3] the topologies in [5] use a single boost inductor; have no circulating currents; have a high voltage DC link and, accordingly, a smaller decoupling capacitor. Also, traditional control methods can be applied. Moreover, the topologies proposed in [6], [7] may provide other choices for single stage solutions. However, the limited DC step-up of [3]-[7] necessitates using a more expensive high voltage PV panels with 70-100VDC output in order to get the desired dc bus voltage compatible to grid connected inverters. Alternatively, using the popular crystalline silicon modules with the 25-50VDC MPP range, these topologies can implement a two-three panel string inverter, which, as any string architecture, is prone to the mismatch problem

In this paper a Single-Stage Inverter is proposed for alternative energy/solar power generation. SSI can be regarded as further improvement of [5]. SSI can attain higher DC gain and, thus, operate off low DC input voltage of a single PV panel. Its switching pattern is so developed that DC-dc and DC-AC

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conversion occurs in a single stage. The power decoupling is performed at high voltage, thus, low value of DC link decoupling capacitor is required. PWM based control technique is used. The paper presents theoretical analysis, simulation results were obtained

II. PROPOSED TOPOLOGY

The prosed topology is as shown in Fig.1. SSI is comprised of MOSFET switches M1-M4, arranged in a full bridge configuration; steering diodes D1,D2; DC link diode D3, the tapped inductor W1:W2; the decoupling capacitor Cdc; and the output filter Lo-Co. The load is represented by the resistor RL. The proposed SSBI is fed by a DC voltage source, Vg, considered to be derived of a single PV panel, and generates utility level AC output voltage Vo. Here, the input current is designated as ig, the output current is io and its average component is Io. Compared to[3], the proposed SSBI topology has the advantages of a larger voltage step-up which can be achieved adjusting the tapped inductor turns ratio, and smaller decoupling capacitor, which is placed on high voltage dc bus.

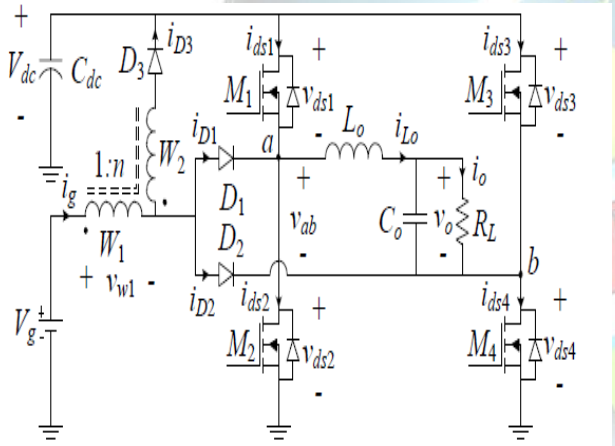

Fig. 1. Topology of proposed single stage inverter

For producing output of positive polarity 3 switching states are created as follows, here boost and buck sub-topologies can be seen.

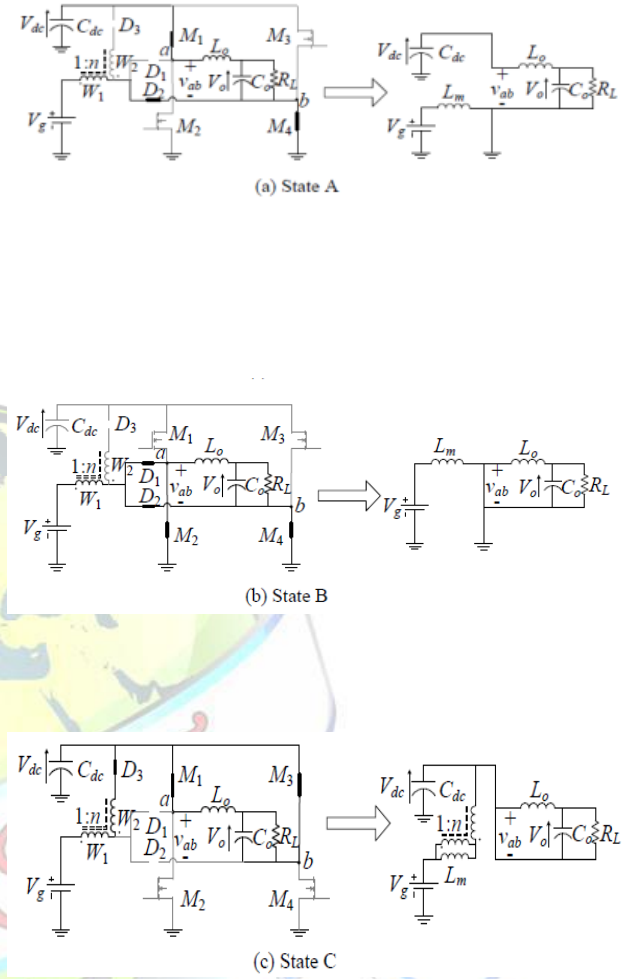

Fig. 2. States of operation and equivalent circuits.

State A

Lasts for a duration of t_a. Here, the switches M_1 and M_4 are on, whereas switches M_2 and M_3 are off, D_2 conducts and D_1, D_3 are cut-off. During this state the tapped inductor primary magnetizing inductance, L_m, is charged from the input voltage source, V_g, while the DC voltage, V_{dc}, is applied to the input terminals of the output filter so the filter inductance, L_o, is charged feeding also the filter capacitor, C_o, and the load R_L.

State B

State B lasts for a duration of t_b .The switch M_1 is turned off and M_2 is turned on, whereas M4 keeps conducting. Here, both D_1 and D_2 conduct while D_3 is cut-off. Hence, the tapped inductor magnetizing inductance, L_m, continues charging from

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the input voltage source, V_g, whereas the input terminals of the output filter are shorted so the filter inductance, L_o, is discharged to the output capacitor C_o and the load R_L.

State C

State C lasts for duration of t_c .State begins as the switches M_1, M_3 are turned on and M_2, M_4 are turned off., and completes the switching cycle. Here, both D_1, D_2 are cut-off and D_3 conducts; the tapped inductor magnetizing inductance, L_m, is discharged via both windings and D_3 into the DC link capacitor, C_{dc}, while the input terminals of the output filter are shorted and the filter inductance, L_o, feeds the output capacitor, C_o, and the load R_L.

In order to generate output voltage of negative polarity, complementary switching states A', B', C' are created by the controller. Switching states of semiconductor devices throughout the switching cycle are summarized in Table I

Table.I . Switching states of MOSFETS

	POSITIVE OUTPUT VOLTAGE			NEGATIVE OUTPUT VOLTAGE		
	STATE A	STATE B	STATE C	STATE A'	STATE B'	STAT E C'
M1	ON	OFF	ON	OFF	OFF	ON
M2	OFF	ON	OFF	ON	ON	OFF
M3	OFF	OFF	ON	ON	OFF	OFF
M4	ON	ON	OFF	OFF	ON	OFF
D1	OFF	ON	OFF	ON	ON	OFF
D2	ON	ON	OFF	OFF	ON	OFF
D3	OFF	OFF	ON	OFF	OFF	ON

The desired switching signals for the H-bridge switches should be generated of the given buck and boost switching functions and the output polarity signal $S_{bk}(D_{bk})$, $S_{bst}(D_{bst})$, P, respectively. Here, the driving signals of the switches $M_1 \ldots M_4$ are realized as below in (2)

$$S_1 = \overline{\overline{P \cdot S_{bk}} \cdot S_{bst}}$$
$$S_2 = \overline{P \cdot S_{bk}} \cdot S_{bst}$$
$$S_3 = \overline{\overline{P} \cdot S_{bk}} \cdot S_{bst}$$
$$S_4 = \overline{\overline{P} \cdot S_{bk}} \cdot S_{bst} \qquad (2)$$

By using the above switching states theoretical waveforms were obtained as per the fig .3.This includesSbst,Sbk,S1,S2,S3,S4,Vab,Vw1,i_{lo}.ig.

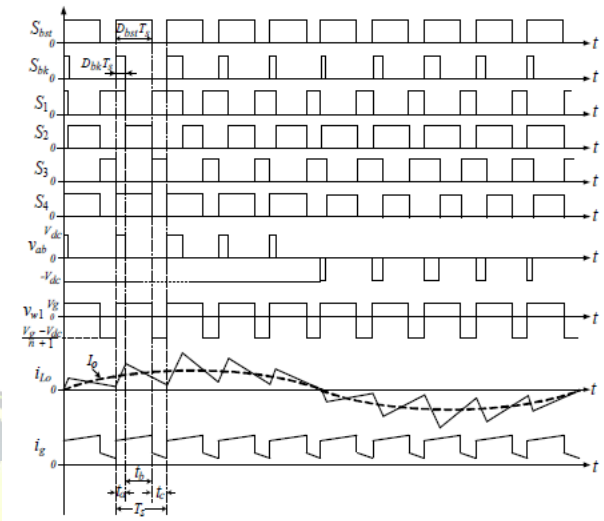

Fig. 3.Theoritical waveforms of proposed scheme

III. SSBI ANALYSIS

Certain assumptions are made to analyse the system proposed (a) all semiconductors are ideal with zero on resistance and voltage drop

(b) the decoupling capacitor and the output filter capacitor are sufficiently large and their voltage ripple is negligible;

(c) continuous current operation of both the tapped inductor and the output filter inductor is assumed.

A. Derivation of Voltage Conversion Ratio

From the analysis of converter's equivalent circuits in Fig. 2 shows that the inverter operates as a boost-derived tapped inductor DC-DC converter merged with a buck-derived full-bridge DC-AC inverter.

Define t_a, t_b, and t_c the duration of states A, B and C respectively and $T_s=t_a+t_b+t_c$ the switching period. Boost charging state, that is the time interval dedicated to charging the primary winding of the tapped inductor, takes place during the states A and B, see Fig. 2(a) and Fig. 2 (b), whereas, boost discharge takes place in state C. The total duration of the boost charging is, therefore:

$$tbst = ta + tb \qquad (3)$$

Accordingly, the resulting boost duty cycle, D_{bst}, is

$$Dbst = \frac{ta + tb}{Ts} \qquad (4)$$

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Here, SSBI creates the DC-DC step-up conversion function identically to the tapped inductor boost converter. Adopting the approach of [8] and [9], the DC-DC voltage conversion ratio of SSBI is

$$Mbst = \frac{Vdc}{Vg} = \frac{1 + nDbst}{1 - Dbst} \qquad (5)$$

According to the state description above, the buck charging state, that is, the time interval dedicated to charging the output inductor, L_o, occurs in state A, whereas buck discharge takes place in states B and C while the terminals of the output filter are shorted. Thus, the duration of the buck charging is:

$$tbk = ta \qquad (6)$$

Accordingly, the resulting buck duty cycle, D_{bk}, is

$$Dbk = \frac{ta}{Ts} \qquad (7)$$

Clearly, under CCM condition of the output filter inductor, the voltage gain of the output section is identical to that of a buck converter and is given by:

$$Mbk = \frac{Vo}{Vdc} = Dbk \qquad (8)$$

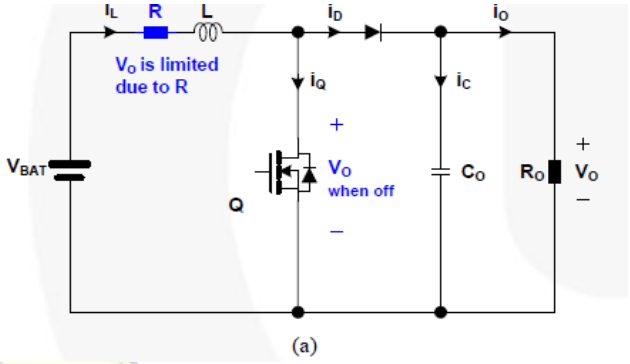
Hence, the overall DC-AC voltage conversion ratio, M, of the proposed SSBI under CCM conditions can be derived combining (5) and (8):

$$M = \frac{Vo}{Vg} = MbkMbst = \frac{(1 - nDbst)\,Dbk}{1 - Dbst} \qquad (9)$$

. An important constrain arising for SSBI operation is that the buck duty ratio, D_{bk}, should be smaller than the boost duty ratio, D_{bst}, at all times: $D_{bk} < D_{bst}$. In stand-alone application the buck duty ratio, D_{bk}, is modulated to attain a sinusoidal output voltage, V_o, of required amplitude and frequency, whereas the boost duty ratio, D_{bst}, is adjusted to satisfy load power demand and so stabilize the DC link voltage, V_{dc}.

IV. COMPARISON

Comparison of the boost equivalent circuit of proposed scheme to that of conventional boost converter is done. a conventional boost converter provides limited output voltage due to the copper loss of the inductor. Moreover, the duty cycle should be increased near to unity to get a large voltage conversion ratio. It requires a smaller inductance, resulting in the high current stress on the main switch and high conduction losses. Since the output voltage is imposed on the main switch when turned off, the voltage stress is also high and so does the switching losses. Figure 5 shows the disadvantages of the conventional boost converter.

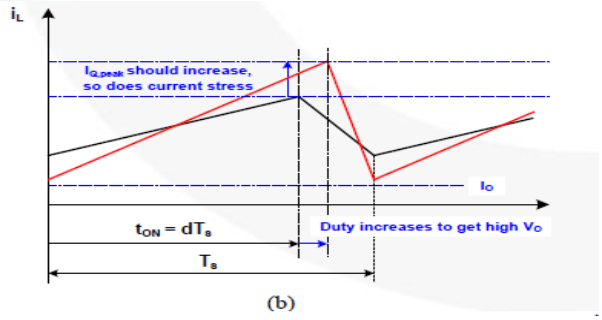


(a)

Fig . 4. Conventional boost converter

Among them the coupled inductor boost converter has attracted a lot of attention due to the high voltage conversion ratio, no additional components, the simple winding structure in the inductor, and low voltage stress on the main switch. To overcome this shortcoming a coupled inductor based boost converter topology is proposed.

Fig.6. shows the schematic of the coupled inductor boost converter and its key waveforms in CRM operation. If the turn's ratio n is zero, i.e. N_2 is zero, it is identical to the conventional boost converter. When the main switch (Q) turns on, $i_Q(t)$ increases with the slope of V_{BAT} over L_1, resulting in the built-up of energy in L_1. Since the voltage across the secondary turns N_2 is nV_{BAT}, the diode.Voltage $V_D(t)$ is V_O+nV_{BAT}, as shown in Figure 6 (b). After Q turns off, the voltage across the total inductor L_{eq} becomes V_O-V_{BAT}, so that the diode current $i_D(t)$ decreases with the slope of V_O-V_{BAT} over L_{eq}. Since the voltage across the primary turns N_1 is $N_1(V_O-V_{BAT})$ over N_1+N_2, the switch voltage $V_Q(t)$ is $(N_1V_O+N_2V_{BAT})$ over N_1+N_2, lower than V_O when N_2 is greater than N_1 for high voltage conversion ratio. Christo Ananth et al.[4] presented a brief outline on Electronic Devices and Circuits which forms the basis of the Clampers and Diodes.



(b)

Fig. 5. (a) Conventional Boost Converter and (b) its Inductor

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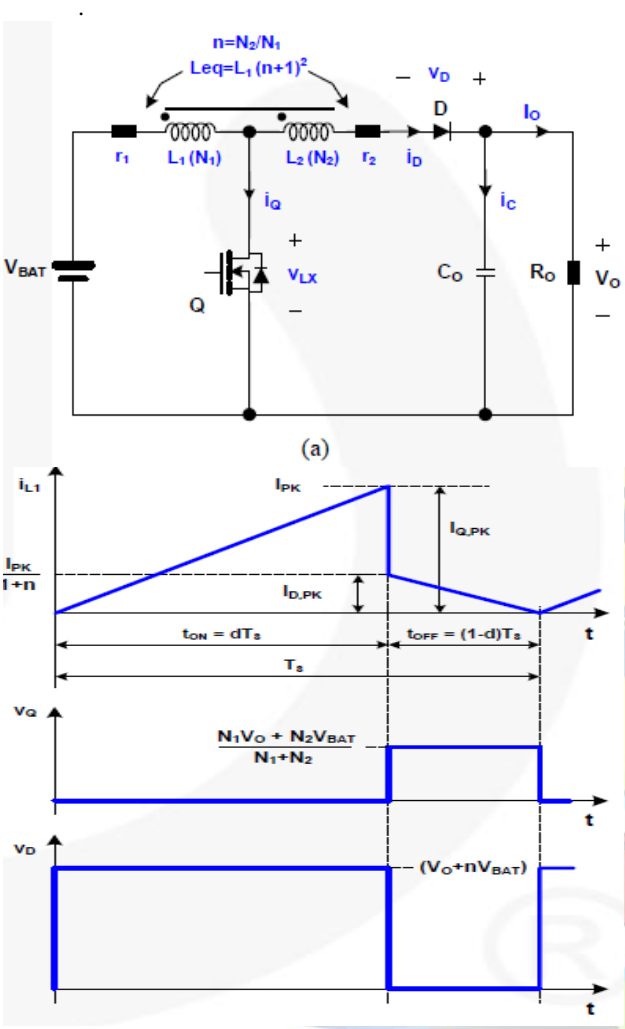

Fig. 6. (a) Coupled Inductor Boost Converter equivalent of proposed system and(b) its Key Waveforms: Inductor Current, Switch and Diode Voltages during CRM Operation.

Since the inductors are coupled in one magnetic core, the total inductance is calculated as follows:

$$L1 + L2 : L2 = (N1 + N2)^2 : N2^2 \quad (10)$$

Therefore

$$Leq = L1 + L2 - (1 + n)^2 L1 \quad (11)$$

To obtain the voltage conversion ratio in CCM or CRM operations, the volt-sec balance is required either for L_1 or for L_2. Let's use L_2. The voltage across L_2 for each mode is as follows:

$$VL2 = nVBAT \quad (12)$$

$$VL2 = (VO - VBAT)\frac{N2}{(N1 + N2)} \quad (13)$$

The voltage conversion ratio can be obtained by letting the sum of the applied voltage on L_2 times its duration over one switching cycle be zero, as follows:

$$\frac{VO}{VBAT} = \frac{1 + nd}{1 - d} \quad (14)$$

According to Equation (14), the voltage conversion ratio depends on the turn's ratio of the coupled inductor. If the turn's ratio is 3, the voltage gain becomes more than 10 for 0.7 of the duty cycle. It will be also decreased when the copper loss of the inductor is considered. Nevertheless, it is large compared to the conventional boost converter. Thus, it is possible to make a sufficient output voltage from a low-voltage battery to drive the piezoelectric actuator by tuning the turn's ratio. As can be seen in Figure 6, the voltage stress on the main switch is much lower than the conventional one. Therefore, the switching losses especially capacitive discharging losses can be reduced. However, the peak current of the main switch is 1+n times larger than the conventional one, which is one of the disadvantages of this topology. In addition, the voltage stress of the diode is increased a well.

V. SIMULATION RESULTS

Simulation of the proposed system in stand alone mode was done using matlab software .PWM control technique was used were the reference output is compared with ground to produce polarity signal P, the reference dc link voltage is compared with ramp inorder to obtain Sbst and also output sine waveform is compared with ramp to produce Sbk. By passing these through a logic necessary switching signals for each switch was obtained. High dc-dc gain was obtained from 35 V input dc from PV 350V in DC link was obtained and an output sine wave of high quality with low thd < 5 was obtained.

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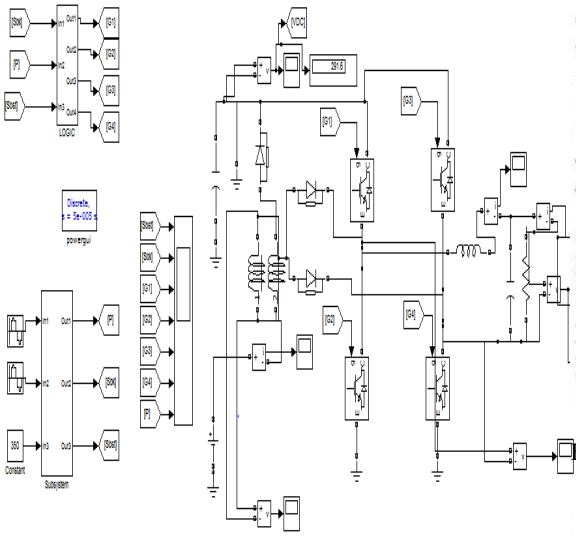

Fig. 7. Simulation diagram

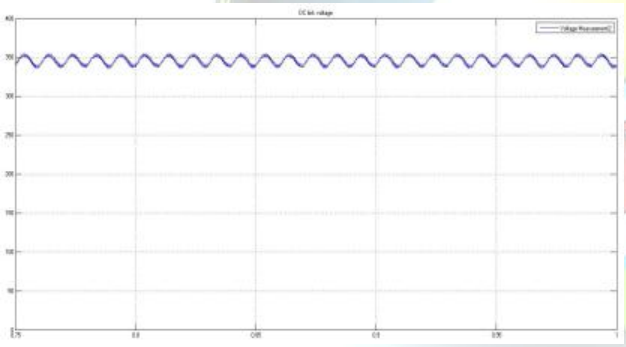

Fig. 8. DC link voltage

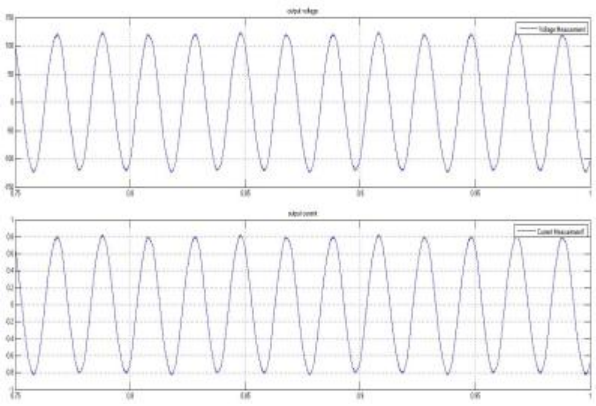

Fig. 9. Output voltage and current waveforms

Fig. 10. Control signals Sbst,Sbk,S1,S2,S3,S4,P

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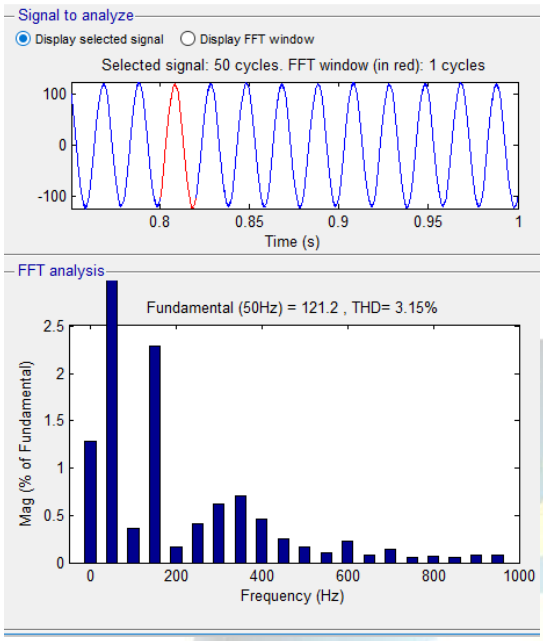

Fig. 11. Thd of the output waveform

VI. CONCLUSION

A PWM based single-stage inverter, SSI, for alternative energy generation applications is presented in this paper. The proposed topology employs a coupled inductor to attain high input voltage step-up and, consequently, allows operation from low DC input voltage. The paper presented principles of operation, simulation results. Theoretical findings stand in good agreement with simulation results. Acceptable efficiency was attained with low voltage input source. The SSI topology has the advantage of high voltage step-up which can be further increased adjusting the tapped inductor turns ratio. The SSBI allows decoupled control functions. By adjusting the boost duty cycle D_{bst} the SSBI can control the dc link voltage, whereas the output waveform can be shaped by varying the buck duty cycle, D_{bk}. The DC-AC power decoupling is attained on the high voltage DC link .The system has demonstrated low THD output for different types of highly non-linear loads.

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