ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 11, March 2017

Efficient low power design for 2:1 Multiplexer using Quasi adiabatic logic

HARITHA.M ,
ME-second year ,
Department of VLSI Design,
Tagore Institute Of Engineering And Technology,
Deviyakurichi(po), Attur(tk),
Salem(dt), Tamilnadu, India.
rrrajapriya@gmail.com

AROKIARAJ.S,
Assistant professor,
Department of ECE,
Tagore Institute Of Engineering And Technology,
Deviyakurichi(po), Attur(tk),
Salem(dt), Tamilnadu, India.
nithiarokia@gmail.com

ABSTRACT

A conventional CMOS logic circuit design access depends upon charging the output capacitive nodes to the supply voltage or discharging it to the ground. This is one of the most used approaches in VLSI designs. There are different techniques to design low power circuits both at system level as well as at circuit level to reduce power consumption. One of the major source of power dissipation is the charging and discharging of capacitor. At all when a capacitor is discharged to ground, an amount of power = ½ C stored in the capacitor is lost. We can reduce this power dissipation by restoring this power to the source alternately of discharging to the ground. Another way of reducing the power dissipation is to design the circuit in such a way that the charging of the capacitive node takes place very slowly. It has been executed that by charging the capacitor slowly, the power require is lesser than faster charging method. Adiabatic circuits use the above two approaches viz. slow charging of capacitor and discharging, and convert of charge to minimize the power consumed. Several Adiabatic designs have been arranged and tested in this paper. Most of them achieve valid power savings in comparison to conventional CMOS designs. The major drawbacks of these circuits include complex design for achieving simple operations, essential of multiple clocks and essential of complimentary input signals for controlling the charging and discharging operation. The Current work is based on an existing adiabatic logic style familiar as PFAL (Positive Feedback Adiabatic Logic) and ECRL (Power Efficient Charge Recovery Logic) which are simple and doesn't require

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 11, March 2017

complimentary signals or complex clocking.. In this paper all circuits are analysed in terms of power and simulated using Tanner EDA.

1. INTRODUCTION

Due to growing market of portable electronic devices such as cellphones, personal digital assistants, laptops etc., low power consumption has become a major concern in integrated circuit design. Due to the defined power supplied by the batteries, the circuitry involved in these devices must be arranged to consume less power.Among many design techniques, adiabatic access is one method of reducing power dissipation in logic circuits. Conventional CMOS based designs consume a lot of power during the charging and discharging of the node capacitances of the circuits[1]. Such part of the full power dissipated by a circuit is called dynamic power. Dynamic power dissipation can be reduced by using an alternative access to the traditional techniques of power consumption rebate called adiabatic switching.

Adiabatic switching technique reduces the power dissipation through PMOS during charging operation and reuses some of the power which is stored on load capacitor during the discharging phase.

2. ADIABATIC LOGIC

The term “adiabatic” full a thermodynamic operation in which there is no power arrangement with the environment, and therefore no dissipation of power or power occurs. Adiabatic logic works on the principle of reversible logics. The power clock is used both as a power supply & as a clock signal. .[6] presented a short overview on widely used microwave and RF applications and the denomination of frequency bands. The chapter start outs with an illustrative case on wave propagation which will introduce fundamental aspects of high frequency technology.

Dynamically adjusting the power-clock voltage to comply with constant-current charging results in adiabatic-charging effect. The power clock supply charges the load capacitor adiabatically during the time it is ramping up and allows the load capacitor power to recycle back when it is ramping down.

The two key rules by which adiabatic circuits try to conserve the power are:

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 11, March 2017

1. Never turn on a transistor when there is voltage difference between drain and source.
2. Never turn off a transistor that has current flowing through it.[4]

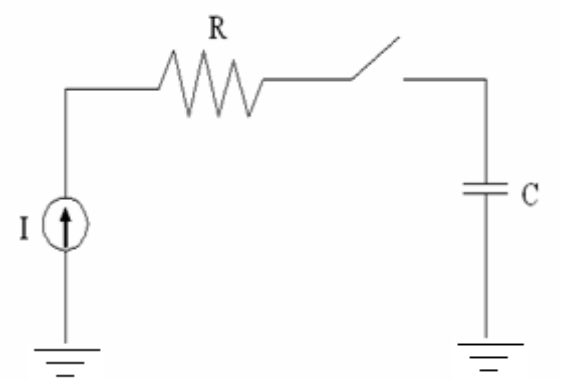

Figure.1: Circuit explaining Adiabatic Switching

Fig. 1 shows the RC model for the adiabatic circuit where the load capacitance C is charged by a time dependent current source I(t) alternately of the constant-voltage source as in the conventional CMOS circuits.
Voltage across the Capacitor V_C (t) = 1/C.I(t).t
The average current from 0 to t, I(t) = C. V_C(t)/t

Full power dissipation in resistor R from 0 to t= T is given by

$E = E_{diss} = R\int_0^T I^2 dt = \frac{2RC}{T} \left(\frac{1}{2} CV^2\right)$

where,

E — Power dissipated during charging,
C —Load capacitance,
R — Resistance of the MOS switch turned on,
V — Ultimate value of the voltage at the load,
T — Charging time.
From the above equation of power dissipation, following closures can be made:

1. For T >2RC, the dissipated power is small as compare to the conventional CMOS.

2. Power dissipation can be made arbitrarily small by more increasing the charging time.

3. The dissipated power is proportional to R. Thus, reducing the on-resistance of the PMOS network results in lower dissipation.

3.ADIABATIC LOGIC FAMILY

The two fundamental classes in which adiabatic circuits can be classified are:

1. Fully Adiabatic Circuit
2. Partially power recovery Adiabatic Circuit.

In fully adiabatic circuits, all charge on the load capacitance is recovered by the power supply whereas in

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 11, March 2017

partially adiabatic some charge is transferred to the ground.
Partial adiabatic approaches are:

- Efficient Charge Recovery Logic (ECRL)
- Positive Feedback Adiabatic Logic (PFAL)
- NMOS Power Recovery Logic (NERL)
- Clocked Adiabatic Logic (CAL)
- True Single-Phase Adiabatic Logic (TSEL)
- Source-coupled Adiabatic Logic (SCAL)

Full adiabatic approaches are:

- Pass Transistor Adiabatic Logic (PAL)
- Split-Rail Charge Recovery Logic (SCRL).

3.1 EFFICIENT CHARGE RECOVERY LOGIC

ECRL has two cross coupled PMOS and two NMOS tree structure. An AC power supply is used to recover the charge & reuse the supplied power. Both Out and $\overline{Out}$ is generated so that power clock generator always drive a constant load capacitance independent of the input signal. The logic function which is to be implemented is executed using NMOS transistors, in both true and integral forms.

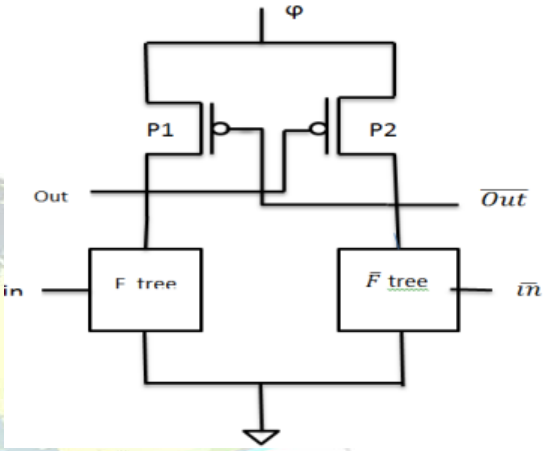

Figure.3: ECRL logic circuit

In above figure, let us assume in is high &inbar is at low. When power supply ramps up from 0 to V_{DD}, 'out' remains at a ground level &outbar follows power clock (φ) through P2.When power clock reaches V_{DD}, out &outbar holds the valid logic levels & these values are maintained during the hold phase and are used for the evaluation of the next stage. As φ ramps down from V_{DD} to ground, outbar returns its power to power clock i.e. delivered charge is recovered back to the power supply.

3.2 POSITIVE FEEDBACK ADIABATIC LOGIC

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 11, March 2017

PFAL consists of 2 cross-coupled inverters as latch familiar as sense amplifier which runs the two integral outputs of the circuit & the logic function N_F and its compliment are executed using NMOS networks which is connected parallel to PMOS.One of the logic blocks connects the concerned input to the power clock with a low resistance path and on the same time the other network provides a very high resistance in between the power clock and the other output. But the inverter's down network provides the second output a conducting path to the ground. In this way one of the two outputs (either integral or un-integral one) is pulled up to the power clock and other down to the ground. PFAL uses four phase clocking technique to recover the charge delivered by the power supply.

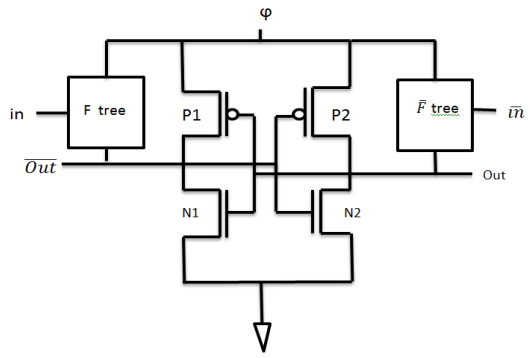

Figure.4: PFAL logic circuit

4. CIRCUIT IMPLEMENTATION

In this paper, three adiabatic techniques (ECRL, PFAL) & conventional CMOS logic were used to design 2:1 Multiplexer. The schematic & simulations of 2:1 Mux arranged using the logic designs are shown in the figures.

4.1.Conventional CMOS 2:1 MUX

A multiplexer is a combinational circuit that prefers one of the data inputs and transmits it to the output depending on the control signals. It implements the function F = $A\bar{S}$ + BS. When select(S) is Low, it outputs the signal A & when select(S) is High, it outputs the signal B.

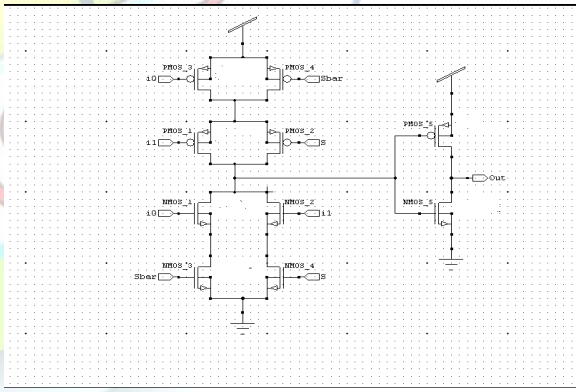

Figure.5:Schematic for 2:1 MUX using conventional CMOS

4.2. 2:1 MUX using ECRL

The logic density of ECRL is more as related to conventional CMOS that is achieved by eradication of PMOS transistors from each logic function. All functions are

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 11, March 2017

implemented using NMOS only, and PMOS transistors serve only as the pull-up devices. In ECRL circuits, the latch is executed using 2 cross-coupled PMOS transistors & the cascade integral logic array is executed with a NMOS logic tree.

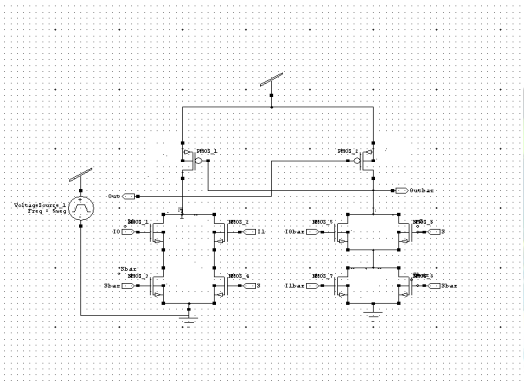

Figure.6: Schematic for ECRL inverter based 2:1 MUX.

4.3. 2:1 MUX using PFAL

The two cross coupled inverters runs the two integral outputs of the circuit. The logic function F = $A\bar{S}$ + BS is executed using NMOS network which is connected parallel to PMOS transistor & results in the rebate of equivalent resistance of the logic network thereby reducing the power dissipation.

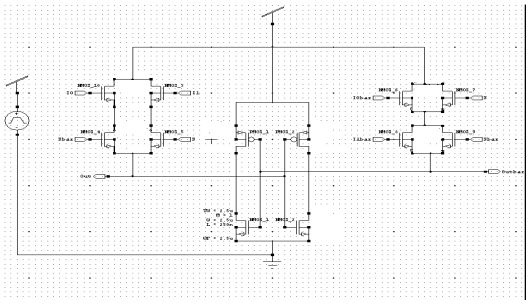

Figure.7: Schematic for PFAL based 2:1 MUX

5. SIMULATION RESULTS

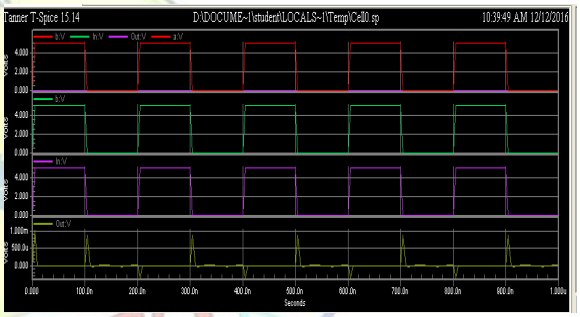

Figure.8: Simulation waveform of CMOS 2:1 MUX

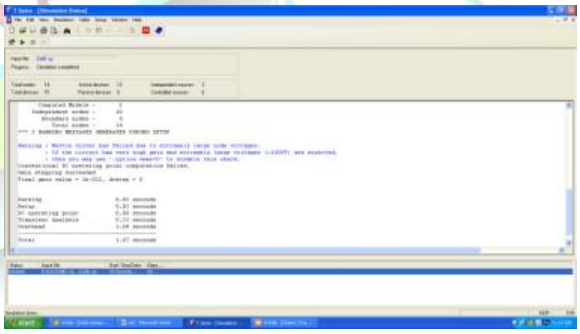

Figure.9:POWERCONSUMPTION

6. CONCLUSION

The main idea of this project is to introduce the design of high

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 11, March 2017

performance and power efficient 2:1 multiplexer design..In the current work,the 2:1 mux design is implemented by conventional cmos logic. More the design is implemented using ECRL &PFALlogic. . These adiabatic techniques can be used for low power applications over the wide range of parameter variation. So, the required logic can be executed within an optimized area which performs faster when related to the conventional CMOS design.

Parameters	CMOS	ECRL	PFAL
Transisitor count	18	10	12
MAX.frequency	25mhz	25mhz	25mhz
AVG.power	83uw	9.53uw	9.24uw

Table.1: Average power dissipation v/s frequency for 2:1Mux.

7. REFERENCES

[1]low power design methodologies Jan.M.Rabey and Massoud Pedram Kluwer academic publishers.

[2] Prof Mukesh Tiwari, Prof Jaikaran Singh, Mr Yashasvi Vaidhya "Adiabatic Improved Efficient Charge Recovery Logic for low power CMOS logic " International journal of Electronic Communication and Computer Engineering pp 350-354 Vol 1 issue 5.

[3]Samik Samanta Power Efficient VLSI Inverter Design using Adiabatic Logic and Estimation of Power dissipation using VLSI-EDA Tool Special Issue of IJCCT Vol. 2 Issue 2, 3, 4; 2010 for International Conference [ICCT-2010], 3rd-5th December 2010.

[4]Prasad D Khandekar, Shaila Subbaraman, and Abhijit V. Chitre Implementation and Analysis of Quasi-Adiabatic Inverters International conference of engineers and computer Scientist 2010 Vol II IMECS 17-19-201 Hong Kong.

[5]Aiyappan Natarajan, David Jasinski, Wayne Burleson, Russell Tessier A Hybrid Adiabatic Content Addressable Memory for Ultra Low-Power Applications GLSVLSI'03, April 28–29, 2003, Washington, DC, USA.

[6] Christo Ananth, [Account ID: AORZMT9EL3DL0],"A Detailed Analysis Of Two Port RF Networks - Circuit Representation [RF & Microwave Engineering Book 1]", Kindle Edition, USA, ASIN: B06XQY4MVL, ISBN: 978-15-208-752-1-7, Volume 8, March 2017, pp:1-38.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 11, March 2017

[7]A.Kishore Kumar, Dr.D.Somasundareswari, Dr.V.Duraisamy, M.Pradeepkumar "Low Power Multiplier Design Using Integral Pass-Transistor Asynchronous Adiabatic Logic" International Journal on Computer Science and Engineering Vol. 02, No. 07, 2010, 2291-2297.

[8]Praveer Saxena ,Prof. Dinesh Chandra, Sampath Kumar V "AN ADIABATIC ACCESS FOR LOW POWER FULL ADDER DESIGN" International Journal on Computer Science and Engineering (IJCSE) Vol. 3 No. 9 september 2011.

[9]Satyam Mandavilli, Prashanth Paramahans " An Efficient Adiabatic Circuit Design Access for" International Journal of Recent Trends in Engineering, Vol 2, No. 1, November 2009 Low Power Applications.

[10]U.Narayanan, H.W. Leong, K.S. Chung, C.L. Liu, "Low power Multiplexer Decomposition,"Proceedings of International Symposium on Low Power Electronics and Design, pp.269-274,1997.