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IMPLEMENTATION OF UART WITH DFT LOGIC FOR BUILT IN SELF TEST USING VERILOG HDL

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ABSTRACT

BIST is one of the most popular test technique recycled now a days. The embedded BIST capability in this project has the objectives to satisfy specified testability requirements and to generate the lowest-cost with the highest performance implementation.

Serial communication is usually implemented by (UART), mostly recycled for short distance, low speed, low cost data exchange tween processor and peripherals . There is a demand for realizing the usefulity of UART in a single or a very few chips. Further, design systems without full testability are open to the expanded possibility of product failures and missed market opportunities. Also, there is a demand to ensure the data transfer is error proof.

In this paper, introduction of BIST and status register for UART to beaten the above two constraints of testability and data integrity. The 8-bit UART with BIST module is coded in VHDL, synthesized and simulated using Xilinx ISE design. The results announce that this model eliminates the demand for higher end, expensive testers and thereby it can reduce the development cost, valuable time.

INTRODUCTION

Universal Asynchronous Receiver Transmitter (UART) is a gentle of serial communication protocol; mostly recycled for short-distance, low speed, low-cost data exchange tween computer and peripherals. UARTs are recycled for asynchronous serial data communication by applying data from parallel to serial at

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transmitter with some extra overhead bits using shift register and vice versa at receiver. It is commonly connected tween a processor and a peripheral, to the processor the UART appears as an 8-bit read/write parallel port. Built-in Self Test, or BIST, is the technique of designing additional hardware and software looks into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation using their own circuits, thereby contacting dependence on external Automated Test Equipment (ATE). BIST is a Design-for-Testability (DFT) technique, because it makes the electrical testing of a chip easier, faster, more efficient, and less costly. The concept of BIST is suited to just about any gentle of circuit, so its implementation can vary as widely as the product diversity that it caters to. Advantages of implementing BIST include: lower cost of test, since the demand for external electrical testing using an ATE will be reduced, if not eliminated; better fault coverage, since special test structures can be integrated onto the chips; shorter test times if the BIST can be arranged to test more structures in parallel; easier customer support; and capability to perform tests outside the production electrical testing environment .

EXISTENCE SYSTEM

The structure design of systems at the gate and flip-flop level has become time consuming as the integrated circuit technology has become very convoluted. In recent years this fact has motivated control of hardware description language in the design process of digital system. VHDL is recycled to describe and simulate the operation of variety of digital system which is ranging in convolutedity from a few gates to an interconnection of many convoluted integrated circuits. Advantages of VHDL implementation includes minimum cost and time, better design, faster time to market and expanded flexibility.

UART ARCHITECTURE

UART supports asynchronous communication in which clock information is not shared tween transmitter and receiver; several overhead bits are sent along with data bits for synchronization purpose. This announces that data bits are transmitted in the form of frame. This frame is accepted at the receiver input where de-framing is done and only the data bits are usable in parallel form at the receiver output. The frame format is shown in fig.1

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Figure1 Frame Format for UART

The design of UART has LCR, Baud Rate Generator (BRG), Transmitter and Receiver as its useful units. All these blocks are elucidated in brief as course of rest of this section.

Line Control Register (LCR)

The line control register (LCR) is a byte register. It is recycled for actual specification of frame format and craved baud rate. The parity bits, stop bits, baud rate selection and word length can be changed by writing the appropriate bits in LCR, announces exact voltage levels of selection lines for choosing divergent baud rates, odd/even parity and data word length. .[7] presented a short overview on widely used microwave and RF applications and the denomination of frequency bands. The chapter start outs with an illustrative case on wave propagation which will introduce fundamental aspects of high frequency technology.

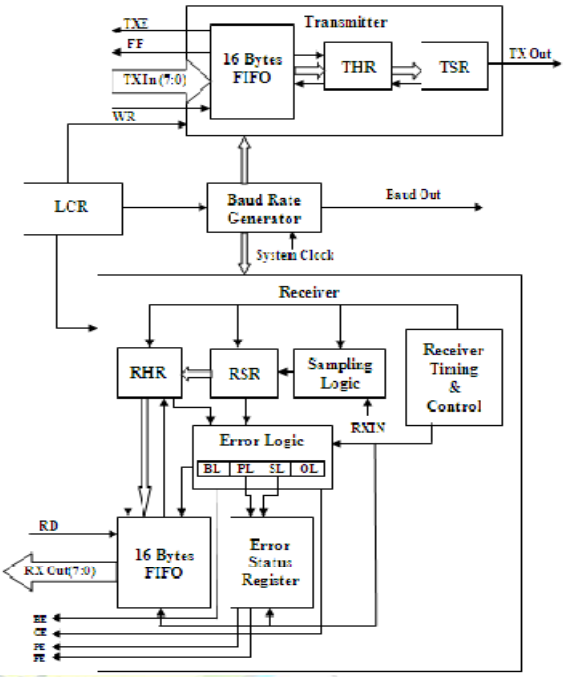

Figure 2. UART Architecture

Baud Rate Generator

The baud rate generator is programmable by three control bits Bit 0, Bit 1, Bit 2 in LCR. 8 divergent baud rates can be selected by divergent combinations of Bit 0, Bit 1 and Bit 2. For the careful baud rate the divisor can be obtained by dividing the system clock by craved baud rate which shows divisors for various baud rates using 10 MHz system clock.

Transmitter

The transmitter section gets parallel data, makes the frame of the data and conveys the data in serial form on the Transmitter Output (TXOUT)

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terminal. Data is weighted from the inputs TXIN0-TXIN7 into the Transmitter FIFO by applying logic high on the WR (Write) input.

Bit	Value			Description
	Bit2	*Bit1*	*Bit0*	*BR Sel.*
0,1,2	0	0	0	57600
	0	0	1	38400
	0	1	0	19200
	0	1	1	9600
	1	0	0	4800
	1	0	1	2400
	1	1	0	1200
	1	1	1	600
3	0			Even Parity
	1			Odd Parity
4	0			Parity Disable
	1			Parity Enable
5,6	Bit4	Bit3		DW Length
	0	0		5
	0	1		6
	1	0		7
	1	1		8
7	0			1 Stop Bit
	1			2 Stop Bits

Table 1 LCR bit description

If words less than 8 bits are recycled, only the least significant bits are transmitted.

Baud Rate	Freq = 10 MHz	
	Divisor	*% Error*
600	8333	0.00
1200	4165	0.00
2400	2082	0.00
4800	1040	0.00
9600	520	0.00
19200	259	0.10
38400	129	0.26
57600	86	-0.17

Table 2 divisors for various baud rates

Receiver

The transmitted data from the TXOUT pin is usable on the RXIN pin. The accepted data is applied to the sampling logic block. The receiver timing and control is recycled for synchronization of clock signal tween transmitter and receiver.

Initially the logic line is high whenever it goes low sampling and logic block will take 4 specimens of that bit and if all four are same it announces the start of a frame. After that resting bits are sampled in the same way and all the bits are send to Receiver Shift Register (RSR) one by one where the full frame is gathered. RSR is a 12 bit shift register. Now if the Receiver Hold Register (RHR) is empty it sends signal to RSR so that only the data bits from RSR goes to RHR which is an 8 bit register. The resting bits in the RSR are recycled by the error logic.

block. Now if receiver FIFO is empty it send the signal to RHR so that the data bits goes to FIFO. When RD signal is affirmed the data is usable in parallel form on the RXOUT0-RXOUT7 pins. The error logic block handles 4 types of errors: Parity error, Frame error, Overrun error, gap error. If the accepted parity does not contest with the parity generated from data bits PL bit will be set which announces that parity error appeared. If receiver fails to detect correct stop bit or when 4 specimens do not contest frame error occurs and SL bit is set. If the receiver FIFO is full and other data arrives at the RHR overrun error

occurs and OL bit is set. If the RXIN pin is beleived low for long time than the frame time then there is a gap in accepted data and gap error occurs

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and BL bit is set.

SIMULATION

Xilinx ISE is a software tool produced by Xilinx for synthesis and search of HDL designs, enabling the developer to synthesize their designs, perform timing search, examine RTL diagrams, simulate a design's reaction to divergent stimuli.

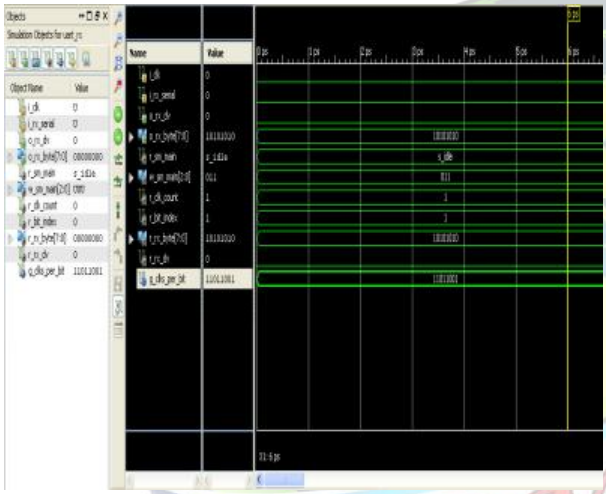

Figure 3: output waveform for UART transmitter

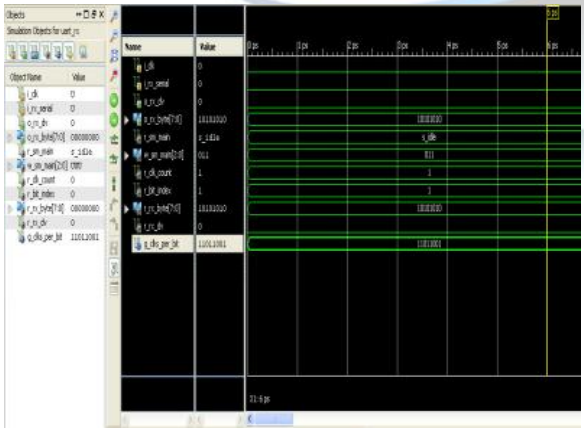

Figure 4: output waveform for UART receiver

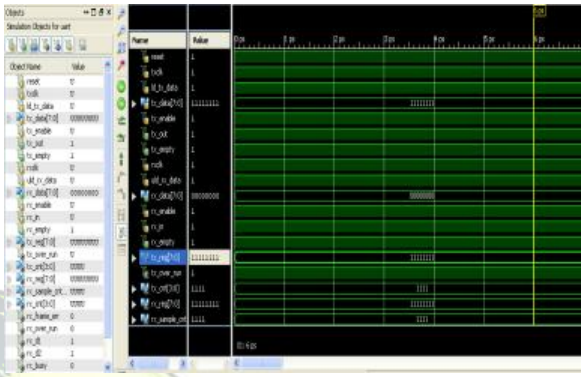

Figure 5: output waveform for UART with BIST module

CONCLUSION

This paper describes the architecture of UART with BIST technique called BILBO which will test that the UART is working properly or not. Working principle of this BIST technique has been tested by considering UART as a digital circuit under test using XILINX ISE simulator, which can be implemented by using VHDL. The architecture of UART that support various data word length, parity selection and divergent baud rates for serial transmission of data. Working principle of this UART has been tested using XILINX ISE simulator, which can be implemented by VHDL. Further the design is implemented using verilog HDL.

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