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Design and Analysis of Low Power Full Adder

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***Abstract*— In recent years there is a huge demand on portable devices that operate under low power. In order to balance the growing needs, chip designers are consistently trying to minimize the power consumption by scaling down the size of the transistors without sacrificing the computational performance. In current scenorio few research efforts are made to reduce the power consumed by transistors. Lot of circuits make use of transistors including full adder.Full adder is mainly used in VLSI devices like microprocessor and ASICs for computational pruposes. Thus the main aim of this project is to design low power fulladder with reduced number of transistors. The internal structure of this new adder consists of two XOR gates and one 2X1 Multiplexer. Pass transistor logic (PTL) is used to implement the two XOR gates and Multiplexer since this logic eliminates the redundant transistors thereby reducing the power. The adder has been developed using logic level, circuit level and mixed mode implementation. The schematic of all three designs has been developed using DSCH and its layout has been created using MICROWIND TOOL. The performance of the proposed design is verified by comparing with the existing full adder design(28T) in terms of power and area. The simulation of the proposed full adder has also been done by varying the foundry technologies from 32nm to 90nm. In comparison with the existing designs, the new design is found to give significant reduction in power.**

Keywords— full adder, mixed level, low power, pass transistor logic.

I. INTRODUCTION

Most of the VLSI applications consist of arithmetic operations. Addition, subtraction, multiplication and accumulate are the most common arithmetic operations. The full adder is the basic building block of all the arithmetic units. So its necessary to design a low power adder with reduced number of transistors to enhance the efficiency of the system. In this paper, the design and performance comparison of two full-adder cells is implemented based on the multiplexing of the Boolean functions XOR/ XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption has been discussed. The full adder has been analyzed using all different styles viz. logic level, mixed level and circuit level. The resultant full-adders show to be more efficient with regard to power consumption when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

II. PREVIOUS FULL ADDER OPTIMIZATIONS

The 1-bit full-adder functionality can be summarized by the following equations, given the three 1-bit inputs A, B, and C , it is desired to generate the two 1-bit outputs Sum and C

Sum =(A XOR B) XOR C
Cout=A B + Cin (A XOR B)

A. Logic Level Implementation

Logic levels are handled by electronic switches, called logic gates [9,10] which perform digital calculations and operations. The logic style used in logic gates basically influence the speed, size, power dissipation, and the wiring complexity of a circuit. Power dissipation is determined by the switching activity and the capacitances. The standard level implementation of the full adder circuit using gates is shown in fig.1. In this module the adder has been implemented using XOR gates and AND gates. Also the power dissipated by implementing the adder circuit with gates is also measured by simulating in MICROWIND tool. It is found to be 64.72µW.

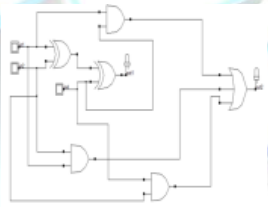

Fig 1: Logic Level Circuit

B. Mixed Level Implementation

In mixed level implementation [7,8], Full adder has been implemented using Multiplexers. In the logic level implementation, it is required to obtain an intermediate value of A(XOR)B and its compliment to obtain the final outputs. Thus the power consumption and propagation delay of the adder circuit depends on the function A(XOR)B and its compliment. From truth table of the full adder it can be seen that it can be seen that the So output is equal to the A (XOR) B when C=0 and its compliment when C=1. Thus a multiplexer can be used to implement the Sum function using carry as the select input. Similarly for the carry function, output is equal to A.B when C=0 and A+B when C=1. Again

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C can be used as select input for the implementation of output carry. The adder implemented using this logic has low propagation delay since MUX has been used in place of XOR /XNOR gates. Also the power consumed is 66.2 µW which is slightly higher compared to the logic level implementation. [7] proposed a system which contributes the complex parallelism mechanism to protect the information by using Advanced Encryption Standard (AES) Technique. AES is an encryption algorithm which uses 128 bit as a data and generates a secured data.

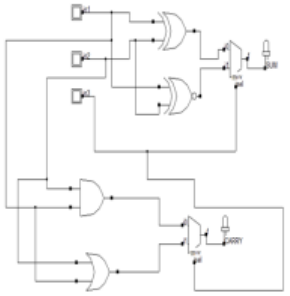

Fig 2: Mixed Level Existing Full Adder

C. Circuit Level Implementation

The circuit level implementation of existing full adder consist of 28 transistor .This 28 transistor is the combination of static CMOS logic [7, 8] and pass transistor logic[1]. The standard implementations of the full-adder cells shown in Fig. is based on the CMOS transmission gates (i.e., the combination of an NMOS and a PMOS pass-transistor) and has 20 transistors . Any logic function can be realized using NMOS pull down and PMOS pullup networks. The full adder cells generate XOR and its compliment function at the output. Both the XOR and its compliment is used to control the transmission gates generating the sum and carry outputs. But the inverter creates a delay between the XOR and XNOR output which creates glitches and leads to increased power consumption. Also the realization of XOR function is complex in CMOS logic.

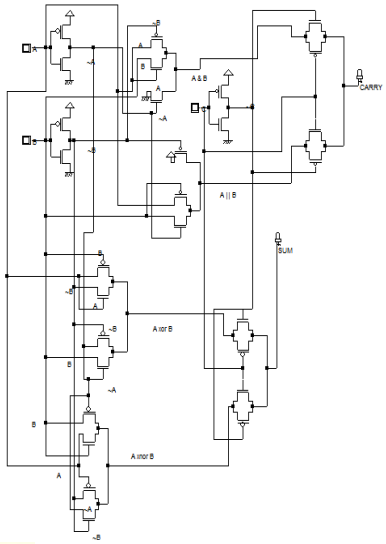

Fig 3: Gate Level Existing Full Adder

Because of these disadvantages pass transistor based implementation has been done. The basic difference of pass-transistor logic and CMOS logic style is that the input signals is connected to the source side of the l transistor networks. The advantage of one pass-transistor network is that it performs the logic operation, which results in a smaller number of transistors. Transistors works as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. So when the full adder design is implemented using 28pass transistor logic, the number of transistors is reduced but the power consumed in high as compared to other two logic levels i.e. 245 µW.
Energy-efficiency is one of the most important features required in modern electronic systems designed for high-performance and portable applications. In this ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. This module is the core of many arithmetic operations like Addition and Subtraction. From the existing designs its clear that making use of Pass Transistor logic reduces the number of transistors used and hence the power consumption. So to increase the operational speed and to decrease the power consumption, the concept of mixed level and pass transistor logic has been combined to implement energy efficient full adder in the proposed design.

III. PROPOSED DESIGN

A. Mixed Level (8T)

In the proposed design the adder has been implemented using mixed level logic design. Here only one MUX has been used as a selector and its used to generate the carry. From the truth table it can be seen that the carry output is equal to A(XOR)B when Cin=0 and its equal to input A when Cin=1.

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Since one of the MUX and AND/OR gates are removed, the number of transistors required for implementing this logic gets reduced and hence the power is reduced. The power consumed for the proposed design using mixed level logic is 42.560µw.

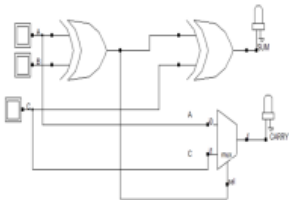

Fig 4: Mixed Level (8T) Circuit

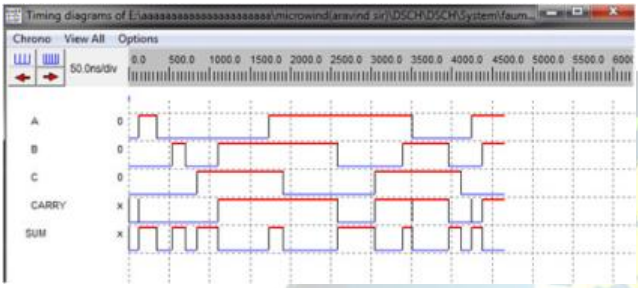

Fig5: Simulation waveform for Mixed Level Circuit

B. Circuit Level (8T)

The concept of complimentary CMOS logic is used in this design. The advantages of this logic are transistor sizing and thus reliable operation at low voltages and arbitrary transistor sizes. This proposed approach gives high performance full adder core based design on transistor level. The complementary CMOS full adder based on the regular CMOS structure with PMOS pull-up and NMOS pull-down transistors as shown in figure. When the input Y is at logic one, the inverter on the left functions as a normal CMOS inverter. Therefore the output is the complement of input X. When the input Y is at logic zero, the CMOS inverter output is at high impedance. The operation of the whole circuit could be given as a 2 input XOR gate as given in the circuit. Exact output logic levels are obtained for all the input combinations without any voltage degradation. However, when X=0 and Y=0, voltage degradation due to threshold drop occurs across the PMOS pass transistor and consequently the output is degraded with respect to the input. Since the output below nano watt cannot be measured using the microwind tool, the power is shown as zero. So an 10 T transistor logic has been proposed and designed.

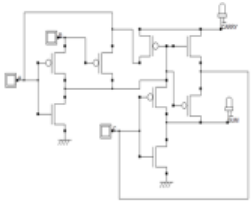

Fig 6: Circuit Level (8T) Circuit

C. Mixed Level (10T)

Proposed full adder circuits have been designed using two inverts and three MUX. A (XOR) B is implemented using a MUX and a NOT gate. One of the inputs to the MUX is A and the other input is the compliment of A. The second input B is given as select line. The output of this MUX is given as select line for the MUX which produces carry and Sum output. From the truth table it can be seen that the carry output is equal to A(XOR)B when C_{in}=0 and its equal to input A when Cin=1. The power consumed for this implementation is 7.341µw which is less than that of a 8T transistor.

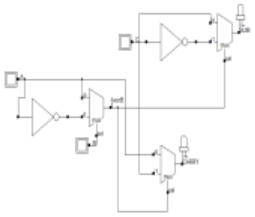

Fig 7: Mixed Level (10T) Circuit

Fig 8: Simulation Wave form for Mixed Level (10T) Circuit

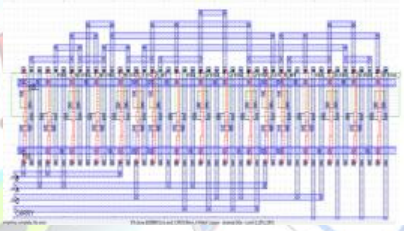

Fig 9: Layout Design for Mixed Level (10T) Circuit

D. Circuit Level (10T)

The circuit level design of proposed method consists of 10 transistors. In this the input V_{dd} is given and multiplexers are designed using pass transistor logic and the full adder is designed using 8 transistors. In this design (A XOR B) signal is passed to the pass transistor multiplexer made of two transistors to choose one among two. The output of this MUX is given as select line for the MUX which produces carry and Sum output. Design of 10T full adder cell has been used to generate the Sum, Carry and XOR. Since pass transistor logic has been used, the number of transistors used has been reduced. There is no static leakage in the pass transistor logic design. The supply voltage can be reduced at the cost of some increase in delay of the circuit.

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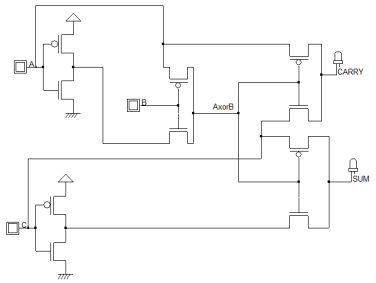

Fig 10: Circuit Level (10T) Circuit

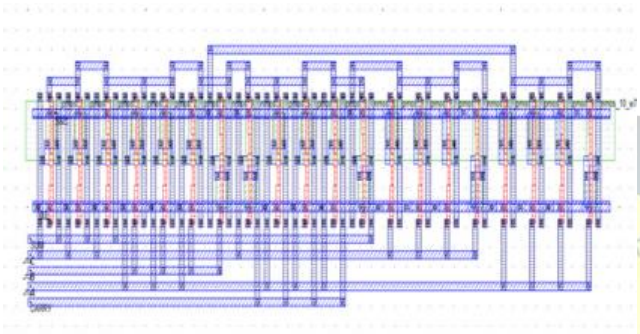

Fig 11: Layout Design for Circuit Level (10T) Circuit

IV. Simulation and Result

The simulation results for the 8T and 10T full adder cells regarding power consumption are shown in table IV. From the table we can see that the 10T designs exhibit the lowest power consumption for the mixed level and circuit level design. This validates the benefits of the structured approach. The adder has also been implemented in 90nm, 65nm and 45nm Technology scale. The power has been measured by connecting and disconnecting the supply voltage. The results are compared in table. The proposed adder design consumes 99% less power than other conventional CMOS adder.

Table 1: Comparison of Power in Digital Circuit

Volt	General Method (µW)	Exiting Method ((µW)	Proposed Method (8T) (µW)	Proposed Method (10T) (µW)
3.3	41. 080	47.081	38.219	7.341
5	47.253	66.200	42. 560	7.466

Table 2: Power comparison among various transistor style and technology by setting V_{dd} as 5v

Transistor Style	90 nm (1.2v)	65 nm (0.7v)	45 nm (0.4v)
28 Static CMOS Full adder	42.882µw	7.074µw	1. 586µw
28 pass transistor full adder	245µw	47.386µw	29.463µw
Proposed method(I)8T	0nw	0nw	0nw
Proposed 10T Transistor	3.551uw	0.849uw	0.250uw

Table 3: Power comparison among various transistor style and technology by setting V_{dd} as 3.3v

Transistor Style	90 nm (1.2v)	65 nm (0.7v)	45 nm (0.4v)
28 Static CMOS Full adder	41.526µw	6.897µw	1.539µw
28 pass transistor full adder	207µw	42.596µw	22.515µw
Proposed method(I)8T	0nw	0nw	0nw
Proposed 10T Transistor	3.563uw	01.014uw	0.281uw

V. Conclusion

The demand for low power circuits increases due to the emergence of wireless technologies which require a limited source of power. So the main idea is designing of high performance and power efficient full adder using multiplexer based pass transistor logic. In the present work, the full adder design is realized by mixed and circuit level designs. Also the design has been realized for various nanometer technologies and the power has also been measured and compared. Further the design is implemented by using pass transistor logic. The number of transistors required for realizing mixed CMOS design of full adder is less than the number of transistors required in realizing the design of full adder using CMOS transistors independently. So, the required logic can be realized within an optimized area which performs faster when compared to the conventional static CMOS full adder design.

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