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A VLSI Architecture for Image Compression Method using 14-Addition Based Discrete Cosine Transform

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***Abstract*— Integral histogram can accelerate the computing process of feature algorithm in computer vision, but exhibits high computational complexity and inefficient memory access. In this paper, we propose a configurable parallel architecture to improve the computing efficiency of integral histogram. Based on the configurable design in the architecture, multiple integral objects for integral histogram image, such image intensity, image gradient, and local binary pattern, are well supported. Meanwhile, by means of proposed strip-based memory partitioning mechanism, this architecture processes the integral histogram quickly with maximal parallelism in a pipeline manner. Besides, in this architecture, the proposed data correlation memory compression mechanism effectively solves the expansion problem of integral histogram memory caused by storing the histogram data. It fully reduces the data redundancy in the integral histogram.**

Keywords*— *Integral Histogram,Adder Unit,Discrete Cosine Transform,D Flip-Flop,Carry Save Adder

I. INTRODUCTION

The computer vision applications are widely used in many contexts. In particular, in mobile or embedded applications, the image detection and recognition based applications are very popular. For these vision applications, computing speed and power efficiency are important factors to consider. Feature algorithms that are commonly used to extract specific characteristics of objects in scenes generally exhibit high computational complexity in these vision applications. The integral histogram image plays an important role in accelerating the feature computing in vision applications. The system introduces a new DCT approximation that possesses an extremely low arithmetic complexity, requiring only 14 additions. This novel transform was obtained by means of solving a tailored optimization problem aiming at minimizing the transform computational cost. Second, to propose hardware implementations for several 2-D 8-point approximate DCT. The approximate DCT methods under considerations are (i) DCT transform; (ii) the 2008 Bouguezel-Ahmad-Swami(BAS) DCT approximation;(iii) the parametric transform for image compression; (iv) the Cintra-Bayer (CB) approximate DCT based on the rounding-off function;(v) the modified CB approximate DCT; and(vi) the DCT approximation proposed in the context of beam forming. All introduced implementations are sought to be fully parallel time-multiplexed 2-D architectures for 8X8 data blocks. Additionally, the proposed designs are based on successive cells of 1-D architectures taking advantage of the separability property of the 2-D DCT kernel. Data compression is the technique to reduce the redundancies in data representation in order to decrease data storage requirements and hence communication costs. Reducing the storage requirement is equivalent to increasing the capacity of the storage medium and hence communication bandwidth. Thus the development of efficient compression techniques will continue to be design challenge for future communication systems and advanced multimedia applications.

Data is represented as a combination of information and redundancy. Information is the portion of data that must be preserved permanently in its original form in order to correctly interpret the meaning or purpose of the data. Redundancy is that portion of data that can be removed when it is not needed or can be reinserted to interpret the data when needed. Most often, the redundancy is reinserted in order to generate the original data in its original form. A technique to reduce the redundancy of data is defined compression. The redundancy in data representation is reduced such a way that it can be subsequently reinserted to recover the original data, which is called decompression of the data. The discrete cosine transform helps separate the image into parts (or spectral sub-bands) of differing

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importance with respect to the image's visual quality. The DCT is similar to the discrete Fourier transform: it transforms a signal or image from the spatial domain to the frequency domain. A discrete cosine transform expesses a sequence of finitely many data points in terms of a sum of cosine functions oscillating at different frequencies. DCTs are important to numerous applications in science and engineering from lossy compression audio and images to spectral for the numerical solution of partial differential equations. The use of cosine rather than sine functions is critical in these applications: for compression, it turns out that cosine functions are much more efficient (as described below, fewer are needed to approximate a typical signal), whereas for differential equations the cosines express a particular choice of boundary conditions.

Multiplier- free approximate DCT transforms have been proposed that offer superior compression performance at very low circuit complexity. We introduce a novel 8-point DCT approximation that requires only 14 addition operations and no multiplications for low power consumption. The proposed DCT approximation is a candidate for reconfigurable video standards such as HEVC. The proposed transform and several other DCT approximations are mapped to systolic array digital architectures and physically realized as digital prototype circuits using FPGA technology. The minimization of data length implies less computation and consequently, low power consumption and higher speed. On the other hand, truncating introduces errors at the outputs and degrades the PSNR (Peak Signal to Noise Ratio). Thus a trade-off between power and PSNR is made. In the input side of the proposed method, the pixels of input images are encoded using unsigned 8-bit values. In the output side, DCT out1 contains the major part of the information, so this value must be encoded by the maximum number of bits. DCT out1 results in 3 successive additions of input pixels. Consequently, and considering the carry of each addition, the DCT out1 is encoded by using 11 bits. [3] proposed a system which can achieve a higher throughput and higher energy efficiency. The S-BOX is designed by using Advanced Encryption Standard (AES). The AES is a symmetric key standard for encryption and decryption of blocks of data.

In this proposed system, a new method of simultaneous compression and encryption based on a DCT transformation is presented. An optimized DCT algorithm is proposed to reduce real time application requirements. This algorithm needs only 4 multiplications to compute relevant DCT output data. The FPGA implementation of the whole method shows improvements in terms of throughput, area and power consumption. To prove the good performance, the proposed algorithm (DCT) is compared favorably with several existing methods.

II. PROPOSED SYSTEM

In this paper, introduce a novel 8-point DCT approximation that requires only 14 additions operations and no multiplications. The proposed DCT approximation that possesses an extremely low arithmetic complexity, requiring only 14 additions this novel transforms was obtained by means of solving a tailored optimization problem aiming at minimizing the transform computational costs. The modified CB-2011 approximation and the proposed transform possess lower computational complexity and are faster than all other approximations under consideration. In terms of image compression, the proposed transform could outperform the modified CB-2011 algorithm cost. An orthogonal approximation for the 8-point discrete cosine transform is introduced. The proposed transformation matrix contains only zeros and ones; multiplications and bit shift operations are absent. Close spectral behavior relative to the DCT was adopted as a design criterion.

The 8-point DCT is a key step in many image and video processing applications. This particular block length is widely adopted in several image and video coding standards, such as JPEG, MPEG-1, MPEG-2,H.261, and H.263. This is mainly due to its good energy compaction properties, which are closely related. The 8X8 DCT is widely used in image compression algorithm because of its energy compaction for correlated image pixels. The basis function for the DCT is the cosine, a real function that is easy to compute. The DCT is a unitary transform, and the sum of the energy in the transform and spatial domains is the same. Fast algorithms for the DCThave been developed to accommodate the many arithmetic operations involved in implementing the DCT directly. Let N=8. According to the 5 product and 29 sum operations have to be performed in order to evaluate eight 1=D coefficients. In every video cube with N=8, the 1-D transform has to be repeated 192 times to obtain 51 frequency coefficients. Imagine a test grayscale video sequence with dimensions of 720X576 picture elements and length of 24 frames. The minimal number of arithmetic operations for encoding such sequence is 18,662,400 products and 108,241,920 sums. The 8X8 DCT can also be viewed in the spatial domain as a weighted linear combination of 8X8 coefficients. If the input is highly correlated and all the coefficients have the same value, all the transform coefficients have a value of zero except the DC coefficient, and data compression is achieved.

The output of the flow diagram is twice the actual output value. Since each of data is processed twice by the 1-D DCT, the final value should divided by four(shifting right by two bits). After this scaling, rounding is required to obtain the final result. This results in eight additional rounding and eight additional scaling operations to the 1-D DCT inner kernel. These scaling and rounding operations can be omitted by scaling the DCT coefficients of the second pass by four, thereby decreasing the cycle count and

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increasing the speed of the 8X8 DCT. However, because two sets of DCT coefficients are needed. This technique requires additional 16-bytes of memory. The error introduced by scaling the coefficients is minimal. In fact, the 8X8 non pruned 2-D transformation can be decomposed into eight non pruned row wise 1-D transformations; followed by eight column wise instantiations of the same 1-D transformation. On the other hand, thevtransforms with lowest arithmetic complexities are the modified CB-2011 appoximation and new proposed transform, both requiring only 14 additions. The new transform could outperform the modified CB-2011 approximation as an image compression Tool as indicated by the PSNR and UQI values.There are three modules in the proposed methodology.

A. 1st stage Adder unit

The input bits are applied to the DCT transform architecture and to optimize the internal operation. The DCT transform is used to optimize the adder and subtractor and the multiplier unit. The adder unit is used to reduce the carry selection process in required addition operation for the DCT transform architecture. This architecture is to modify the adder carries propagation chain along the critical path. And this architecture is to improve the system efficiency.

B. Carry Save Adder

The adder section is to using modified the carry save adder process and optimize the adder architecture. The carry save adder unit is reducing the transform function due to the transmission time. The transforming operation is mainly focused by the carry selection process and reduces the number of gates into transform architecture. To reduce the power consumption level and the system speed to be high. This modified architecture used in the cryptography applications.

C. D Flip-Flop

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. The D flip-flop is widely used. It is also known as a “data” or”delay” flip-flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). And that captured value becomes the Q output. At other times, the output Q does not change. The D flip flop can be viewed as a memory cell.

The flow diagram (fig.1) gives full information about how the data compression is done. Then each process will explained in modules descriptions.

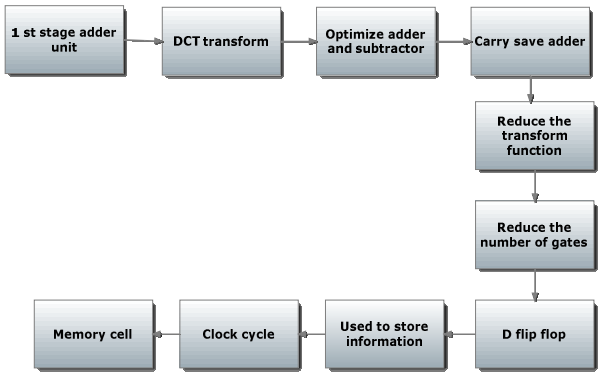

Fig.1 Data flow diagram

III. EXPERIMENTAL RESULTS

Histogram of input image

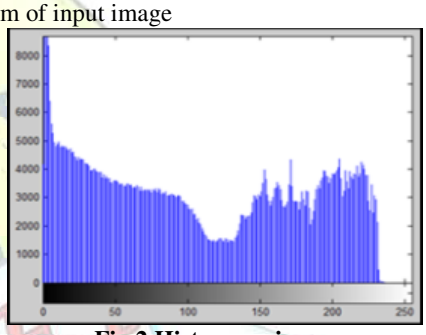

Fig.2 Histogram image

The transformed image is given as follows

Fig.3 Transformation of image

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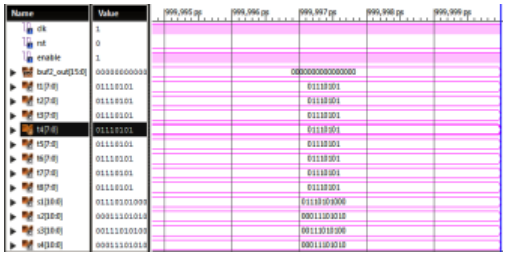

Fig.4 Simulation result

Fig.5 Synthesis report

Output results for proposed system

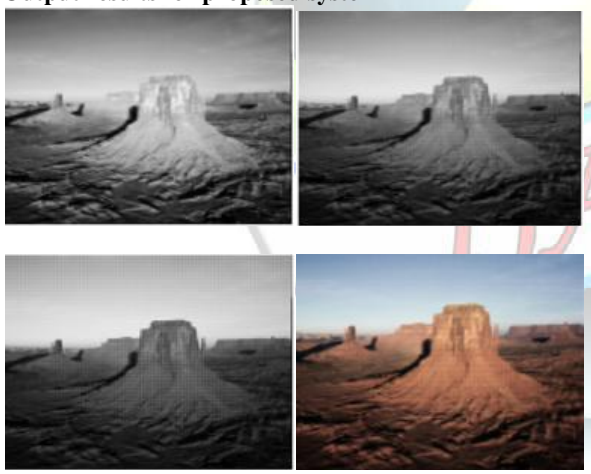

Fig.6 Output results

Table 1 shows that the design summary of Proposed System

Resources	Used	Available	Utilization
Number of slice LUT's	96	63400	0%
Number of fully used LUT FF pairs	0	96	0%
Number of bonded IOB's	153	230	72%
Number of slice LUT's	96	63400	0%

Table 1 Design summary

Comparison Table

Parameter	Existing System	Proposed System
Additions	10	14
Multiplications	1	0
Image resolution	640X480	720X576
Clock speed(MHz)	50	255
PSNR=67,1804		
MSE=0.0277		
Com-ratio=12		

Table 2 Comparison table

IV. CONCLUSION

We presented a very low-complexity DCT approximation obtained via pruning. The resulting approximate transform requires only 14 additions and possesses performance metric comparable with state of the art methods, including the recent architecture presented. By means of computational simulation, VLSI hardware realizations, and a full HEVC implementation, we demonstrated the practical relevance of our method as an image and video codec.

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