ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 20, March 2017

DESIGN OF MULTILEVEL FILTER BANK ARCHITECTURE OF SIGNAL DENOISE USING SIMULINK

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***Abstract*— Communication technology is focused by long distance data transmission and reception without noise and to optimize the signal denoise processing systems and improve accuracy level. The existing system concerns about the commercial ANC headphone in which uses the digital signal processors with high speed to remove the noise from the input signal results high power consumption. The contribution of ANC system can be classified into: 1) proper filter length selection; 2) low-power storage mechanism for convolution operation; 3) high throughput pipelining architecture. The proposed FPGA-Simulink based multilevel filter bank architecture design to improve the signal reconstruction effectively and reduce the latency level. Xilinx simulink design is used to remove the noise from the input speech signal. Finally, the simulink design is analyzed through simulation and synthesis results. The complexity has been reduced up to 95% through the selection of filter length as two at each stage of DWT algorithm.**

Keywords*— Discrete wavelet transform, Xilinx based simulink design, Xilinx hardware process.

I. INTRODUCTION

Active control technique can attenuate low-frequency noise in ducts-headphones home window applications, high speed elevator, and yacht environments where many methods have been used, such as feedback controller, feedforward controller, and hybrid controller. The existing active noise cancelling systems use filtered-x least, mean square algorithm to continuously adjust the coefficients of the digital filter through a cost function based on the amount of noise measured. These ANC systems require high computational complexity, power intensive hardware, and significant processing time for measuring noise signal, and then calculating and synthesizing proper anti-noise signals to cancel out the noise signals in real time.

The theory of actively cancelling the noise is simple, but the realization of an efficient ANC system is challenging due to several physical constraints. This paper proposes high performance feedforward ANC architecture and implements a high performance low-power circuit design accordingly based on the filtered-x least mean square algorithm. This system has high filter length but low switching activity to save power and it has high complexity [1], [2]. Reducing noise in hearing aids is difficult in many different ways over the years. This has been identified as the great problem while increase the speed and memory space in buffer section and saves power [3].With ideal spatial adaptation, an oracle furnishes information about how to best adapt a spatially variable estimator, whether piecewise polynomial,variable knot spline, or variable bandwidth kernel, to the unknown function. This paper describes a new principle for spatially-adaptive estimation: selective wavelet reconstruction. The system has high complexity and better BER and PSNR values [4].the need for evidence of benefit specific to digital signal processing in hearing aids is stressed as well as addressing cost-benefit ratios in the view of the high cost of digital hearing aids. The system has low performance but it saves power [5]. This paper investigates the use of wavelet transform for denoising speech signals intercept with common noises. Shown are the basic principles of wavelet transform as an alternative to the Fourier transform. This system consumes more power [6].

In existing work; a feedforward ANC circuit implementation based on the FxLMS adaptive algorithm for high fidelity in-ear headphones is developed. We have optimized the FxLMS adaptive algorithm with filter length exploration and proposed efficient hardware architecture for realizing the required convolution operations. A dedicated storage mechanism called one update circular buffer is proposed to keep the switching activity low to save power. Finally, three stage multiply accumulator is used to increase

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ISSN 2394-3785 (Online)
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the data throughput. The proposed filter bank design uses the one low-pass filter and one high-pass filter to decompose the incoming signal in simulink through discrete wavelets. The discrete wavelet transform is responsible for achieve a less computational load for DSP operations. The proposed system for denoising the signal is obtained by simulink with Xilinx blocks based design.this work is to modify the regular filtering process and to analysis the internal filtering samples. Finally, architecture work is to convert the simulink design into hardware code and optimize the filter processing time and speed.

II. PROPOSED SYSTEM

Unlike the standard HDL languages Xilinx system generator provides a model based design interface using an extended library of building blocks to create hardware. Rather than at textual code level, Xilinx system generator takes the abstraction level one step higher, and uses the Mathworks simulink environment to provide a graphical approach. Xilinx system generator uses simulink tool to model designs by connecting hardware blocks together. Interfacing between the simulink environment and FPGA platform is done using a slower standard JTAG connection or a gigabit Ethernet connection which allows a fast data transfer. The noise from the input speech signal is removed using Xilinx simulink design. The DWT (discrete wavelet transform) technique is used for simulink design and to minimize the filter circuit process. DWT is a linear transformation that provides the different vector of same length when operates on a data vector with length of integer's power of two. Isolation of data into frequency components and also matching of each component with resolution to the scale is done by DWT. Multiscale representation of function is the special feature of DWT. There are five modules in the proposed methodology.

A. Signal Pre-Processing

First we select the limited no of sample signal from the speech signal as an input. Then add the AWGN noise signal to the selected input signal which is apply to simulink model.

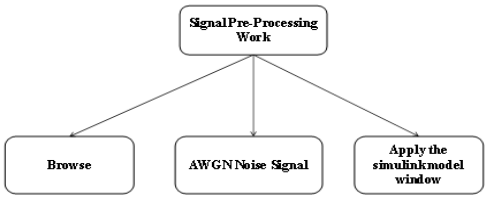

Fig.1 Speech Pre-Processing

B. Xilinx based Simulink design

Xilinx system generator (XSG) simulink model is used to satisfy the binary signal processing work. The gate in function is used to convert the integer value to binary values.

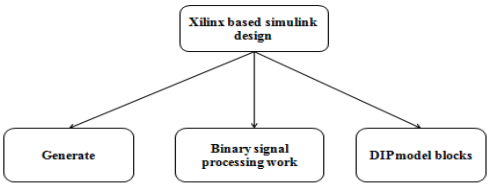

Fig.2 XSG blocks based design

C. Multilevel filter bank DWT architecture

DWT technique has three main blocks such as decomposition, threshold function and reconstruction. Textures recorded different resolutions have to analyze by effective wavelets. To increase the frequency resolution, the decomposition process is repeated again. It is calculated by the series of filters each followed by the down sampling with factor 2. The process is represented as sub-space with time-frequency locale which is implemented by binary tree with different nodes. This tree is called as filter bank. Two filter pairs are used in each decomposition and reconstruction block. Each filter pair consist of one low pass filter and one high pass filter. DWT of a signal is calculated by signal passing through the cascade of filtering using low pass and high pass filter. The outputs giving the detailed coefficients from high pass filter and also approximation coefficients from the low pass filter. [7] discussed about Improved Particle Swarm Optimization. The fuzzy filter based on particle swarm optimization is used to remove the high density image impulse noise, which occur during the transmission, data acquisition and processing. The proposed system has a fuzzy filter which has the parallel fuzzy inference mechanism, fuzzy mean process, and a fuzzy composition process.

Threshold function is works based on frequency level and timing sequences at cut-off level. Non-uniform band of filters are designed using reconstruction filters (low pass G0, high pass G1).

D. System Generator

Xilinx simulink design is transformed to HDL programming within Xilinx software. It is used to configure the simulink design to Xilinx process for calculating the speed, time performance and complexity.

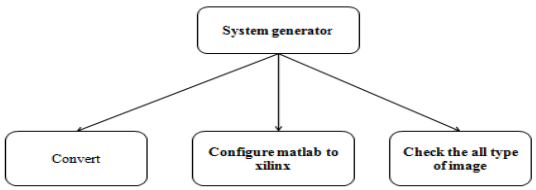

Fig.3 System generator

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E. Xilinx Hardware process

Xilinx system generator simulink design creates the hardware package function and checks all type of signal processing Xilinx blocks for binary based edge detection hardware architecture. Finally, we simulate and synthesis the hardware architecture.

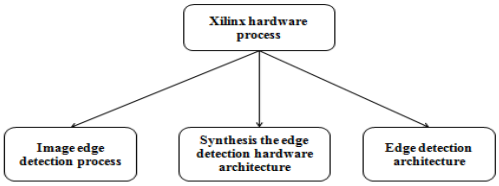


Fig.4 Xilinx hardware process

The flow diagram (fig.3) gives the full information about the process how the isolation of data into frequency components is done and matched the each component with resolution to the scale. Then each process will explained in modules descriptions.

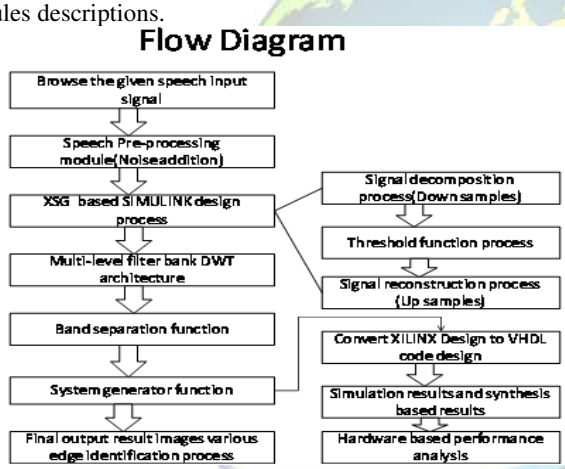


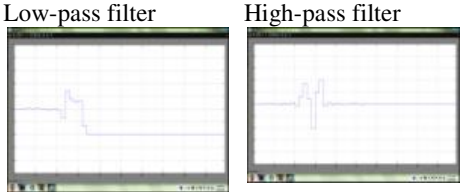
Fig.3 Flow diagram of Proposed system

III. EXPERIMENTAL RESULTS

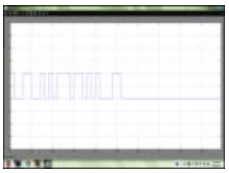
The proposed design contributes the three tools like Matlab,simulink and Xilinx tool. We can get the input signal through matlab and noise is removed using Xilinx simulink design. the simulink design is converted to VHDL code using system generator.this work is used to compute and optimize the filter processing speed and time. The below diagram shows that results of three stages of DWT (Discrete wavelet transform) algorithm.

Stages | Low-pass filter | High-pass filter

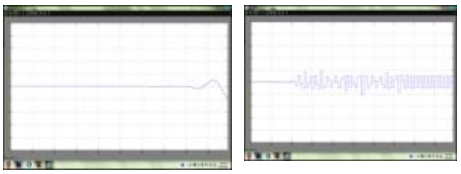
Decompositio n stage



Threshold function



Reconstructio n stage



Combined output

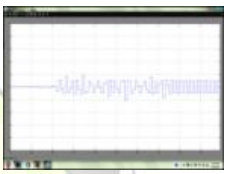


Fig.6 output results for DWT algorithm

The FPGA-simulink based mulitilevel filter bank architcture for signal denoise was designed with less delay (0.853ns) and enchance the speed in 1171.78Mhz. this has been done by utilizing the slice register's and slice LUT's in range of 111 and 152 respectively.

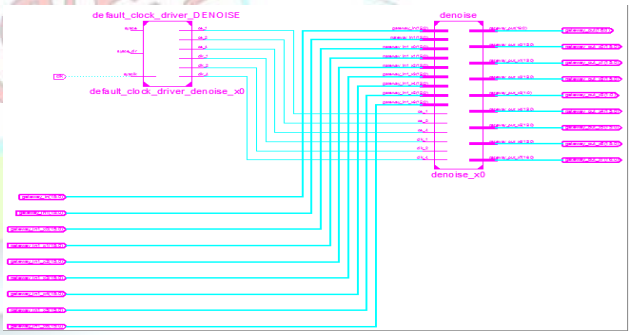


Fig.5 RTL schematic diagram

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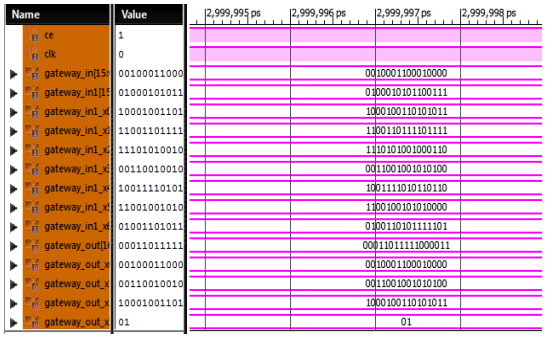

Fig.7 Simulation result

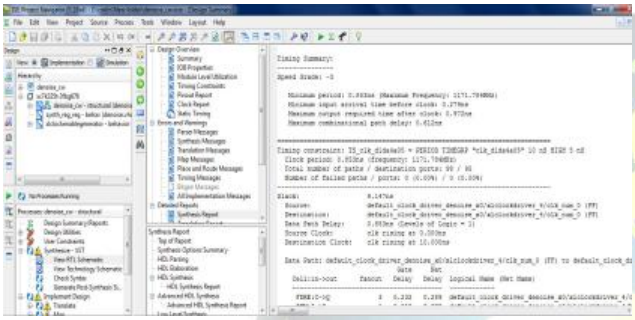

Fig 7. Synthesis report

Table 1 shows that the design summary of xilinx simulink design

Resources	Used	Available	Utilization
Slice registers	111	407,600	1%
Slices	152	50,950	1%
Slice LUT's	212	203,800	1%
IOB's	277	400	69%
Clock period(ns)		1.745	

Table 1 Design summary

Comparison Table

Parameter	Existing System	Proposed System
Speed(MHz)	104	1171.78
Delay(ns)	4	0.853
Latency(ns)	0.134	1
Additions & Subtractions	118(M=L=24)	2

Table 2 Comparison table

IV. CONCLUSION

In this architecture, FPGA- simulink based multilevel filter bank discrete wavelet transform design was designed. This proposed design provides the major advantage that had fewer multiplications, fewer coefficients, less group delay and less matching error than recent approaches. overall,the proposed method would be more suitable for future system integrations and hearing aid applications.

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