ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 10, March 2017

UTILIZATION OF QCA BASED FLIP FLOPS TO DESIGN FREQUENCY DIVIDERS

J.Padma Selvi[1]
PG Scholar
ME VLSI Design, Department of ECE,
PSN Engineering College,
Tirunelveli, India
padmaselvi.j@gamail.com

P.Shyni[2]
Assistant Professor
ME VLSI Design, Department of ECE,
PSN Engineering College,
Tirunelveli, India
shyni260788@gmail.com

***ABSTRACT*:** As CMOS technology has a scaling limitation in deep nanometer technologies, the best alternative for CMOS technology is a Quantum – Dot Cellular Automata (QCA) technology. Quantum dot Cellular Automata has the combined nature of both quantum mechanics and cellular automata. The QCA technology has many advantages than transistor based technology such as small size, high speed, and low power consumption. The working principle of QCA technology is at the molecular level. In conventional CMOS technology, transistors are used to create a logic gate. But in QCA technology, QCA cells are used to create logic gates and wire. The basic logic elements are an inverter and the majority gate. By using these elements many of the combinational and sequential circuits are created. In brief, we propose the frequency divider using flip flops. T flip flop, D flip flop, JK flip flop based frequency dividers are implemented using the above mentioned QCA technology. The layout was designed and the functionality of the frequency divider circuit was verified using QCA Designer tool.

Keywords: Quantum-dot cellular automata, Sequential circuits, frequency dividers

I. INTRODUCTION

According to the Moore's law, as the year, increasing the size of the chip will be decreasing [1]. This prediction of Moore's law will become true in CMOS based VLSI circuit design. But now a day CMOS –VLSI technology has a scaling limitation in deep nanometer technology. To overcome the physical limitation of MOSFET based VLSI circuit design, such as tunneling currents, sub-threshold leakage, quantum effects, fabrication cost, interconnect delay, the researchers found a new technology that uses both quantum mechanics and cellular automata. The best replacement of the CMOS based VLSI technology is a Quantum-dot Cellular Automata (QCA). This is a new kind of computing paradigms that operating at the quantum level. We have implemented automation physically using with the quantum-dot cells in 1993. In 1997, QCA cell was first fabricated [2]. The QCA has a small cell which contains a four quantum dots with two free electrons. These dots are connected via tunneling barriers and the electrons are allowed to move through the barrier between the quantum dots. The size of the cell can be in a nanometer range. Thus the area occupied by the QCA circuit will become very low. And the switching speed of the cell is very fast. Therefore the speed of the QCA device is approximately high. Here the binary values are encoded in the polarization state of the cell that is the charge configuration of the cell, not by the current switches. Thus the power consumption of the QCA device is extremely low.

The digital electronics are divided into two main categories. They are combinational circuits and sequential circuits. In QCA both the circuits are implemented. The combinational circuits are directly implemented in QCA with the same Boolean logic functions used in the conventional CMOS circuits. In sequential circuits, the conventional CMOS circuits are not directly implemented in QCA circuits. Thus the truth table of sequential circuits is identified and then the Boolean logic equations are derived. Then the sequential circuits are designed.

II. BASICS OF QCA

A. QCA CELL

The Fundamental element of QCA technology is a QCA cell. That can be used to design Logic gates, wires and memories. The cell has a structure of the square and the potential walls are located at four corners of a QCA cell shown in Fig. 1. In a QCA cell, exactly two electrons are locked in and they can be residing only in the potential wells. The potential wells are connected with electron

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 10, March 2017

tunnel junctions shown in Fig. 2. The tunnel junction can be opened for the electrons to travel through them under a particular condition, given by a clock signal. Without any interaction from outside, the two electrons will try to separate from each other as far as possible, due to Coulomb force that interacts between them. So the electrons will be located diagonally inside the potential wells, because the diagonal is the largest possible distance for them to reside [3].

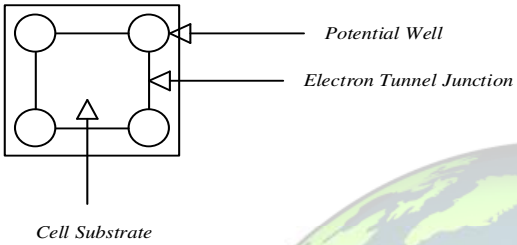

Fig.1. Anatomy of QCA cell

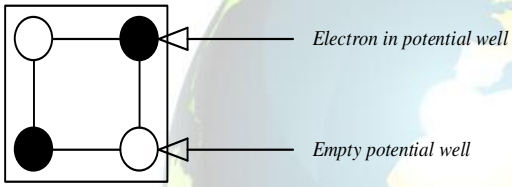

Fig.2.Electrons in potential well

There are two polarization states in QCA cell that can be used to represent binary information i.e., binary "0" and binary "1" shown in Fig. 3.

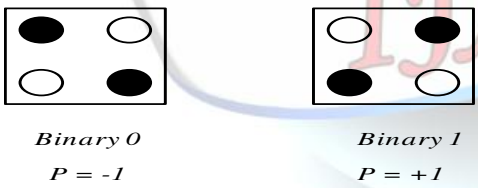

Fig.3. Binary representation of QCA cell

There are some special arrangements of cells called symmetric cells where the four wells are not in the corners of the cell but in the middle of the edges shown in Fig. 4.

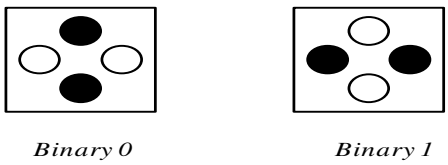

Fig.4. Symmetric QCA cell

B. QCA WIRE

The QCA wire is just an array of QCA cells through which the information is passed from one point to another point. To maintain the flow of information correctly through the wires, we must give the proper clock signal. In an ordinary QCA wire the same polarization state is carried which is shown in Fig. 5. But if the symmetric cells are used to create a QCA wire which carries opposite polarization state of the cell shown in Fig. 6 [4]

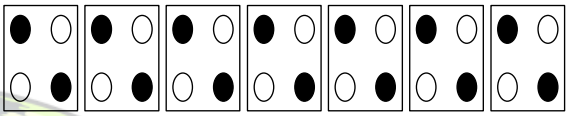

Fig.5. QCA Wire using ordinary QCA cells

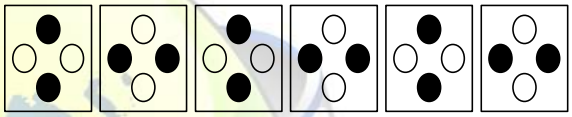

Fig.6. QCA Wire using symmetric cells

C. LOGIC GATES IN QCA

A digital circuits having one or more inputs and only one output which is based on some logic is known as logic gate. Logic gates are required to build arithmetic circuits. The fundamental logic gates used in QCA are the inverter and the majority gate.

The Inverter

The inversion is the most basic operation in digital electronics. The truth table for an inverter is shown in Table I. Here if the input is logical 0, then the output will be logical 1 and vice versa. The logic gate symbol and the QCA layout diagram will be shown in Fig. 7.

Input	Output
1	0
0	1

Table 1: Truth table for an Inverter

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 10, March 2017

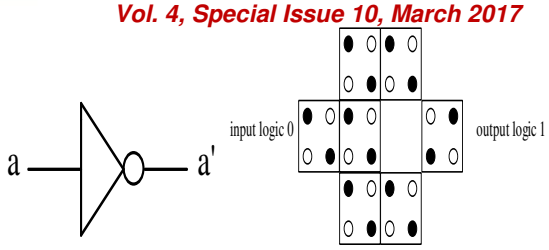

Fig.7. Logic gate symbol and the QCA layout diagram for inverter

The Majority Gate

The majority gate operates with the majority voter logic. The equation that governing the majority logic is M (a, b, c) = ab + bc + ca. Where a, b, c are the inputs. And the output M (a, b, c) is generated by the center cell. The center cell is the device cell. This device cell gets the polarization state according to the majority of the 3 input cell states. The truth table for the majority gate is shown in Table II. And the logic gate symbol and their layouts are shown in Fig.8. By setting any one input of the majority gate with a constant value, we get the basic gates such as "AND" and "OR" gates.

a	b	c	M(a, b, c)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 2: Truth Table for the Majority Gate

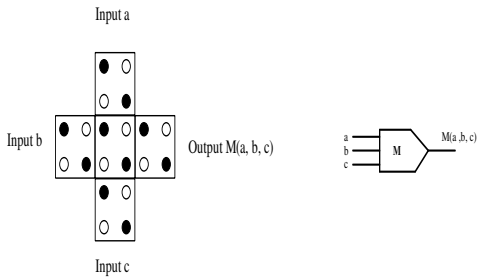

Fig.8. Logic gate symbol and the QCA layout diagram for the majority gate

The logical AND function is obtained from the majority gate by setting any one of the input by zero. The layout and symbolic representation of AND gate is show in Fig. 9. The logical expression for AND gate is

$$a \,.b = M(a, b, 0)$$

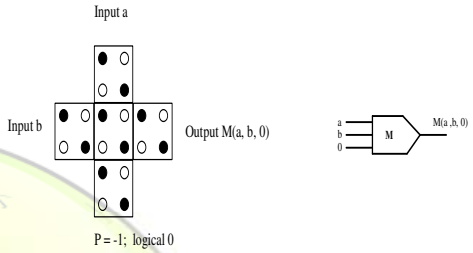

Fig.9. QCA AND gate

The logical OR function is obtained from the majority gate by setting any one of the input by one. The layout and symbolic representation of OR gate is show in Fig. 10. The logical expression for OR gate is

$$a + b = M\,(a, b, 1)$$

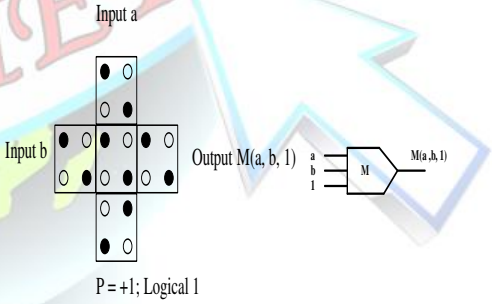

Fig.10. QCA OR gate

D. CLOCKING IN QCA

The QCA clocks are areas of conductive material under the automation's lattice. The clocks are used to modulating the electron tunneling barriers which is in the QCA cell. The main purpose of QCA clock is powering the automation lattice and to controlling the data flow direction. When the clock signal is high it lowers the electron tunneling barrier and the electrons are free to move. Here the cell is in an unpolarized state. When the clock is low it higher the electron tunneling barrier and the electrons are in

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 10, March 2017

stable state and the cell maintain the finite polarization state. To maintain the correct flow of information through the QCA wire is done with help of QCA clock. In QCA one clock cycle has four clock signals with equal clock frequency which are delayed by ¼ of whole clock cycle among each other are shown in Fig. 11.

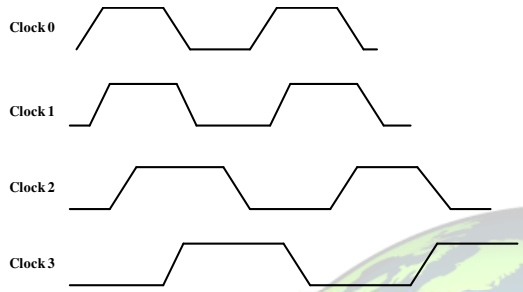

Fig.11.Four shifted clock signals

Each clock signal has four clock phases. These phases are used to maintain the stable state of the system. Thus the four phases shown in Fig. 12 corresponds to clock signal are

1. Switch phase
2. Hold phase
3. Release phase
4. Relax phase

At the starting of the switch phase the tunneling barrier is in low potential and the cells are in unpolarized state. During the switch phase, the tunneling barriers are raised gradually. Then the extra electrons in a cell are polarized under the influence of neighboring cells. In this phase, a cell attains a definite binary value. In the hold phase, the interdot barriers are raised. So the electrons do not switch and retain their polarity. In release phase, the interdot barriers are reduced and the cell loses their polarity. In relax phase, there is no interdot barrier and keep the cell in an unpolarized state.

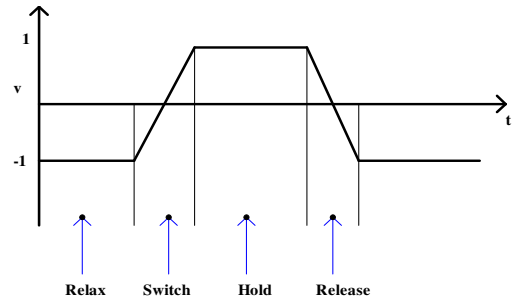

Fig.12. Clock Signal with 4 phases

E. QCA TOOLS

QCA Designer is the most important layout tool which is used to design and simulate the layout for quantum dot cellular automata. This tool gives most accurate results then other tools such as AQUINAS, QBert. [5] The QCA Designer has two types of simulation type. [6] They are

- Exhaustive verification
- Vector table

In exhaustive verification simulation type, all possible combinations of the input vectors will be simulated automatically. If we have 'n' input, then all 2^n input state will be simulated in increasing order. But in vector table simulation type, we have to specify the input vectors. QCADesigner has two types of simulation engines. They are

- Bi-stable simulation engine
- Coherence vector simulation engine

In bi-stable simulation engine, the simulation is done faster. This engine assumes that each cell is a simple two-state system. The coherence vector simulation engine works slower than bi-stable simulation engine but gives more accurate results.

III. FREQUENCY DIVIDER

A frequency divider is a circuit that takes an input signal of a frequency f_{in} and generates an output signal of a frequency f_{out}.

$f_{out} = f_{in} / n$ where,''n'' is an integer.

Frequency dividers are used for both analog and digital applications. Analog frequency dividers are used only at very high frequencies. Digital dividers can work up to tens of GHz. The flip flops are also used to divide the frequency of a periodic waveform.In fact, depending on the frequency that needs to be divided, different approaches can be used in this QCA technology. In QCA frequency dividers are constructed by using flip flops and the way in which they can be looped in a circuit. Here the divide- by- 2 circuits are implemented by using the flip flops such as T flip flop, D flip flop and JK flip flop[7]. A frequency divider is the circuit that takes the input signal of a frequency f_{in} and generates an output of the frequency f_{out}.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 10, March 2017

Here the negated output of the flip flop is connected back to the T input of the flip flop. Thus it produces the output as just one half of the input digital signal. The output changes with respect to the input, only during the negative edges of the input. There will be no change in the output during the positive edges of the input.The block diagram for the frequency divider using T flip flop design is shown in Fig. 13.

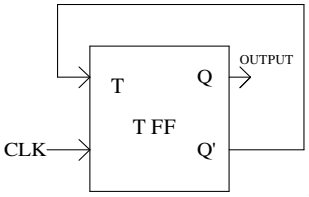

Fig.13. Divide-by-2 frequency divider using T flip flop

The D flip flop is a very versatile circuit. It can be used in many areas where an edge triggered circuit is needed. The negated output of the second flip flop is connected back to the input terminal of the both flip flops. The first flip flop produces the output as the normal data output as in a given input. The output state changes with respect to the input, only during the negative edges of the input state. There will be no change in the output during the positive edges of the input[12]. The block diagram for the frequency divider using D flip flop design is shown in Fig. 14.

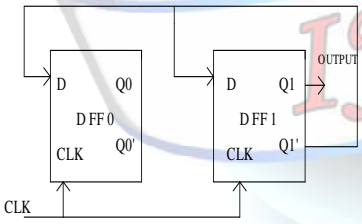

Fig.14. Divide-by-2 frequency divider using D flip flop

Here, the J input terminal of the flip flop is as set as one always and the positive output of the flip flop is connected back to the K input terminal. And the input clock pulse is applied to the clock input. The output state of the flip flop changes with respect to the input state of the clock signal during the negative edge.[16] Thus the configuration of the JK flip flop gives the output frequency as half of the input frequency. The block diagram is as shown in Fig. 15.

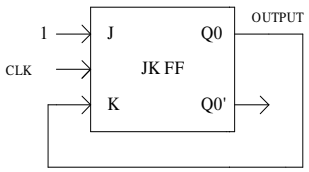

Fig.15. Divide-by-2 frequency divider using JK flip flop

The QCA implementation of these frequency dividers using T flip flop, D flip flop and JK flip flop are shown in Fig. 16, Fig. 17 and Fig. 18. And the corresponding simulated results are shown in Fig. 19, Fig. 20 and Fig. 21.

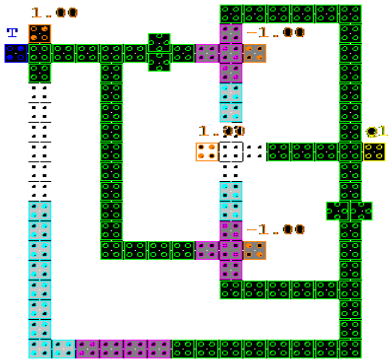

Fig.16. Layout for frequency divider using T flip flop

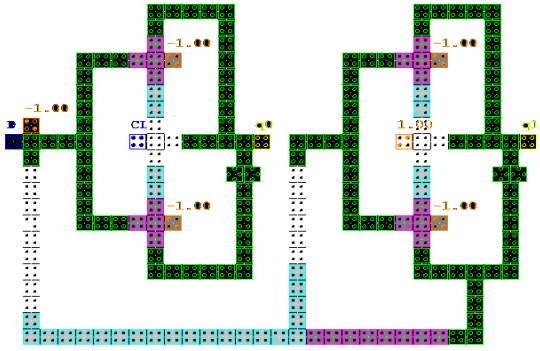

Fig.17. Layout for frequency divider using D flip flop

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 10, March 2017

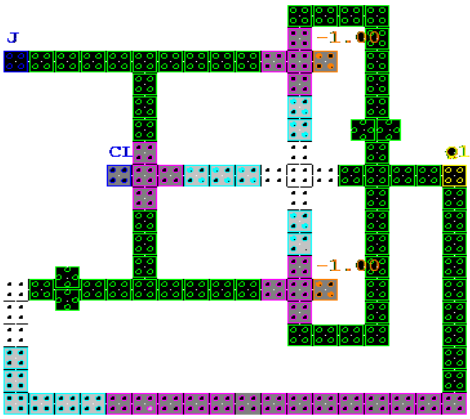

Fig.18. Layout for frequency divider using JK flip flop

Fig.19. Result of frequency divider using T flip flop

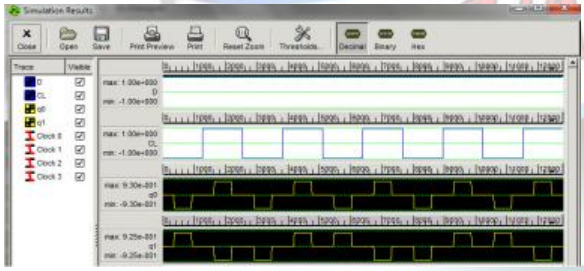

Fig.20. Result of frequency divider using D flip flop

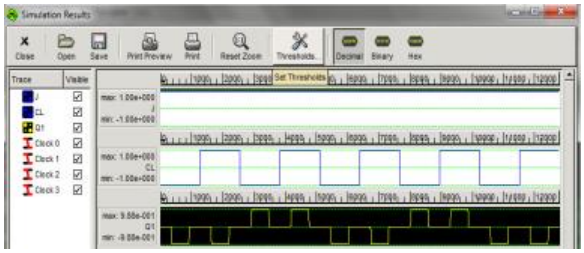

Fig.20. Result of frequency divider using JK flip flop

The total size and the number of QCA cells used to design the frequency divider using T flip flop, D flip flop and JK flip flop circuit will be given in the below Table 3.

Circuit	Area	Number of cells
Frequency divider using T flip flop	0.12 μm^2	102
Frequency divider using D flip flop	0.25 μm^2	193
Frequency divider using JK flip flop	0.19 μm^2	121

Table 3: Frequency divider Design- Area and Number of Cells

IV. CONCLUSION

Thus the frequency divider using T flip flop, D flip flop and JK flip flop was design in QCA. And the functionality of that frequency divider circuit using T flip flop, D flip flop and JK flip flop was verified using QCA Designer tool. Totally 102 cells are used to create the frequency divider circuit using T flip flop and obtain the area of 0.12μm^2. Likewise, frequency divider circuit using D flip flop uses 193 cells with area 0.25μm^2 and the frequency divider circuit using JK flip flop uses 121 cells with area 0.19μm^2

ACKNOWLEDGEMENT

I thank the almighty god for endowing me with the immense blessings that helped me in every step of my progress to complete this project successfully. I am greatly indebted to my guide **Mrs.P.Shyn,** Assistant Professor, ECE department, without whom this entire project would be unthinkable source of knowledge. I would like to express my thanks to my most beloved **parents and friends** whose continuous support and encouragement all the way through the course has led to pursue the degree and complete the project confidently. Finally I extend my sincere thanks to one and all who helped me for my work with their valuable advices and constant inspiration which enabled to complete my project successfully in time.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Special Issue 10, March 2017

REFERENCES

[1] D. Grier, "The innovation curve [Moore's Law in semiconductor industry]" computer, vol 39, pp. 8-10, feb 2006.

[2] C. Lent, P. Tougaw and W. Porod, "Quantum Cellular Automata: the physics of computing with arrays of quantum dot molecles", in physics and computation, 1994. Phycomp'94, proceeding..workshop on pp. 5-13, Nov 1994.

[3] Rahul Singhal "Logic Realization Using Regular Structures in Quantum-Dot Cellular Automata (QCA)" A Thesis, January 2011.

[4] Heumpil Cho and Earl E. Swartzlander "Adder Design and Analyses for Quantum-Dot Cellular Automata," IEEE Trans. Nanotechnology, vol. 6, no. 3, pp. 374–383. May 2007.

[5] Timothy J. Dysert "Defect Properties and Design Tools For Quantum-Dot Cellular Automata" A Thesis, July 2005.

[6]QCADesigner Documentation [online].Available http://www.qcadesigner.ca.

[7]Salivahanan.S and Arivazhagan.S (2007) "Digital Circuits and Design" 3rd Edition, Vikas Publishing House pvt. ltd.

[8] Lee Ai Lim, "Sequential Circuit Design Using Quantum-Dot Cellular Automata (QCA)" IEEE Conf. Circuits and Systems, pp. 162-167, October 2012.