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EMERGING NESTED NEUTRAL POINT CLAMPED MULTILEVEL INVERTER FOR TRACTION APPLICATION

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Abstract-- **In this project using of a newly voltage balancing NNPC inverter had been developed. This output is utilized in the transportation industry to adopt the multilevel inverter-based propulsion systems. In this proposed work space vector pulse width modulation (SVPWM) technique is used, this technique is very efficient and eliminate unwanted harmonics from the output voltage over than other PWM technique. This PWM method is easy to implement and a very few reckoning. This inverter module having back-to-back clamped diode, voltage modulation operation thus to achieve a voltage regulation and high efficiency at any loading condition. Multilevel inverters are very popular in medium-voltage power conversion such as motor drives, power conditioning devices, renewable energy generation and distribution because of low voltage stress on switching devices, better harmonic reduction, low switching frequency, and less switching losses.Due to the presence of these elements the inverter can operate normally and the voltage stress is shared uniformly to all switching devices and capacitor voltage should be controlled. Thus results overabundance of switching states. The cogency and results of the proposed topology is verified by simulation. That inverter design is help to reduce the harmonic in normal and that result was analysis in MATLAB SIMULINK model**.

KEYWORDS:Nested neutral point clamped inverter (NNPC), Space vector pulse width modulation (SVPWM).

I. INTRODUCTION

Power Electronics is the art of converting electrical energy from one form to another in an efficient, clean, compact, and robust manner for convenient utilization.The simplest dc voltage source for a VSI may be a battery bank, which may consist of several cells in series-parallel combination. Solar photovoltaic cells can be another dc voltage source. The PWM converters have a dramatically low working efficiency levels at high auxiliary resonant circuitry during the switch transition period to achieve zero-current switching (ZCS) for the IGBT switches

An Inverter is basically a converter that converts DC-AC power. Even though input to an inverter circuit is a dc source, it not uncommon to have this dc derived from an ac source such as utility ac supply. Thus, for example, the primary source of input power may be utility ac voltage supply that is converted, to dc by an ac to dc converter and then inverted back to ac using an inverter. The metal-oxide-semiconductor field effect transistor is a type of transistor used for amplifying for switching electronics signals. This topology is has raised the competition bar for working efficiency of the inverters used in the rail transit industry to above 98% from the traditional 92% achieved by the hard-switched two-level pulse width-modulated (PWM) inverters. The metal-oxide-semiconductor field effect transistor is a type of transistor used for amplifying for switching electronics signals. Structure of 3-level NPC. The DC bus voltage is split into 3 levels by using 2 DC capacitors, C1 and C2. Each capacitor has Vdc/2 volts and each voltage stress will be limited to one capacitor level through clamping diodes The metal-oxide-semiconductor field effect transistor is a type of transistor used for amplifying for switching electronics signals Structure of 3-level NPC. The DC bus voltage is split into 3 levels by using 2 DC capacitors, C1 and C2. Each capacitor has Vdc/2 volts and each voltage stress will be limited to one capacitor level through clamping diodes To implement space vector pulse width modulation ,a reference signal Vref is sampled with frequency fs(ts=1/fs).the reference signal may be generated from three separate phase reference using the fourier transforms. Space vector pulse width modulation is an algorithm for the control of pulse width modulation. It is used for the creation of alternating current waveforms most commonly to drive three phase AC powered motor at varying speeds from DC using multiple class-d amplifier Voltage imbalance that occurs in the series stacking capacitor has being investigated and comparison study of the performance of each types of multilevel inverter such as the Neutral-Point-Clamped (NPC), Flying Capacitor (FC) and h-bridge cascaded (HBC) has also being performed and analyzed. The small footprint of the proposed multilevel inverter is a good fit for some applications where powering from either an overhead system or a wayside

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rail is desired (like the transit system in Guangzhou, China). The isolation circuit is designed for a smooth transition between the overhead catenary and the wayside rail. Simulation model was built in PSIM with the parameters calculated through transit Studio software as explained in the following section and results will be reported after the design section. The proposed idea is very simple to implement without the need to do very rigorous mathematical work as in. A very systematic approach was presented in to minimize the harmonics but with a trial and error process for the modulation index, which is tricky

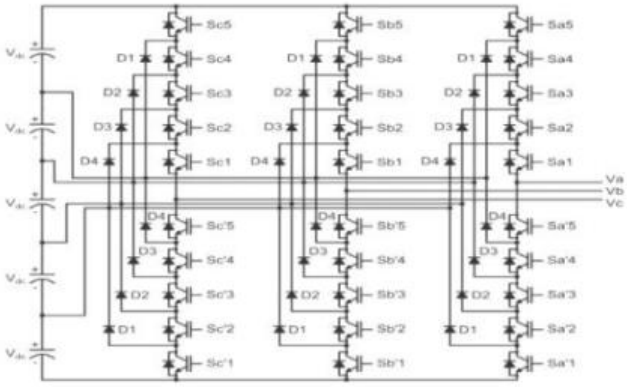
II IMPROVED NESTED NEUTRAL POINT CLAMPED INVERTER

A Circuit configuration and operation:

The width of this pulses are modulated to obtain inverter output voltage control and to reduce its harmonic content. Sinusoidal pulse width modulation or SPWM is the mostly used method in motor control and inverter application SPWM or sinusoidal pulse width modulation is widely used in power electronics to digitize the power so that a sequence of voltage pulses can be generated by the on and off of the power switches. The pulse width modulation inverter has been the main choice in power electronic for decades, because of its circuit simplicity and rugged control scheme SPWM switching technique is commonly used in industrial applications SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. In propose we achieve the draw backs of existing system and compare to the result with exiting method. In proposed three phase, six switch, full-bridge inverter is used to reduce the harmonic level. The SVM technique based PWM very help full to making the switching pulse with better perform output. In this paper, constant switching frequency and variable switching frequency based on carrier pulse width modulation methods are presented and compared. A new modulation method called trapezoidal triangular multi carrier (TTMC) SPWM is implemented and compared with other methods. This new modulation method gives advantages in multilevel inverter to minimize the percentage of total harmonic distortion (THD) and to increase the output voltage. The structure is made up of three modules.

B. Operation:

Module 1 is the conventional full-bridge circuit whose switches are utilized to generate the maximum and minimum voltage levels in the line-to-line waveform. Module 2 is composed of three bidirectional switches in which each of them represents each phase. In other words, each switch functions in the normal mode in the sense that it is exclusively employed for a particular phase. Module 3 comprises a string of bidirectional switches which are connected to DC sources. The switches are made to operate in optimized mode in a way the operation of each switch is divided among three phases.



Various modulation techniques have been used for multilevel inverters. These include those of low-frequency-based methods such as selective harmonic elimination and space vector control. Other competitive methods involve high switching frequency such as multicarrier pulse width modulation (PWM). In this work, one of the most preferred PWM strategy known as the space vector PWM is employed. This section presents the description about how the space vector PWM is adapted for the proposed five-level inverter. Computer simulation is carried out as the first step to examine the performance of the proposed multilevel inverter. For this purpose, a simulation model of the five-level inverter is developed in MATLAB/SIM ULINK environment. V dc is set to be equal to 50 V. The modulation scheme described in the previous section is used for the control with a sampling frequency of 3.3 kHz. A Y-connected RL load is considered with the following values: R = 30.5 Ω per phase and L = 68 mH per phase.

Vo=Vo1+Vo2+Vo3+….Von…(1)equ

Vomax=(2n-1)vdc if vj=2j-1 vdc for j=1,1…n….(2)equ

Vo=Vvdc+(n-1)/2 V2vdc+(n-1)/V3vdc…(3)equ

If n=odd number n=3,5…….

Vo=Vdc+n/2V2vdc+(n/2-1)V3vdc…..(4)equ

If n=even num n=2.6…..

The reference voltage vector is set at 90% of the maximum value. Here, the maximum value is de fined as the radius of largest circle that can be formed within the vector hexagon. In Common Mode Voltage The multilevel inverters produce common mode voltage, reducing the stress of the motor.

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Multilevel inverters can draw input current with low distortion Switching Frequency The multilevel inverter can operate at both fundamental switching frequencies that are higher switching frequency and lower switching frequency. It should be noted that the lower switching frequency means lower switching loss and higher efficiency is achieved. Reduced harmonic distortion Selective harmonic elimination technique along with the multi level topology results the total harmonic distortion becomes low in the output waveform without using any filter circuit.

Nstep=2n+1

Vomax=n*vdc

Nstep=5n-2 if n=odd number

Nstep=5n-3 if n=even number

Vomax=(5n-2)/2vdc if n=odd…..(5)equ

Vomax=(5n-3)/2vdc ifn=even…(6)equ

III INPUT DESIGN PROCEDURE:

All voltage source of inverters assume stiff voltage supply at the input. The first topology introduced the series H-bridge design. This was followed by the diode clamped converter can utilized a bank of series capacitors. Another multilevel design involves parallel connection of inverter phases designs have also emerged some involving cascading .These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. Recent advances in power electronics have made the multilevel concept practical. In fact, the concept is manufactured have obtained recent patents on multilevel power converters and associated switching techniques. It is evident that the multilevel concept will be a prominent. Moreover, modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM),selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. In addition, many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, Universal Power All voltage source of inverters assume stiff voltage supply at the input. The first topology introduced the series H-bridge design. This was followed by the diode clamped converter can utilized a bank of capacitors..These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. Recent advances in power electronics have made the multilevel concept practical. In fact, the concept is so advantage manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. It is evident that the multilevel concept will be a prominent. Moreover modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM),selective harmonic elimination (SHE-PWM), space vector modulation (SVM), and others. Conditioner and traction drive systems. Speed control is an essential feature in crane drives. It is required for allowing soft starting and stopping of the travel motions for enabling its correct positioning of load. For the lifting drive the speed control in a wide speed range, from zero to nominal values, is required.

Switches states	V_{out}						
	-30	.....	-10	0	-10	.....	30
S1	0	.....	0	0	1	.....	1
S2	0	.....	0	1	0	.....	1
S3	1	.....	1	0	0	.....	0
S4	1	.....	1	1	0	.....	0
S5	0	.....	1	0	1	.....	0
S6	0	.....	0	0	0	.....	0
S7	0	.....	0	0	0	.....	0
S8	1	.....	0	0	0	.....	1

Table 1:switch state

During acceleration, kinetic energy is stored in the system. To stop the crane, this energy must be absorbed by the drive. In the indoor situation, this energy is well known and only present for a short period of time. For outdoor applications, the wind forces may become very important The drive must be capable of handling this inverse power direction either by consuming the power in a resistor or preferably by feeding it back to the supply. Speed control is an essential feature in crane drives. It is required for allowing soft starting and stopping of the travel motions for enabling its correct positioning of load. For the lifting drive the speed control in a wide speed range, from zero to nominal values, is required. During acceleration, kinetic

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energy is stored in the system. To stop the crane, this energy must be absorbed by the drive. In the indoor situation, this energy is well known and only present for a short period of time. For outdoor applications, the wind forces may become very important The drive must be capable of handling this inverse power direction either by consuming the power in a resistor or preferably by feeding it back to the supply. SVPWM involves synthesizing the reference voltage space vector by switching among the three nearest voltage space vectors SPWM involves the comparison of a reference signal with a number of level shifted carriers to generate the PWM The two main techniques of PWM generation for multilevel inverters are sine-triangle PWM (SPWM) and space vector PWM (SVPWM) Multilevel SPWM involves the comparison of a reference signal with a number of level shifted carriers to generate the PWM signal.The voltage space vectors of higher level inverter can be generated from the voltage vectors of an equivalent 2-level inverter using simple addition operations. Sector identification and switching vector determination in SVPWM get operations without any computational complexity.

Switches states	V_{out}						
	-60	.....	-10	0	-10	.....	60
S1	1	.....	1	1	0	.....	0
S2	0	.....	0	1	1	.....	1
S3	0	.....	0	0	1	.....	0
S4	0	.....	1	0	0	.....	0
S5	0	.....	0	0	0	.....	0
S6	0	.....	0	0	0	.....	0
S7	0	.....	0	0	0	.....	1
S8	1	.....	0	0	0	.....	0

Table 2:ON switch table

The proposed algorithm doesn't use any look up table for sector identification and switching vector determination. The most common MLI topologies classified into three types are diode clamped MLI (DCMLI), flying capacitor MLI (FC-MLI), and cascaded H-Bridge MLI (CHB-MLI). The hybrid and asymmetric hybrid inverter topologies have been developed according to the combination of existing MLI topologies or applying different DC bus levels respectively. Type I and Type II Type I uses multiple dc voltage sources and Type II uses multiple (split or clamping) dc voltage capacitors. Type I include the traditional cascaded topologies, those presented in and so forth. Type II includes the conventional diode clamped, capacitor-clamped inverters, and the topologies proposed in. In terms of single phase multilevel inverters, the disadvantages of the two types are apparent. Type I suffers from the availability of the multiple dc voltage sources. As the powersemiconductors play role in Multilevel Inverters the proposed system is much reliable, has less control complexity and fewer switches.

High reliability and low electromagnetic interference (EMI) are two important factors for many industrial applications such as air based electric transport system charger (AETSCAs far as the commutation problem is concerned, it is not possible to define a timing which allows to carry out a safe commutation of the load current between two diode bridge switches. However, the commutation process cannot be based on a switching method other than the "make-before-break" or "break-before-make" one. With respect to the circuit scheme, if a make-before-break switching method is used, the on-coming switch is turned on before the off-going switch is turned off. In this way the switches S1 and S2 establish a short circuit path between the two voltage sources V1 and V2. The consequent generated current spikes, if not limited somehow, would destroy the switches. In the case a break-before-make switching method is employed, the dual situation occurs: the off-going switch is turned off before the on-coming is turned on and in this way a path for the conduction of the inductive load current is no longer provided. Destructive voltage spikes are induced on the opened switches. In this switch arrangement separated internal conduction paths exist for the two load current polarities and these paths can be independently controlled. This is a basic feature, which allows, by means of proper commutation strategies, to safely commutate the load current between different bi-directional switches, reducing the switching losses and eliminating any local network requirements. Furthermore, compared to the diode bridge switch, this solution has also the advantage of lower conduction losses, since only two devices are conducting at any given time. Depending on how the two IGBTs are connected a common emitter and a common collector arrangement is possible. The connection mode does only affect some technological aspects of the converter realization, as the number of isolated power supply needed for the gate drive circuits. With common emitter switches an isolated power supply per switch is needed, for a total of 9. With common collector switches, since the emitter of each device is connected to an input or an output line of the matrix converter, the number of isolated gate drive supplies is reduced to six. The last proposed configuration of bi-directional switch and consists of two NPT-IGBTs with reverse blocking capability in anti parallel connection.

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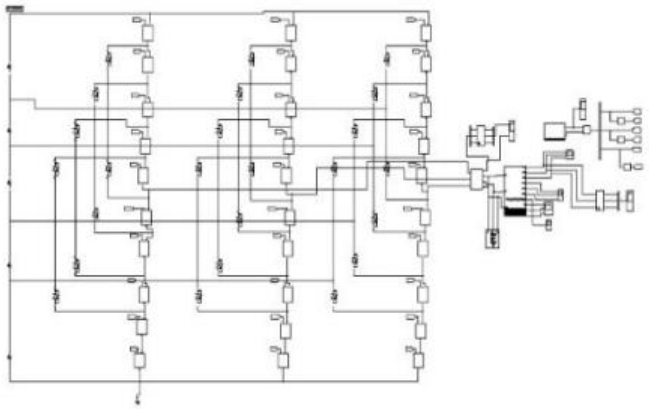
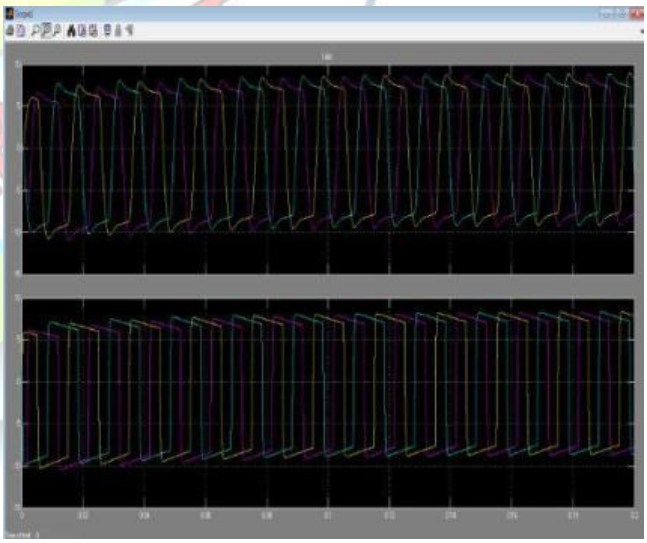
RB-NPT-IGBT stands for reverse blocking NPTIGBTs switches. CCC stands for the anti parallel common collector arrangement with series diode switches. But, for a given rated power of the load, whatever is the AC mains voltage level, the NPTIGBTs switch imposes a lower switching frequency which consequently will lead to the design of a larger input. In this paper, a selective harmonic elimination technique is introduced to cascade multilevel converter. With the switching angles which are found out, it could be obtain that the low order harmonic of the output from the converter is minimize. A simulation model of 9-level H-bridge multilevel converter with sources is engaged to authenticate the method presented in the paper. The results show that the method can in actual fact eliminate the specific harmonics, and the output voltage waveform with low THD as anticipated in theory analysis. In this paper, a selective harmonic elimination technique is introduced to cascade multilevel converter. With the switching angles which are found out, it could be obtain that the low order harmonic of the output from the converter is minimize. A simulation model of 9-level H-bridge multilevel converter with sources is engaged to authenticate the method presented in the paper. The results show that the method can in actual fact eliminate the specific harmonics, and the output voltage waveform with low THD as anticipated in theory analysis. The practical problems related to the implementation of the bi-directional switch and the relevant commutation issues have represented one of the main obstacle to the industrial success of forced commutated direct AC-AC power converters. This chapter, after a brief description of the different possible configurations for the bidirectional switch implementation, focuses the attention on the commutation problem in bidirectional switches realized with two discrete anti-parallels connected unidirectional IGBTs with series diode Most of the existing commutation strategies are reviewed.complexity, size, and cost of the circuit. Thus, reducing the number of power Hybrid cascade multilevel inverters combine semi-conductor devices of different voltage ratings and technologies, which theoretically allow high efficiency to be achieved. Christo Ananth et al.[6] presented a brief outline on Electronic Devices and Circuits which forms the basis of the Clampers and Diodes.Hybrid cascade multilevel inverters combine semi-conductor devices of different voltage ratings and technologies, which theoretically allow high efficiency to be achieved. They one to design single- and three-phase inverters that can be operated either with staircase or with PWMSHE has been often studied based on the assumption of balanced dc levels and single switching per level. This dissertation addresses the further developed harmonics injection and equal area criteria based four-equation method to realize for two-level inverters and multilevel inverters with unbalanced dc sources

IV SIMULATION RESULTS:



A.Output waveform for three phase current with filter:



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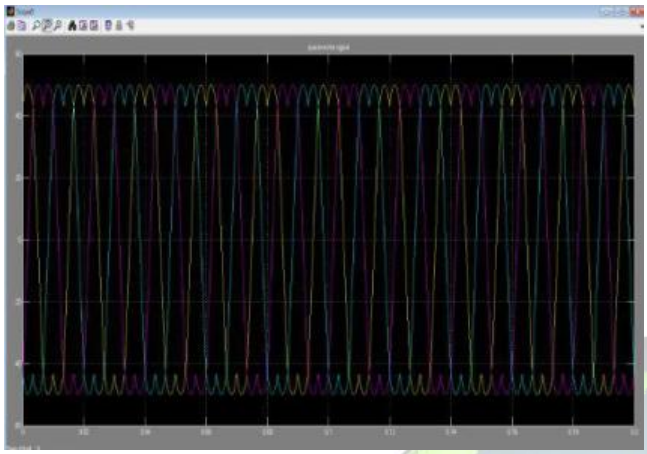
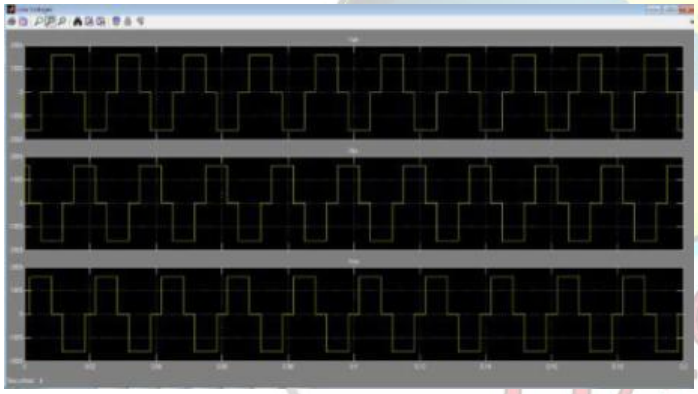
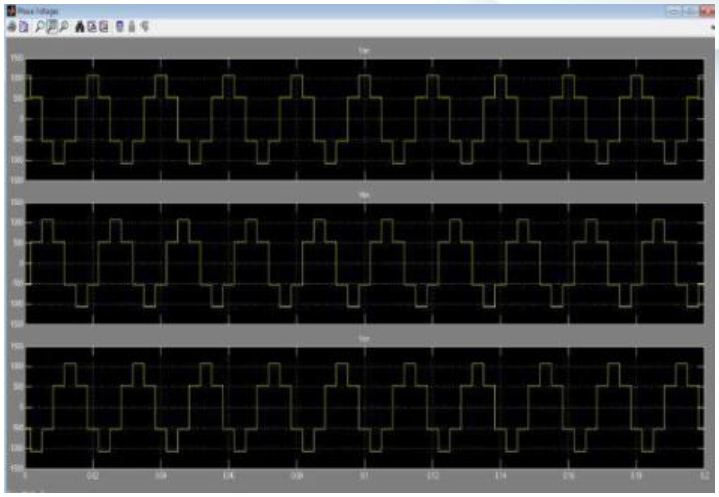
B.Output waveform of control signal:



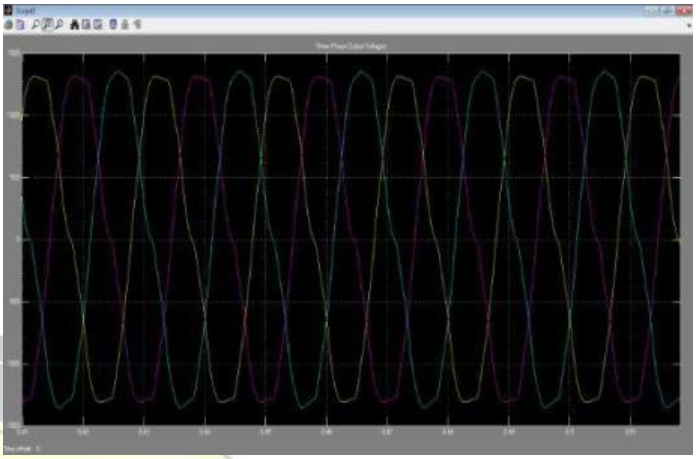
C.Output waveform of line voltage without filter:



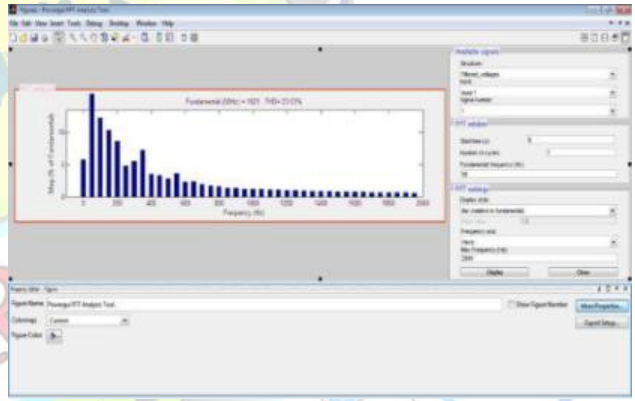
D.Output waveform of phase voltage without filter:



E.Output waveform of three phase line voltage with filter:



F.THD Output of proposed topology:



V CONCLUSION:

For verifying the validity of the proposed multilevel inverter in the generation of the desired output voltage waveform, prototype is simulated based on the proposed topology. This topology is easy and potent logic tables are developed. These harmonics are determined based on the type of the rail system and the inverter topology. The multilevel inverter is adjusted to produce a 50-Hz, 5-level staircase waveform. The parameter selected for testing are (a) L=50mH with R=100Ω (b) R=100Ω(c) Each 5vdc source =100 V. The output waveform of a single phase is shown in fig 1.6 with their corresponding Fourier spectrum. The total harmonic distortion (THD) is one of the measure harmonics in waveform. The SVPWM technique allows for the development of a specific switching pattern for

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every alignment, which guarantees the elimination of the harmonics

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