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LOW POWER CLOCK TREE SYNTHESIS USING CLOCK GATING TECHNIUE

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Abstract:

The Clock Tree Synthesis from the clock gating can enable the clock signals. This technique can be used the clock which place is needed for the operation. The unwanted clock signals are deactivated during the clock gating. The technique can be used in clock tree synthesis in saves the dynamic power consumption of the circuit. The flip-flops are to be using the clock gating technique for power consumption.We are going to design the circuit based on a clock gating which is used for every clock pulses. The clock pulses are enabling from derived the timing signals to be the gated logic is to be save the power from flip-flops. The clock gating technique can also be reducing the delay from the circuit for the achievements of the application level. This method can be applied to specified application level implementation. This architecture can be designed and verified by using TANNER EDA software tool.

Introduction:

The VLSI technology in physical design flow, CTS (Clock Tree Synthesis) is performed in between the placement and routing [1].The clock tree synthesis is an important element in the physical design which control the whole circuit. The goal of the clock tree synthesis is to minimize the skew and insertion delay[1].But the power consumption of clock tree dominate over 40% of the total power over the modern high performance VLSI designs[3].So we reduce the power consumption in using the clock gating technique. The clock gating technique in which place is clock enable in the part is the clock is applied. The clock gating is the clock signals are enabled at the process of system level [4], and it can be effectively identified the functional block modules. The grouping of Flip-Flop is used in a data driven clock gating method [5].The data driven clock gating circuit using clock enabling signals are manually added for every FF as a part of a design methodology [5]. Clock gating is employed at all levels of system architecture, block design, logic design, and gates. Several methods to take advantage of this technique are described, with all of them depending on various heuristics in an attempt to increase clock gating opportunities [7].

Clock gating circuit is power consumed by 50 % of dynamic power. The clock gating reduce dynamic power by combinational logic circuit and then the circuit reduce clock pulse and sharing the clock signal in merging flip-flops and reduce clock signal. The profitable EDA tools are supported clock gating technique. There are two types of clock gating technique. They are flip flop-based clock gating and Latch-free clock gating. The latch-free clock gating technique uses a simple AND or OR .The flip flop-based clock gating technique is a
level-sensitive. In this project using in latch based clock gating technique. The latch-based clock gating
Technique is called Integrated Clock Gate (ICG). The Integrated gated clock will be disables in the next cycle
By XORing the output of the present data input and it will reveal at the output in the next cycle. Then the
Output of the XOR gates are ORed for generating the gate signal for the FF's which is to be used to avoid
The glitches. The Integrated clock gate (ICG) can be used by the environmental tools by the combination of

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Flip flop with the AND gate. These latches could be used in ultra-low power applications for a digital filter.

The data driven clock gating signal are being used as an enabling signals in this applications. There will be a

Trade□off for ICG is the number of clock pulses could be disabled. The pulses could also be a trade-off for

The hardware over-head. While increase the number of flip-flops the hardware overhead decreases to

obtain by ORing the enable signals. The level of this high and the low state of signals could be processed in

the same to give the proper output.

Clock gating techniques:

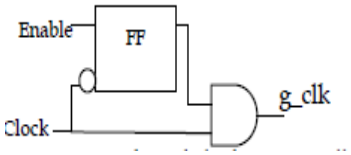
Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power consumption .Clock gating saves power by adding more logic to a circuit to the clock tree.. In synchronous system clock distribution networks consumes a large amount of total power because of high operation frequency of highest capacitance. An effective way to reduce capacity of clock load is by minimizing number of clocked transistor. The clock gating technique has three types,

1. Latch based clock gating
2. Flip-Flop based clock gating
3. Gated based clock gating.

In the three clock gating technique in Latch based clock gating is dynamic power is reduced by 32.28%.And the Gated based clock gating technique in dynamic power is reduced by 27.93%. But the Flip-Flops based clock gating technique is reduce 44.71% the dynamic power consumption. So the flip-flop based clock gating is more efficient consume be less power.

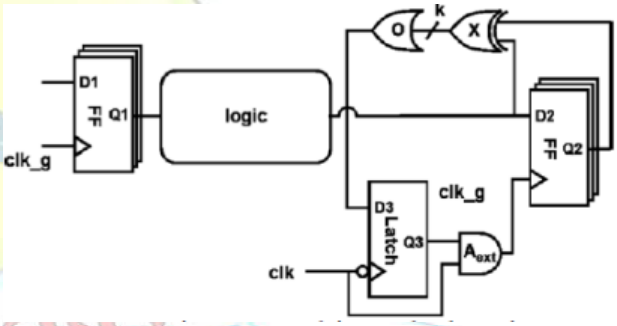
Flip-Flops based clock gating:

In FF based clock gating, FF is used as control element. When the negative edge of clock arrives, change of Enable will be reflected on FF output. If output of FF is high, clock is applied on sequential circuit. The sleep period is longer in FF based clock gating compared to Latch based clock gating. The testability can be easily implemented in FF clock gating and also minimize the skew.



Proposed System:

The dynamic power consumption can be reduced by using the clock gating technique. The clock gating signal enables to have the clock signals. So the flip-flop and the latches are to be enabling by using the gate signals. The output from the X-OR gate is given to the OR gate. The OR gate output is feedback to join the gate signals from the FFs. And the latches are used to avoid the glitches in the presented specified units.



In the figure in the latch and gate is given to the clock gating signal. In the clock gating signal is feedback to the flip-flops. And the logic blocks are used in to which logic is used in to the circuit. The flip-flops given to the logic is the X-OR gate. The X-OR gate is the given input is same, it transfer the clock signal. So used in to the X-OR gate. The X-OR gate in output is the given to the OR gate. The OR gate is feedback to the clock gating. It was the process is continually to the generate the clock signal, to reduce the power in the clock gating signal.

Rising or falling fringe of the modify signal are available in flip-flops, this modifications are done by solely.

But, once the rising or falling fringe of the modify signal, the flip-flop's content remains constant even Though the input modification. in a very typical D Flip Flop, the clock signal perpetually flows into the D flip- flop no matter whether or not the input changes or not. A part of the clock energy is consumed by the interior clock buffer to manage the transmission gates unnecessarily. Hence, if the input of the flip-flop is the image of its output, the shift of the clock will be suppressed to conserve

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power. The auto gated flip-flop design has been illustrated in Fig 3. This block consists of master and the slave combination of flip-flops and the latch. The FF's falling edge of the clock pulse could be gives the time prior of the input signal. The XOR gates are to be highlighting the state of the slave latch when it could be enabled. The sectional view of this latch and the flip-flop can be having the timing constraints when compared to the data driven clock gating. The level of the clock signal enables the pulses from the triggering edges of the input. The gating can be detected to be critical in the
Master slave flip-flop enabling.

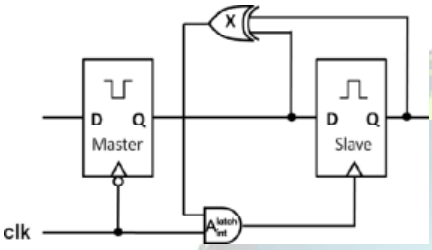

Fig 3: Block diagram of auto gated flip-flop

VI. CONCLUSION

In this paper we have proposed the gated flip flop design with the implementation and
Specific applications. The circuit has been designed and verified by using the T-SPICE compiler (TANNER EDA). The power and delay are compute could be each clock pulses arrived signal. Auto gated flip flop is applied in each clock cycling. The nano meter technology could be adopted as a 45nm process to detect the chip integration level from the analysis. Power is reduced to 44.71%.

RESULT FOR FF BASED CG CELL WITH AND WITHOUT RESET

cell	Area (μm²)	Dynamic power (nW)
FFBased CG Cell	31851.357	1741111.98
FF Based CG Cell with Reset	30996.302	962499.389

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