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VLSI Implementation of Error Correcting Codes and Detailed Assessment of their Peculiarities and Performance

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Abstract: In the contemporary era, the field of communication has achieved greater heights. Within moments data can be sent to any where we want despite of the distance. The signals used for this purpose are either in the analog or digital form. Nowadays the digital communication has shown tremendous growth and all communication channels are slowly switching in to the digital communication. The biggest threat faced by the digital systems are mainly the soft errors or the transient multiple errors mainly caused by the toggling of the bits. Many methods were introduced to detect and to efficiently correct these errors. Such introduced Error Correcting Codes have their own drawbacks. In this paper, some of the commonly used Error Correcting codes are extensively analyzed, studied and implemented using Verilog.

Keywords: Error Correcting Codes (ECC), Decimal Matrix Codes (DMC), Modified Decimal Matrix Codes (MDMC),Encoder Reuse Technique (ERT), Orthogonal Latin Square Codes (OLSC).

I. INTRODUCTION

The digital communication systems have taken a greater leap over the last decade. The technology scales down to the nanotechnology and also the memories are becoming more complex with many advanced electronic systems The major threats to the digital systems are various types of errors like soft errors due to radiations, transient multiple errors etc. Also the rate of errors has increased in the memories. Thus the memories get exposed to the alpha particles or the cosmic rays resulting in single bit or multiple bit errors. To ensure the reliability of the memories, some Error correcting codes are widely used. But these codes require more area, power, and delay overheads. This is because of the complexity of the encoder and decoder circuits. Initially interleaving technique was implemented where the same logical word has been rearranged into different physical words. The tight coupling of hardware structures from both cells and comparison circuit structures made the interleaving method less reliable. Following this was the Single error correcting codes [1] like Hamming codes. But this could correct only single error. Later these codes were extended to the single error correction double error correction codes [2]. These SECDED-DAEC codes were modified later on by adapting some peculiar properties of the Orthogonal Latin Square Codes [3] and Golay codes [4]. Afterwards the matrix codes based on the hamming codes were introduced. Matrix codes successfully reduced the decoding delay. However the number of redundant bits required was elevated. To reduce this Decimal Matrix [5] codes were designed.

The basic error correcting codes comprises of an encoder and a decoder units. The encoder unit generates the required redundant bits according to the Error correcting scheme that is being used. Once the redundant bits are generated, then the digital information is transmitted or stored in the memory [6]. During the decoding, the previously generated redundant bits are compared with the newly calculated redundant bits. Any mismatch in the redundant bits indicates the presence of an error. In order to correct these errors an error locator and error correction units are also employed. The error locating unit identifies the error location through the proper processing of the redundant bits. The error correcting circuit corrects the errors and retrieves the initial digital data lucratively. The encoding and the decoding units require an encoder circuit in order to generate the redundant bits. This makes the circuit complex. To reduce the complexity the Encoder Reuse Technique was introduced, where the same encoder is reused in the decoding section [6].

This paper is mainly a review on various commonly used error correcting codes and their advantages and disadvantages. All these discussed error correcting codes has

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been implemented using Verilog and their properties are comprehensively premeditated.

II. Error Correcting Codes

This section is dedicated to cover the idea of the basic error correction mechanisms that are often used in the storing and communication systems.

A. Basic Hamming Codes Method

In the case of the basic Hamming codes, an error is located with the help of the parity check bits. The parity check bits are generated with reference to the digital data bit positions. For example, in case of a 4 bit data, 3 parity check bits are required. Whereas a 5 bit data requires 4 parity check bits. This code can correct only single errors. In order to make the hamming code efficient enough to correct single errors and detect double errors, an additional check bit is added at the end of the word which will consider all the data bits. The other check bits will compare only particular bit locations.

In case of a 3 bit data, the generation of parity bit is explained below. Table I gives the bit representation of the locations and the Table II gives the parity bit and data bit arrangement in the word.

TABLE I
BIT REPRESENTATION OF LOCATIONS

B1	B2	B3
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

TABLE II
BIT POSITIONS IN A WORD

P1	P2	D3	P4	D5	D6	D7

The parity check bit P1 is generated comparing the data positions 1,3,5,7. In all these locations, the B3 is logically 1. The parity check bit P2 is generated by comparing the locations 2,3,6,7. In these locations, the B2 is logically 1.Similarly the B1 is logically high at the positions 4,5,6,7. Hence the P4 parity check bit compares these positions. This example is of an 4 bit data. The parity check bits for any higher bit word can also be generated in this same method. The word hamming distance refers to the number of bits between two adjacent errors. The rule to determine the number of parity check bits (P) for a N bit data is that $P^2>2N$.

In some cases an additional bit is added at the end of the word for the double error detection purpose. This bit is the parity bit that considers all the bits in that word. Eventually this helps in detecting the double errors in a data. But the double error correction in memory is not possible with the hamming code method [7].

B. Matrix codes

The Single Error Correction Double Error Detection Double Adjacent Error Correction codes commonly known as the SEC-DED-DAEC codes are introduced to overcome the limitation of the previous error correction methods. Here the data is arranged in a matrix and they are grouped in to several groups. From this arrangement, they calculate the parity bits and add these bits in the word itself in an interleaving form. The major disadvantage of these codes was that in some special conditions, the adjacent errors were not successfully detected. Particularly saying, in the cases of adjacent errors occurring at the extreme ends of two groups, the error detection was not possible. The reason for this was the grouping pattern of the data. To overcome this problem, A class of SEC-DED-DAEC codes derived from the Orthogonal Latin Square codes were introduced [2]. Here the properties of the Orthogonal Latin Square Codes [OLSC] were clubbed with the SEC-DED-DAEC codes. This could eliminate the problem created by the grouping of the data.

Another class of matrix code was the Decimal Matrix Codes [DMC]. These codes employs the simple decimal operations such as addition, XOR operation etc for the check bit generation. This scheme of error correction is explained with an example of a 32 bit data. The 32 bit data is converted in to a matrix of 2*4 dimensions. Now along with this we add the Check bits both in the horizontal direction and the vertical direction. The horizontal check bits are calculated by the addition of two 4 bit data. Such 4 bit data are called symbols. Hence the horizontal check bits are generated by the addition of two symbols. Thus by adding two 4 bit data we get 5 bit horizontal check bits along with the carry. Thus for a complete of 32 bit data, we have 8 set of 4 bit data symbols. Thus by adding them we get total of 20 horizontal check bits.

The vertical check bits are calculated by simply carrying out the bit wise XOR operation of the vertical data bits. Thus for a 32 bit data, we have 16 vertical check bits.

Thus the total number of redundant bits are 20+16=36.From this we can conclude that the main limitation of this codes is the higher number of check bits. The main

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reason for higher check bit is the higher number of the horizontal check bits. To reduce this, the horizontal check bits are calculated by the XOR operation of the 4 bit alternative symbols. This block is called the Re-configurable Exclusive Or Logic (Re-AXL). This reduces the number of check bits from 36 to 32.

This system consists of an encoder, a decoder, an error locator and an error corrector. The encoder is reused in the decoder to reduce the complexity of the system. Here encoder receives the data and process the data to generate the horizontal and the vertical check bits. Once the check bits are generated, then the data along with the check bits are stored in the memory or transmitted in the case of data communication systems. This complete process is termed as the write process. Fig.1. shows the DMC encoder unit.

For retrieving the data, the system receives the stored or transmitted data along with the initially calculated check bits. Now the encoder unit is reused to generate a new set of check bits from the received data by the same method. For the easier understanding, this set of check bits are known as the syndromes. Fig.2 shows the DMC Decoder unit.

These syndromes are then compared with the previously calculated check bits. Any mismatch in the check bits refers to the possibility of any errors. The location of the errors can also be deduced by processing the horizontal and vertical check bits together. Then the error corrector corrects the errors by toggling the data at the error locations. This complete process is termed as the read operation.

For the convenience, the encoder system is reused in the decoder system. In order to make this possible, a 2 bit enable signal is employed. Whenever the enable signal is 01, the encoder will carry out the write operation. When the enable signal is 10, the encoder will act as a part of decoder to perform the read operation. Table III gives the enable signals and the corresponding operation of the encoder.

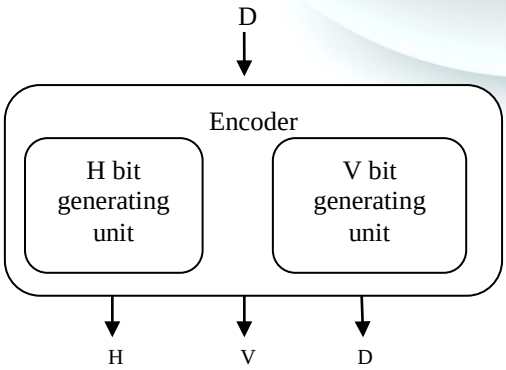

Fig.1.DMC Encoder Unit

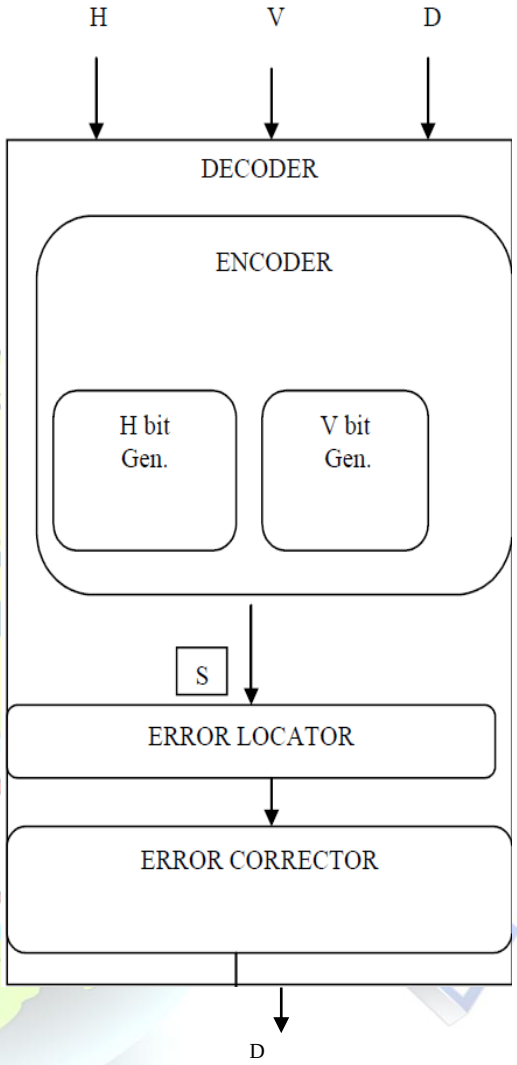

Fig.2. DMC Decoder

TABLE III ENCODR OPERATION

Enable Signal	Encoder Operation
01	Write Operation
10	Read Operation

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III. EVALUATION

Table IV shows the result of the comparison between the commonly used error correcting codes on the basis of the number of redundant bits present. From this table we can deduce that the hamming code requires the minimum number of redundant bits for decoding an 32 bit data. DMC code requires more number of redundant bits and this is reduced in the MDMC codes. This reduction in number of check bits is due to the use of Re-AXL logic.

Considering the area required, the DMC requires around 336 gates for the implementation of error correcting. But in the case of the MDMC, the Encoder Reuse Technique (ERT) is implemented. By this the number of gates required is reduced to 224 gates. Thus the area required also reduces. The chip area thus in MDMC can be recuced about ¼ times as that of DMC.

In terms of the reliability, the MDMC is foremost. The hamming code is the worst option.

TABLE IV
COMPARISON IN TERMS OF REDUNDANT BIT USAGE

SI.NO	ECC	DATA BITS	REDUNDANT BITS
1	Hamming	32	7
2	DMC	32	36
3	MDMC	32	32

TABLE V
PERFORMANCE ANALYSIS

ECC	AREA (μm^2)	DELAY (ns)	POWER (milli watt)
Hamming	58409.1	6.7	132.3
DMC	41572.6	4.9	164.24
MDMC	10393.2	3.2	122.59

TABLE VI
MBU DETECTION COMPARISON FOR VARIOUS ECC

ECC	Number of Error Bits					
Detection (%)	1	2	3	4	8	16
MDMC	100	100	100	100	100	100
DMC	100	100	100	100	100	100
MC	100	100	0	0	0	0

The performance of each code is analyzed and is tabulated in Table V. Here the implementation of the hamming code consumes more area compared to the other coding systems. The delay is also more in the hamming code. In the case of power, the DMC consumes more power than the other coding systems.

The Table VI provides proper information about the possible detection percentage of errors in various Error Correcting Codes. It is clearly evident that the MDMC and DMC is better than the Matrix codes in the case of error detection.

The Table VI indicates that the Decimal Matrix Codes (DMC) and Modified Decimal Matrix Codes(MDMC) has better coverage compared to the other error Correcting Codes.

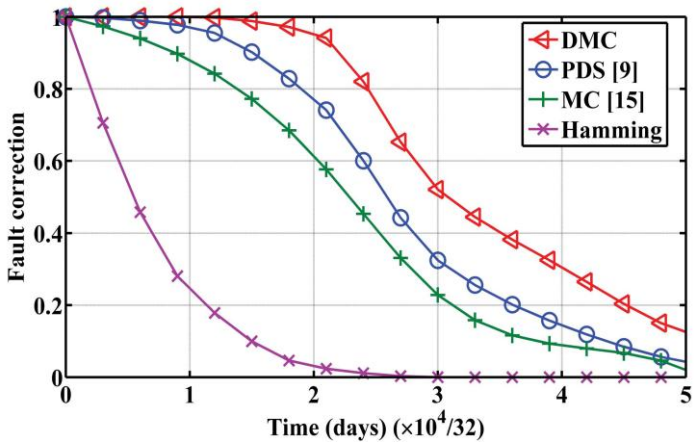

Fig.3. J (S) versus time of different protection codes

On the basis of Mean Time To Failure (MTTF), the reliability of these Codes can be analysed. The correctable probabilities *J (S) s* of different protection codes are shown

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in Fig. 3. It can be seen that the correctable probability *J (S)* of the DMC scheme is larger than other codes.

IV. CONCLUSION

This paper analyses the various existing coding techniques that are used for error correction in the digital systems. Some systems show adequate improvement in area and power analysis but fails in the delay analysis. Some other works that are considered fails to give improvement in any fields. By analyzing table, it can be concluded that the Modified Decimal Matrix Codes (MDMC)is efficient among the existing method. The MDMC code provides single and double error correction .It also provide higher tolerance against large MCUs.

V. FUTURE SCOPE

The study carried out in this paper can be extended to many other potential fields. Major possibility is to develop an error correcting system which can provide better performance, with less delay overhead, lower power requirements and less area consumption. The study can be carried out by pipelining the existing codes in to an efficient form so that the delay overhead is reduced. Also by changing the adders and other elements used in realization , the area can be reduced, by the proper implementation of the above indicated two ideas the power consideration can also be considerably reduced.

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REFERENCES

[1]. Yoon Seok Yang , Seung Eun Lee, Wei Wu, Ravi Iyer, Gwan S. Choi, *Low-Power, Resilient Interconnection with Orthogonal Latin Squares*, in IEEE design & test of computers.

[2]. V. Gherman, S. Evain, N. Seymour, and Y. Bonhomme, *Generalized parity-check matrices for SEC-DED codes with fixed parity*, in Proc. IEEE On-Line Testing Symp., Jul. 2011, pp. 198–20.

[3]. Jing Guo, Liyi Xiao, Zhigang Mao, and Qiang Zhao ,*Enhanced Memory Reliability against Multiple Cell Upsets Using Decimal Matrix Code*, IEEE Transactions On Very Large Scale Integration (VLSI) Systems, March 2014.

[4]. Pedro Reviriego, Salvatore Pontarelli, Juan Antonio Maestro, and Marco Ottavi, *A Method to Construct Low Delay Single Error Correction Codes for Protecting Data Bits Only*, IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems., vol. 32, no. 3, pp. 479 - 483, March 2013

[5]. Ahilan.A and Deepa.P ,*Modified Decimal Matrix Codes in FPGA Configuration Memory for Multiple Bit Upsets*, IEEE January 2015.

[6]. J. D. Warnock, Y.-H. Chan, S. M. Carey, H. Wen,P. J. Meaney, G. Gerwig and W. V. Huott ,*Circuit and physical design implementation of the microprocessor chip for the Enterprise system*, IEEE J. Solid-State Circuits, vol. 47, no. 1, pp. 151–163,Jan. 2012.

[7]. J. Tausch, *Simplified birthday statistics and hamming EDAC*, IEEE Trans. Nucl. Sci., vol. 56, no. 2, pp. 474–478, Apr. 2009.

BIOGRAPHY

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