ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Special Issue 24, April 2016

AN EFFICIENT CARRY SELECT ADDER WITH REDUCED AREA AND DELAY

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Abstract

The logic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA to study the data-dependency and to identify redundant logic operations. We have eliminated all the redundant logic operations present in conventional CSLA and proposed a new logic formulation for CSLA. In this method, the carry-select operation is scheduled before the calculation of final-sum, which is different from the conventional approach. Bit-patterns of two anticipating carry-words and fixed Cin bits are used for logic optimization of carry select and generation units. An efficient CSLA design is obtained using optimized logic units. The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. Due to small carry-output delay, the proposed CSLA design is a good candidate for square-root (SQRT)-CSLA. Theoretical estimate shows that the proposed SQRT-CSLA involves nearly25% less area-delay-product (ADP) than the BEC-based SQRTCSLA which is the best amongst the existing SQRT-CSLA designs on average for different bit-widths.

INTRODUCTION

1.1 Carry-Select Adder

A carry-select adder is a particular way to implement an adder, which is a logic element that computes the -bit sum of two -bit numbers. The carry-select adder generally consists of two ripple carry adders and a multiplexer.

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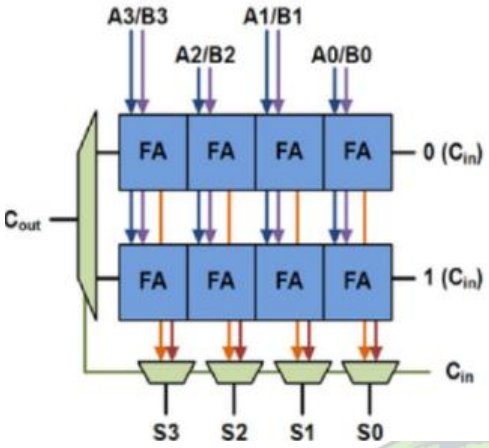

Fig 1.1 Block diagram of carry select adder

Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one.

1.2 Carry-Look Ahead Adder (CLA)

Carry-look ahead adder (CLA) is a type of adder used in digital logic. A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits. Most other arithmetic operations, e.g. multiplication and division are implemented using several add/subtract steps.

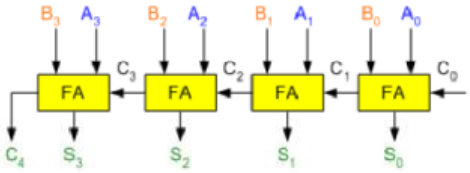

Fig 1.2 Block diagram of carry look ahead adder

Accordingly, reducing the carry propagation delay of adders is of great importance. Different logic design approaches have been employed to overcome the carry propagation problem. One widely used approach employs the principle of carry look-aheadsolves this problem by calculating the carry signals in advance, based on the input signals.

1.3 Propagation Delay

Propagation delay is the amount of time it takes for the head of the signal to travel from the sender to the receiver. It can be computed as the ratio between the link length and the propagation speed over the specific medium.

1.4 Value Changed Dump (VCD) File

Value change dump is an ASCII-based format for dump files generated by EDA logic simulation tools. An Extended VCD format defined six years later in the IEEE Standard supports the logging of signal strength and directionality.

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1.5 Modified Carry Save Adder (MCSA)

A carry-save adder is a type of digital adder, used in computer micro architecture to compute the sum of three or more n-bit numbers in binary.

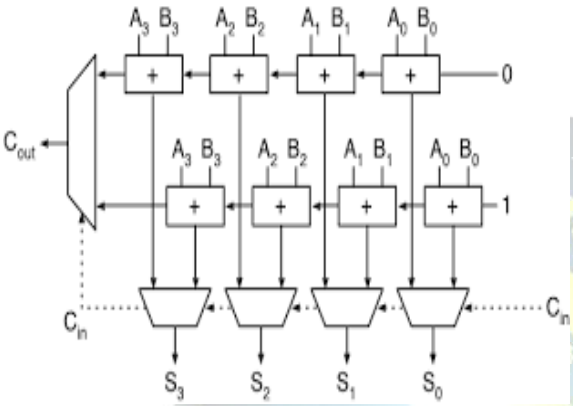

Fig1.3: simple block diagram of modified carry save adder

It differs from other digital adders in that it outputs two numbers of the same dimensions as the inputs, one which is a sequence of partial sum bits and another which is a sequence of carry bits

1.2 STRUCTURED ASICS

A new alternative has recently emerged to address the market void between FPGAs and cell-based ASICs. Analysts term this as the Structured ASIC.

1.2.1 First Generation Structured ASICS

Like the FPGA market, the Structured ASIC market had a flurry of early entrants many of who have departed the market. Examples include respectable semiconductor companies like NEC, LSI logic and EDA vendors such as Simplicity.

First Generation Structured ASICs provided designers with considerable power and cost improvements over FPGAs but failed to remove many barriers to entry that existed with traditional cell-based ASICs. First generation Structured ASICs had the following characteristics:

- Turn-around times were still 2-5 months from tape-out to silicon
- NREs were still in the range of $150-$250K or more making the technology difficult to access for mainstream users.
- Minimum order quantities were required as wafers could not be shared amongst projects or customers
- Development costs and time were also very high and long respectively, as designers were expected to undergo rigorous verification down to the transistor level
- Designers transitioning from prototyping devices like FPGAs to first generation Structured ASICs

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were still expected to redesign the product into a completely new device, revisit timing closure and re-qualify the new device before it production ready.

While some companies still offer first generation Structured ASICs today, market acceptance has been severely limited as a result of these barriers to entry. However, these first generation Structured ASICs paved the way for a new generation that would combine the benefits of both FPGAs and cell-based ASICs.

1.2.2 Second Generation Structured ASICS

A new generation of Structured ASICs has emerged on the market and is gaining traction. This generation utilizes a single via mask for configuring the device. In doing so, it removes the need for the massive amounts of SRAM configuration elements and metal interconnect that plagues today's FPGAs. The benefits to designers are delivered through a device that provides up to 20X lower device power consumption and up to 80% lower unit cost than FPGAs, depending on device density, (larger FPGAs have more configuration elements and metal interconnect).

This new generation of Structured ASICs, available from eASIC Corporation, and named Extreme also removes the barriers of traditional cell based ASICs and also first generation Structured ASICs. With Extremes Structured ASICs advantages include:

- Turn-around times from tape-out to silicon is only 3-4 weeks
- There are zero mask charges as multiple projects can be shared on a wafer
- There is no minimum order quantity
- Development tools costs are low (analogous to FPGA type tools)
- Development time is short as designers need not perform verification down to the transistor level or perform exhaustive test coverage
- Coarse FPGA-like architecture based on calls which provides manufacturing yield advantages .

There are device options for both prototyping and mass production. Designers transitioning from prototyping Nextreme Structured ASICs to mass production Nextreme Structured ASICs need not revisit timing closure or re-qualify the production device.

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Area and Delay of AND,OR,and NOT Gate Data Sheet:

	AND - gate	OR - gate	NOT - gate
Area(um^2)	7.37	7.37	6.45
Delay(ps)	180	170	100

Area and delay of 2-input AND, 2-input OR and NOT gates area and delay of each design is calculated from the AOI gate counts (Na;No;Ni),(na; no; ni), and the cell details of Table . the proposed CSLA involves 0.42ns more delay, but it involves nearly 28% less ADP due to less area complexity. Interestingly, the proposed CSLA design offers multi-path parallel carry propagation whereas the CBL-based CSLA of offers a single carry propagation path identical to the RCA design. Besides, the proposed CSLA design has 0.45ns less output carry delay than the output-sum delay. This is mainly due to the CS unit which produces output-carry before FSG calculate the final-sum.

3.1 EXISTING METHOD

Conventional CSLA is a RCA-RCA configuration which generates a pair of sum words and output-carry bits corresponding the anticipated input-carry (cin= 0 and 1), and selects one out of each pair for final-sum and final-output-carry. He have proposed a square root (SQRT)-CSLA to implement large bit-width adders with less delay. In SQRT CSLA, CSLAs with increasing size are connected in a cascading structure. The main objective of SQRT-CSLA design is to provide parallel path for carry propagation which helps to reduce the overall adder delay. have suggested a BEC-based CSLA.

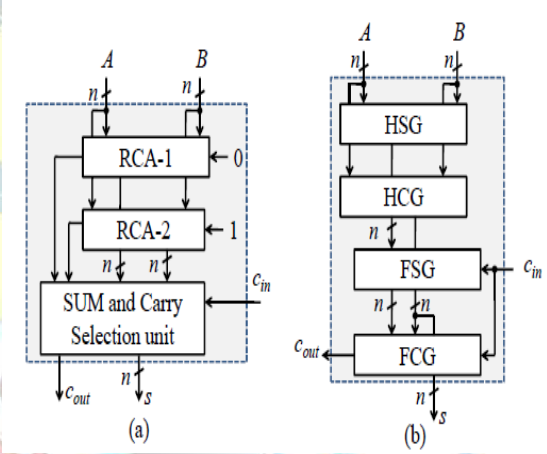

Fig 3.1(a) Conventional carry select adder (b) logic diagram of RCA

The BEC-based CSLA involves less logic resources than the conventional CSLA but it has marginally higher delay. A CSLA based on common Boolean logic (CBL) also proposed in. The CBL based CSLA of involves significantly less logic resource than the conventional CSLA, but it has longer CPD which is almost equals to that of RCA. To overcome this problem,

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SQRT-CSLA based on CBL have been proposed in. However, CBL-based SQRT-CSLA design of requires more logic resource and delay than the BEC-based SQRT-CSLA.The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. Due to small carry-output delay, the proposed CSLA design is a good candidate for square-root (SQRT)-CSLA. Theoretical estimate shows that the proposed SQRT-CSLA involves nearly35% less area-delay-product (ADP) than the BEC-based SQRTCSLA which is the best amongst the existing SQRT-CSLA designs on average for different bit-widths. ASIC synthesis result shows that, the BEC-based SQRT-CSLA design involves 48% more ADP and consumes 50% more energy than the proposed SQRT-CSLA on average for different bit-widths.

The CSLA is uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input CIN=0 and CIN=1, then the final sum and carry are selected by the multiplexers (mux). The speed of addition is limited by the time required to propagate a carry through the adder.

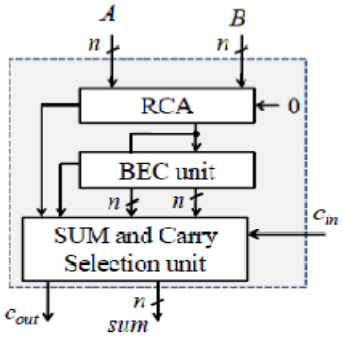

Fig 3.2 structure of BEC based CSLA

Based on this have used an add-one circuit instead of RCA-2 in the CSLA, where a BEC circuit is used in for the same purpose. Since, BEC based CSLA offers best area-delay-power efficiency amongst the existing CSLA. This system has developed to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum Since, BEC based CSLA offers best area-delay-power efficiency amongst the existing CSLAs.

3.1.1 Existing System Drawbacks

- Low area efficient.
- High power consumption.
- High delay.

In this paper to improve the speed of addition a very simple approach is proposed. CLA is arranged in the form of ripple carry adder (RCA) and is used to speed up the final addition in many parallel multipliers. But due to the

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structure of the CSLA it occupies more chip area, because it uses multiple pairs of RCA's (CLA) to generate partial sum and carry by considering Cin=0 and Cin=1. Thus the complexity of the final adder structure is high.

4.1 PROPOSED METHOD

Conventional CSLA is a RCA-RCA configuration which generates a pair of sum words and output-carry bits corresponding the anticipated input-carry (cin= 0 and 1), and selects one out of each pair for final-sum and final-output-carry. He have proposed a square root (SQRT)-CSLA to implement large bit-width adders with less delay. In SQRT CSLA, CSLAs with increasing size are connected in a cascading structure. The main objective of SQRT-CSLA design is to provide parallel path for carry propagation which helps to reduce the overall adder delay have suggested a BEC-based CSLA.

The BEC-based CSLA involves less logic resources than the conventional CSLA but it has marginally higher delay. A CSLA based on common Boolean logic (CBL) also proposed in. The CBL based CSLA of involves significantly less logic resource than the conventional CSLA, but it has longer CPD which is almost equals to that of RCA. To overcome this problem, SQRT-CSLA based on CBL have been proposed in. However, CBL-based SQRT-CSLA design of requires more logic resource and delay than the BEC-based SQRT-CSLA.

The proposed CSLA is based on the logic formulation given in and its structure is shown in fig. It consists of one HSG unit, one FSG unit, one CG unit and one CS unit. The CG unit is comprised of two carry-generators (CG0 and CG1) corresponding to input-carry '0' and '1'. The HSG receives two n bit operands (A and B), and generate half-sum word s0 and half-carry word c0 of width n-bit each. Both CG0 and CG1 receive s0 and c0 from the HSG unit and generates two n-bit full-carry words c01 and c11 corresponding to input-carry '0' and '1', respectively. The logic diagram of HSG unit is shown in Fig. The CS unit selects one final-carry word from the two carry words available at its input-line using control signal cin. It selects c01 when cin = 0, otherwise it selects c11.

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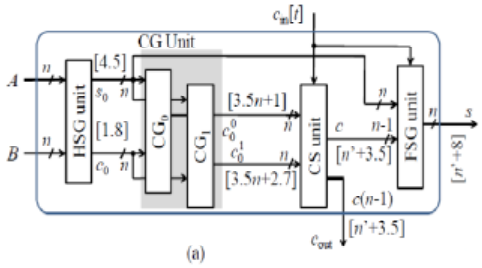

Fig 4.1 Carry select adder design

The CS unit can be implemented using n-bit 2-to-l MUX. The proposed CSLA design is more favorable than the existing CSLA designs for area-delay efficient implementation of SQRT-CSLA. A 16-bit SQRT-CSLA design using proposed CSLA is shown in Fig. we have estimated area and delay of SQRT-CSLA using proposed CSLA design and the BEC-based CSLA of [6] and CBL based CSLA of for bit-widths 16; 32 and 64 using Table I and II. The estimated values are listed in Table IV for comparison. As shown in Table IV, delay of CBL-based SQRT-CSLA is significantly higher for large bit-width than the proposed SQRT-CSLA and BEC-based SQRT-CSLA designs. Compared with SQRT-CSLA designs of and,the proposed SQRT-CSLA design, respectively.

4.1.1 Proposed System Technique

SQRT-CSLA

CSLAs of increasing size are used in the SQRT-CSLA to extract maximum concurrency in the carry propagation path. Using SQRT-CSLA design large size adders are implemented with significantly less delay than a single-stage CSLA of same size.

Advantages

- Less area overhead system
- Less power consumption
- High speed architecture.

5.1 MODULE'S

1. HALF SUM GENERATOR (HSG)
2. CARRY-GENERATOR (CG0)
3. CARRY-GENERATOR (CG1)
4. CARRY-SELECT (CS) UNIT
5. FINAL-SUM GENERATION (FSG) UNIT

5.1.1 Half Sum Generator (HSG)

The proposed SQRT CSLA is developed with the help of modified half adder (HAM), modified full adder (FAM) andmodified XOR gate (XORM). In place of BEC, combinational logic block (CLB) is used. XORM has 1 gate less than the conventional XOR gate of 5 gates (AND-OR-NOT implementation).

HAM has 2 gates less than the conventional half adder as shown in Fig.4.

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The full adder is constructed with two HAMs and an AND gate .has only 9 gates, 4 gates less than conventional full adder. As the number of gates reduce in the basic building blocks of the proposed SQRT CSLA area is also reduced.

A part from the above modifications, one more small change is made in the design which allows us to get the carryout of the group without using the mux .

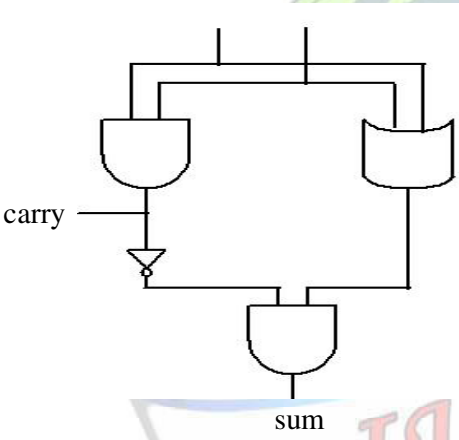

Fig 5.1 Design of half sum generator

5.1.2 Carry-Generator CG0 and CG1

The logic circuits of CG0 and CG1 areoptimized to take advantage of the fixed input carry bits. Theoptimized designs of CG0 and CG1 are shown in Fig.

It selects c01 when cin = 0, otherwise it selects c11 The CS unit can be implemented using n-bit 2-to-l MUX. But, we find from the truth-table of CS unit that carry-words c01 and c11 follow a specific bit-pattern. If c01 (i) = '1', then c11

(i) = 1, irrespective of s0(i) and c0(i), for 0 _ i _ n & 1. This feature is used for logic-optimization of CS unit. The optimized design of CS unit is shown in Fig.3(e) which is comprised of n AND-OR gates. The final-carry word c is obtained from the CS unit. The MSB of c send to output as cout, and (n&1) LSBs are XORed with (n &1) MSBs of half-sum (s0) in the FSG (shown in Fig.3.5) to obtain (n& 1) MSBs of final-sum (s). The LSB of s0 is XORed with cin to obtain LSB of s.

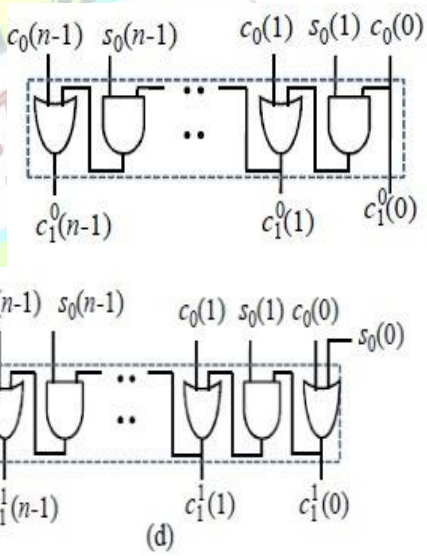

Fig 5.2 Design of carry generator CG0 and CG1

The CS unit selects one final-carry word from the two carrywords available at

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its input-line using control signal cin. It selects c01 when cin = 0.

5.1.3 Carry-Select (CS) Unit

The CS unit selects one final-carry word from the two carry words available at its input-line using control signal c_{in}. It selects $c^0_1$when c_{in} = 0, otherwise it selects c^1_1. The CS unit can be implemented using n-bit 2-to-l MUX. But, we find from the truth-table of CS unit that carry-words $c^0_1$and c^1_1follow a specific bit-pattern. If $c^0_1(i)$ = '1', then $c^1_1(i)$ = 1, irrespective of $s_0(i)$ and $c_0(i)$, for 0 <i<n - 1. This feature is used for logic-optimization of CS unit. The optimized design of CS unit is shown in Fig

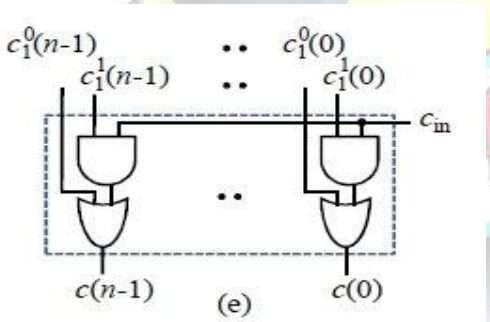

Fig 5.3 Design of carry select unit

Most other arithmetic operations, e.g. multiplication and division are implemented using several add/subtract steps. Accordingly, reducing the carry propagation delay of adders is of great importance. One widely used approach employs the principle of carry look-aheadsolves this problem by calculating the carry signals in advance, based on the input signals.

5.1.4 Final-Sum Generation (FSG) Unit

The full adder is constructed with two HAMs and an AND gate .it has only 9 gates, 4 gates less than conventional full adder. As the number of gates reduce in the basic building blocks of the proposed SQRT CSLA area is also reduced. AND-OR gates. The final-carry word c is obtained from the CS unit. The MSB of c send to output as c_{out}, and (n-1) LSBs are XORed with (n - 1) MSBs of half-sum (s_0) in the FSG (shown inFig 3.7) to obtain (n - 1) MSBs of final-sum (s). The LSB of s0 is XORed with c_{in} to obtain LSB of s.

A part from the above modifications, one more small change is made in the design which allows us to get the carryout of the group without using the mux. CG unit is comprised of two carry-generators (CG0 and CG1) corresponding to input-carry '0' and '1'. Both CG0 and CG1 receive s0 and c0 from the HSG unit and generates two n-bit full-carry words c01and c11 corresponding to input-carry '0' and '1', respectively. The logic diagram of HSG unit .The logic circuits of CG0 and CG1 are optimized to take advantage of the fixed input carry bits.

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6.1 SIMULATION RESULTS

6.1.1 Half Sum Generator

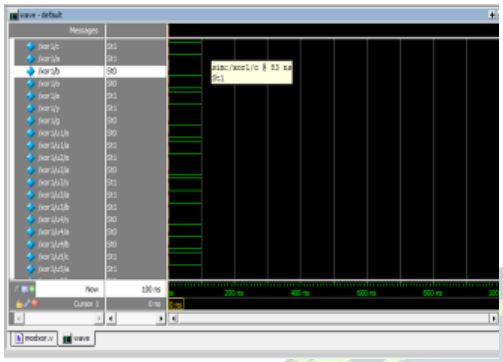

Fig 6.1 Modified xor gate

6.1.2 Carry Generator 0

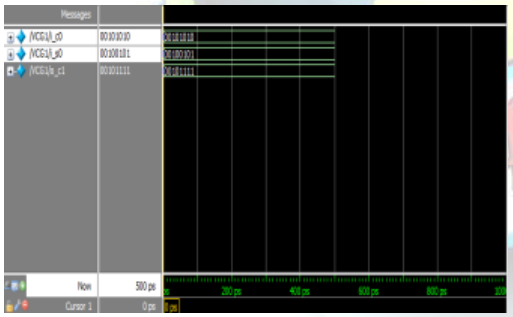

Fig 6.2 Carry generator 0

6.1.3 Carry Generator 1

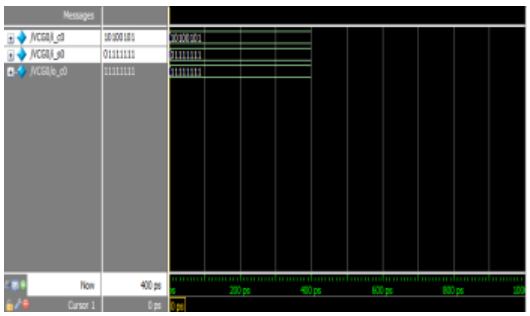

Fig 6.3 Carry generator 1

6.1.4 Control Selection

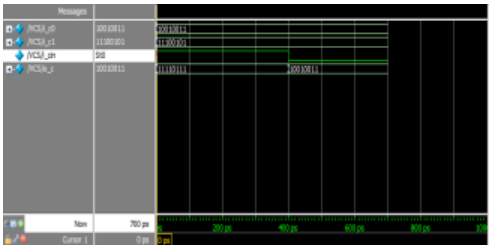

Fig 6.4 Control selection

6.1.5 Full Sum Generator

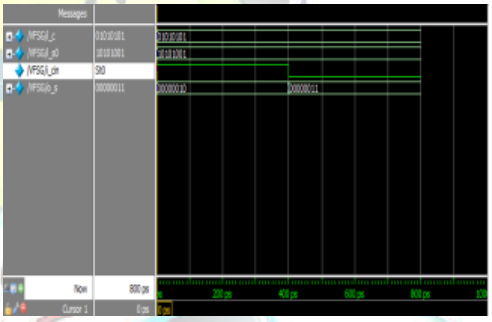

Fig 6.5 Full sum generator

6.1.6 Carry Select Adder

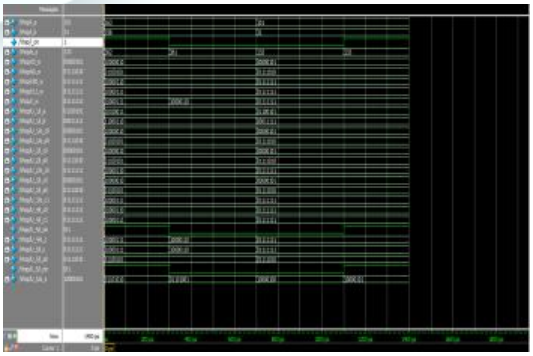

Fig 6.6 Carry select adder

7.1 CONCLUSION

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We made an analysis on the logic operations involved in conventional CSLA and BEC-based CSLA to study the data dependency, and to identify redundant logic operations. We have eliminated all the redundant logic operations of conventional CSLA, and proposed a new logic formulation for CSLA. In the proposed scheme, the carry-select operation is scheduled before the calculation of final-sum, which is different from the conventional approach. Carry-words corresponding to input carry '0' and '1' generated by the CSLA based on the proposed scheme follow a specific bit-pattern which is used for logic optimization of carry-select unit. Fixed input bits of carry generator unit are also used for logic optimization. Based on this, an optimized design for carry-select unit and carry generator unit are obtained. Using these optimized logic units, an efficient design is obtained for CSLA. The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. Due to small carry output delay, the proposed CSLA design is a good candidate for SQRT adder.

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