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SINGLE-PHASE HIGH STEP-UP CONVERTER WITH HALF-BRIDGE-BASED PV INVERTER SYSTEM

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Abstract-*In this paper, a single-phase high step-up converter isproposed, designed not only to boost the relatively low photovoltaic(PV) voltage to a high bus voltage with high efficiency, but also tooffer a neutral point terminal for the half-bridge-based inverters.First and foremost, two symmetrical high step-up converters arecombined and integrated to derive an improved converter withneutral point terminal, which is strongly expected for the half-bridge-based inverters. Secondly, the voltage gain of the converteris extended and the narrow turn-off period is avoided by using thecoupled inductor multiplier. Furthermore, the coupled inductormultiplier reduces the voltage stress of all the power devices. Asa result, the low voltage-rated power devices can be employed tominimize the conduction losses. More importantly, all the activeswitches work in the zero-voltage-switching condition, which reduces the switching losses effectively. All these factors improve thecircuit performance in the high step-up applications, especially forthe half-bridge based PV inverter systems. Finally, the experimental results from a 500 W, 48 –760 V prototype at 100 kHz switchingfrequency are provided to verify the effectiveness of the proposedconverter. The highest efficiency of the prototype is 96.5% and theefficiency is over 94% in a wide load range.*

I.INTRODUCTION

Because of the environmental problems on the globalwarming and the increasing threat of the fast exhaustionof the fossil fuel, more and more efforts have been made toexplore the renewable energy sources, such as the wind generation, the geothermal, the photovoltaic (PV), and the fuel cells.These renewable energy sources can generate electricity without harming
environment. In recent years, as one of themost promising sources in the renewable energy, the distributedPV generation systems have received increasing popularity in the residential areas. Therefore, many researches concentrate on the small size PV grid-connected inverter, which isdesired for the low-power and high-efficiency applications.

In the low power grid-connected PV system, the transformer less configuration has become a widespread tendency due to itshigher efficiency, smaller size, lighter weight, and lower costcompared with the isolated counterparts. However, in thetransformerless condition, when the traditional full bridge inverter with unipolar sinusoidal pulse width modulation (SPWM)modulation is adopted, the common mode (CM) ground leakage current may appear on the parasitic capacitor between thePV cell and the ground, which brings out the safety issue andreduces the efficiency of the inverter. Consequently, how tosuppress and eliminate the CM leakage current caused by theparasitic capacitor between the PV and the ground is one ofthe most emergent technologies. Unfortunately, somepublished state-of-the-art full-bridge-based transformer less inverters, such as H5 inverter, H6 inverter, the HERIC inverter andso on, contain more power switches or increase the conduction losses. In fact, the half-bridge inverter and neutral pointclamped (NPC) inverter can naturally eliminate the CM leakagecurrent because the grid neutral line is directly connected to theneutral point of the dc bus. However, the dc bus voltage of the half-bridge-based inverters should be twice as thatof the full-bridge-based topologies and the neutral point of thedc bus should be also required. Therefore, how to explore thehigh-step-up and high-efficiency dc–dc converters is nowadaysthe focus of an intensive research effort by the power electronicscommunity. These high step-up converters are strongly expected to not only boost the relatively low voltage to a high busvoltage with high efficiency, but also offer a neutral point terminal for the half-bridge-based transformerless inverters, which is shown in Fig 1.

The conventional boost converters are not suitable for thehigh step-up conversion applications because the duty cycle ofthe conventional boost converter with high step-up conversionis very large, which results in narrow turn-off period, large current ripple, and high switching losses. In order toachieve large voltage conversion ratio, some switched capacitor-based converters were published. With the switchedcapacitor technology, the conversion ratio of the converteris increased and the voltage stresses of the devices are decreased. Unfortunately, the switched capacitor techniquemakes the switch suffer high transient current and large conduction losses. Moreover, many switched capacitor stages are required to achieve the high voltage gain, which makes the circuitcomplex. It is easier for the isolated converters to achieve an extremelyhigh voltage gain because the turn's ratio of the transformer canbe employed as another control freedom to extend the voltage gain. By adjusting the transformer turns ratio appropriately, high voltage conversion ratio can be realized withoptimal duty cycle. However, one inductor and one transformerare necessary in these converters, which increase the circuitvolume and reduce the power density. Furthermore, the drivingcircuits and the sampling circuits in the isolated converters mayincrease the system complexity when compared with those inthe non-isolated converters. Christo Ananth et al.[2] discussed about principles of Electronic Devices which forms the basis of the project.

In fact, most of the non-isolated high step-up converters can bederived from their isolated counterparts. Some highstep-up boost converters with coupled inductor are introducedto achieve large voltage conversion ratio.

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The voltagegain is extended and the switch voltage stress is reduced by thetransformer function of the coupled inductor. Moreover, onlyone magnetic component is used, which reduces the volumeand the complexity of the converter. However, the leakage inductance of the coupled inductor may not only bring about highvoltage spikes on the switch when it turns OFF, but also inducelarge energy losses.Combing the concept of coupled inductor and switched capacitor, a single-phase improved active clamp-coupled inductor-based converter with extended voltage doubler cell is proposed with some significantly indispensable advantages, such asvoltage gain extension without extreme duty-cycle, switch voltage stress reduction, zero-voltage-switching (ZVS) soft switching operation and output diode reverse-recovery problem alleviation. Unfortunately, this converter cannot offer a neutralpoint terminal for the half-bridge-based transformer less inverters. However, it provides an excellent high step-up convertercandidate for further topology derivation if the neutral pointterminal is required.

In this paper, an improved single-phase high step-up converter with coupled inductor multiplier is derived, which has allthe above-mentioned advantages that the converter in has Active inductor coupled based converter.More importantly, the proposed converter can naturally createa neutral point terminal and its voltage gain is twice of that ofthe converter in Active inductor coupled based converter, which can be employed as a high step-up dc–dc converter for the secondary half-bridge-based transformerless inverter system. The topology derivation principle ishighlighted and the circuit operation of the proposed converteris explored clearly. The advantageous circuit performance canbe proved by a 500-W 48–760 V prototype operating at 100-kHzswitching frequency.

1. BLOCK DIAGRAM:

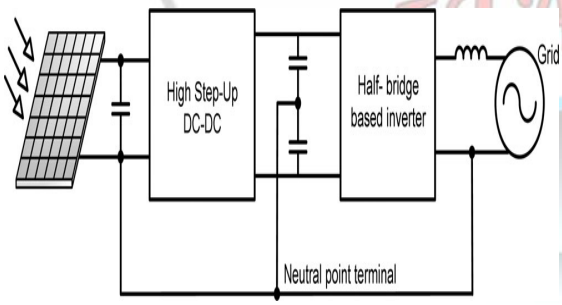

Fig.1.High step-up dc–dc converter for half-bridge-based inverter.

PHOTOVOLTAIC CELL:

PV cells are made of semiconductor materials, such as silicon. For solar cells, a thin semiconductor wafer is specially treated to form an electric field, positive on one side andnegative on the other. When light energy strikes the solar cell, electrons are knocked loose from the atoms in the semiconductor material. If electrical conductors are attached to the positive and negative sides, forming an electrical circuit, the electrons can be captured in the form of an electric current - that is, electricity. This electricity can then be used to power a load. A PV cell can either be circular or square in construction

DC-DC CONVERTERS:

DC-DC converters can be used as switching mode regulators to convert an unregulated dc voltage to a regulated dc output voltage. The regulation is normally achieved by PWM at a fixed frequency and the switching device is generally BJT, MOSFET or IGBT. The minimum oscillator frequency should be about 100 times longer than the transistor switching time to maximize efficiency. This limitation is due to the switching loss in the transistor. The transistor switching loss increases with the switching frequency and thereby, the efficiency decreases. The core loss of the inductors limits the high frequency operation. There are four topologies for the switching regulators: buck converter, boost converter, buck-boost converter, cúkconverter. However my paper work deals with the boost regulator and further discussions will be concentrated towards this one.

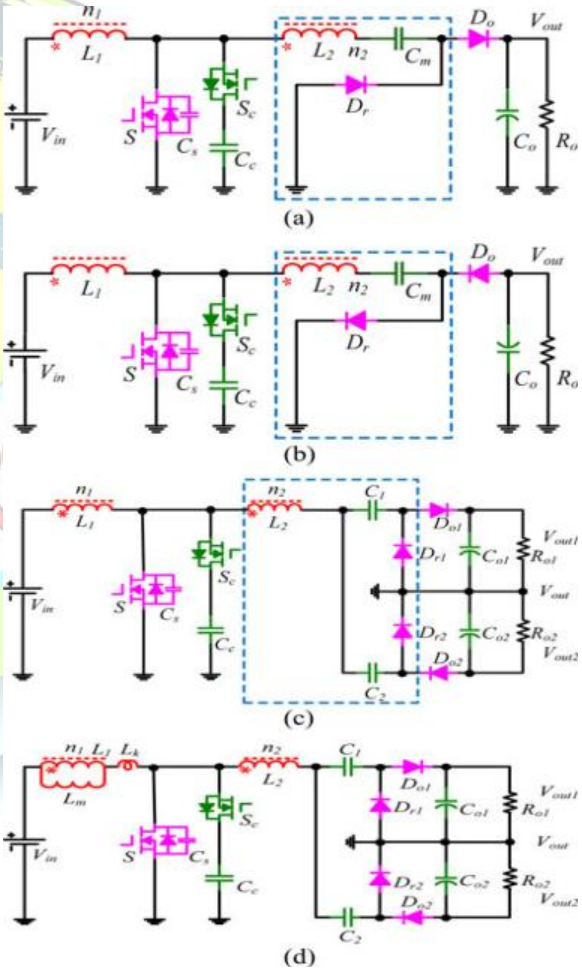

Fig. 2.Topology derivation: (a) active clamp-coupled inductor-based converter; (b) symmetrical converter based on the converter in [active clamp coupled-Inductor-basedconverter;(c) Proposed converter; (d) equivalent converter.

HALF BRIDGE INVERTER

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The D.C to A.C power converters are known as inverters. An inverter is a circuit which converts a D.C power into A.C power at desired output voltage and frequency. The A.C output voltage could be fixed at a fixed or variable frequency. Switches S_1 and $S_2$are the gate commutated devices such as power BJTs, MOSFETs, GTO, IGBT, MCT, etc. Switch S_1 Conducting time period (0<t<T/2) and Switch S_2 Conducting time period (T/2<t<T), T=1/f and f is the frequency of the output voltage waveform.

3. CIRCUITOPERATIONAL ANALYSIS

The single-phase coupled-inductor-based converter with extended voltage doubler cell proposed in Single-phase improved active clamp coupled-inductor-based converter with extended voltage doubler cell is given in Fig. 2(a).The extended voltage doubler cell circuit is plotted in the dashblock, composed by an inductor L2 , a switched capacitor Cm ,and a regenerative diode Dr. The clamp circuit is composed ofan auxiliary switch Sc and a capacitor Cc . Based on the converter in Single-phase improved active clamp coupled-inductor-based converter with extended voltage doubler cell, a symmetrical converter shown in Fig. 2(b) can beeasily derived by changing the direction of regenerative diode
Dr , output diode Do , and output capacitor Co .Compared with the converter in Single-phase improved active clamp coupled- inductor-based converter with extended voltage doubler cell, the converter in Fig. 2(b)operates similarly and offers a negative output voltage. More importantly, the converter in Fig. 2(b) has the same active switchesand coupled inductance with the converter in Fig. 2(a). Therefore, by combining and integrating these two symmetrical converters, the proposed converter can be derived without adding
extra active switches and magnetic component, which is given
in Fig. 2(c).

In the proposed converter, the clamp circuit includes a switchSc and a capacitor Cc . The coupled inductor multiplier in the
dash block contains a secondary winding of the coupled inductor, two switched capacitors C1 and C2 , and two regenerative
diodesDr 1 and Dr 2 . The inductor L1 is coupled to the inductorL2 . The coupling reference is marked by "∗", and the turns ratiois expressed by N =n2 /n1 . The output load can be divided intotwo equal parts, the voltage on the load Ro1 is Vout1 and the
voltage on the load Ro2 is Vout2 .

The coupled inductor can be considered as an ideal transformer, a parallel magnetizing inductance and a series leakageinductance High-efficiency, high step-up DC-DC converters. The equivalent circuit of the proposed converter is shown in Fig. 2(d). L1 and L2 represent the primaryand secondary windings, respectively. Cs is the parallel capacitor, including the parasitic capacitors of the main and clampswitches.

As shown in Fig. 3, there are eight main operation stages inone switching cycle. The explanation of the key waveforms is thefollowing: iL k is the current through the leakage inductance Lk ;vds is the voltage across the main switch S; vC c is the voltage
across the clamp capacitor Cc ; iC c is the current though theclamp circuit Sc and Cc ; iL 2 is the current through the secondary
winding L2 ; vD o1 , vD r 1 , vD o2 , vD r 2 , and iD o1 , iD r 1 , iD o2 , andiD r 2 are the voltages and currents of the diodes Do1 , Dr 1 , Do2 ,and Dr 2 . The equivalent circuits for each stage are shown inFig. 4.

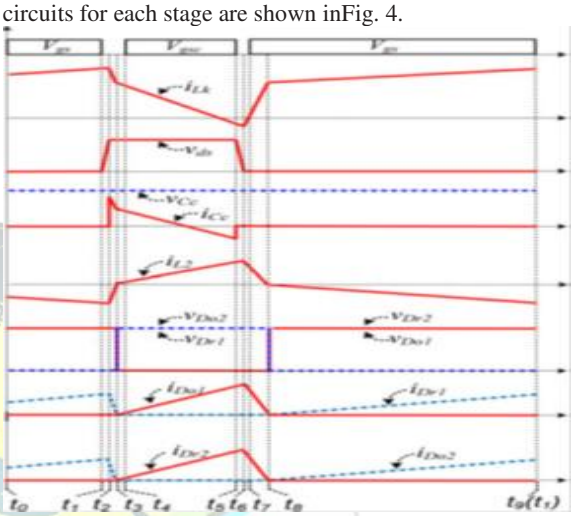

Fig. 3.Key waveforms of converter.

Stage 1 [t0 –t1]: Before t1 , the main switch S is in the ONstate, while the clamp switch Sc is in the OFF state. Duringthis period, the diodes Dr 1 and Do2 conduct, while Do1 andDr 2 are reverse biased.

The magnetizing inductance Lm andthe leakage inductance Lkare charged by the input voltage Vin ;thus, the magnetizing current and leakage inductance currentincrease gradually almost in a linear way. At the same time, theswitched capacitor C1 is charged by the secondary winding L2 ,also the energy stored in L2 and the switched capacitor C2 istransferred to the load Ro2 .

Stage 2 [t1 –t2]: The main switch S turns OFF at t1 , then the parallel capacitor Cs begins to resonant with the leakage inductance Lk . Considering that Cs is small and Lk is relatively large, the voltage vds on the main switch S rises almost at a constant slope from zero. The turn-off losses of the main switch are reduced due to the existence of Cs .

Stage 3 [t2 –t3]: At t2 , the switching voltage of the main switch reaches the clamp capacitor voltage, and the antiparallel diode of the clamp switch Sc conducts. Then vds is clamped to vC c by the antiparallel diode of the clamp switch Sc . Since the clamp capacitor Cc is much larger than Cs , Cs can be neglected and almost all the current flow through Cc . After t2 , the leakage inductance Lk is discharged by the voltage of Cc . In this stage, the current through Lk decreases sharply, as well as the current through the secondary winding.

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Stage 4 [t3 –t4]: At t3 , iL 2 falls to zero, then the diodes Do1 and Dr 2 begin to conduct, while Dr 1 and Do2 are reverse bi-
ased. In this stage, both Lm and Lk are discharged; thus, the current through Lk decreases gently when compared to Stage
3. At the same time, the switched capacitor C2 is charged by the secondary winding L2 , also the energy stored in L2 andthe switched capacitor C1 is transferred to the load Ro1.
Stage 5 [t4 –t5]: The turn-on signal is applied to the clamp switch Sc at t4 . Sc is turned ON when its body diode is conducting; thus, the ZVS turn-on condition of the clamp switch Sc is achieved.The equivalent circuit and currents equations in this stage are similar to that of Stage 4.

Stage 6 [t5 –t6]: The clamp switch Sc is turned OFF at t5 . After that the parallel capacitor Cs begins to resonant with the
leakage inductance Lk again. Because Cs is small and Lk is relatively large, voltage on the main switch vds decreases almost
at a constant slope and the voltage across the clamp switch Scincreases from zero at the same rate. Thus, the turn-off losses of the clamp switch are reduced due to the existence of Cs . The analysis in this stage is very similar to Stage 2.

Stage 7 [t6 –t7]: The voltage of the parallel capacitor Cs falls to zero at t6 , and then the antiparallel diode of the main switch S begins to conduct. Cs and Lkstop resonating. The increasing rate of the current through Lk is controlled by the output voltage,and at t6 the current through the secondary winding iL 2 begins to fall.

Stage 8 [t7 –t8]: The turn-on signal is applied to the main switch S when its antiparallel diode is conducting; thus, the ZVS turn-on condition of the main switch S is achieved. The equivalent circuit and current equation in this stage are similar to Stage 7.

At t8 , the current through the secondary winding iL 2 falls to zero, then the diodes Dr 1 and Do2 begin to conduct while Do1 and Dr 2 are reverse biased. After that both Lm and Lk are charged by the input voltage Vinagain, thus the current through Lk increases gently when compared to Stage 7 and Stage 8. The converter goes back to Stage 1 and begins a new switching cycle.

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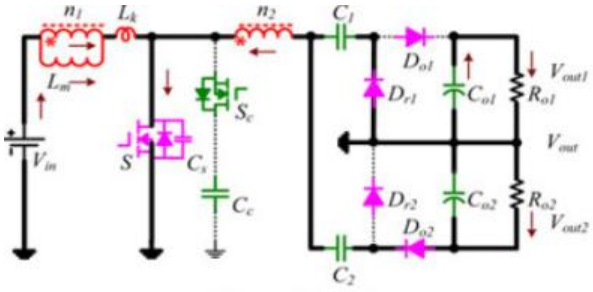
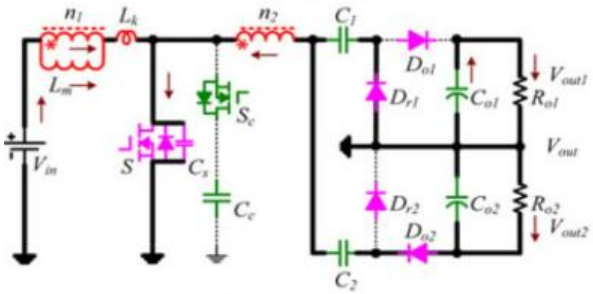
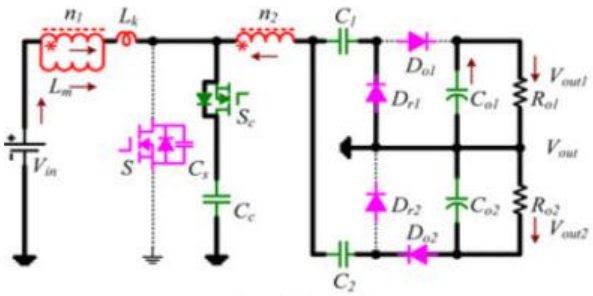


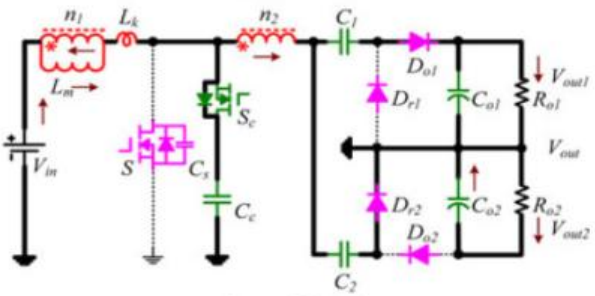
Stage 1 [t_0~t_1]



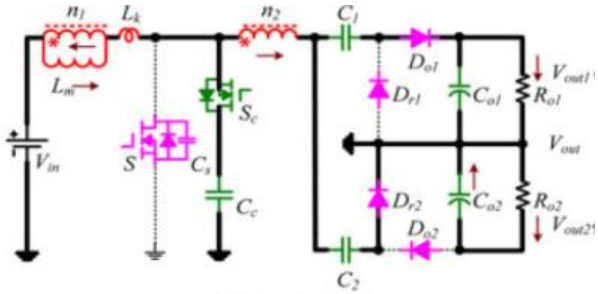
Stage 2 [t_1~t_2]



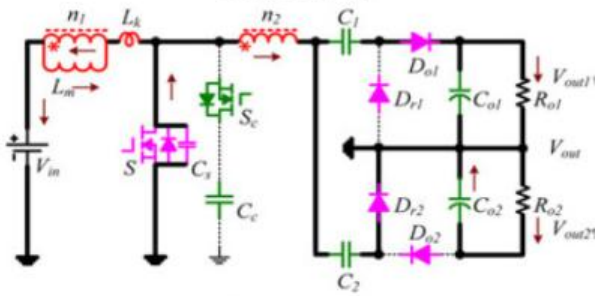
Stage 3 [t_2~t_3]



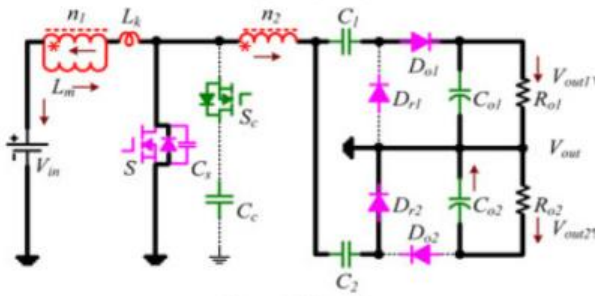
Stage 4 [t_3~t_4]



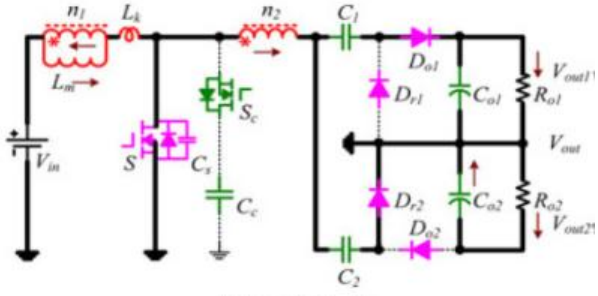
Stage 5 [t_4~t_5]



Stage 6 [t_5~t_6]



Stage 7 [t_6~t_7]



Stage 8 [t_7~t_8]

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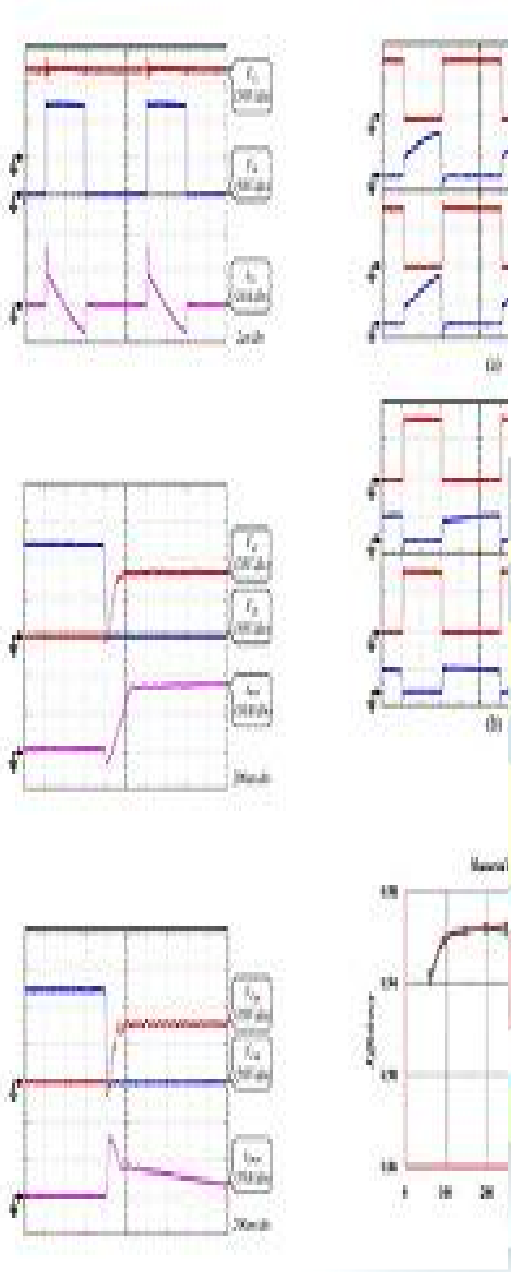

Fig:a)clamp circuit performance b)ZVS on performance of main switch c) ZVS-on performance of clamp switch

4. CONCLUSION:

The gate–source voltage, drain–source voltage, and currentwaveforms of the main and clamp switches are shown in Figs. 9and 10, respectively. It can be found that ZVS turn-on conditions are realized for both the main and clamp switches during the whole switching cycle, which reduces the switching losses significantly.

The voltage and current waveforms of the four diodes are illustrated in Fig. 11. It is shown that the voltage stresses of these four diodes are equal to half of the output voltage and the reverse-recovery problem of diodes is partly solved.

The measured efficiency of the prototype at different loads under different input voltages is sketched in Fig. 12. The highest efficiency of the converter is 96.5%, and the efficiency is higher than 94% over a wide load range.

In order to provide a neutral point terminal for the half-bridge- based inverters, this paper has proposed a single-phase high step- up converter which not only boosts the relatively low PV voltage to a high bus voltage but also offers a neutral point output voltage without any additional active switches and magnetic components. This converter presents some clear main advantages.

1) By combining and integrating two symmetrical high step- up converters, a neutral point terminal is created, which meets the input voltage requirement of the half-bridge-based inverter.

2) A coupled inductor multiplier which consists of a secondary winding of the coupled inductor, two switched capacitors and two regenerative diodes are employed in the converter to extend the voltage gain and reduce the voltage stress of the switches. So the high performance switches with low RDS–on are adopted to reduce the conduction losses and improve the efficiency.

3) The ZVS condition is achieved for all the active switches, which reduces the switching losses greatly, especially in high-frequency and high-power applications. Finally, a 500-W prototype has been built to verify the theoretical analysis and the experimental results have demonstrated that the proposed converter is a good candidate for the half- bridge-based PV inverter systems. It should be also pointed out that the input current of the proposed converter is pulsed, which has some negative influence on the input voltage source,especially in a little large power conversion applications.

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