ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Special Issue 22, April 2016

AN AREA EFFICIENT MULTIBAND DIVIDER WITH INTEGRATED P AND S COUNTER USING 32nm CMOS TECHNOLOGY

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***Abstract*—In this paper, an area efficient hybrid multiband divider with integrated P and S counter for IEEE802.15.4 and 802.11a/b/g WLAN frequency synthesizer is proposed and designed in 32nm CMOS technology. The proposed multiband divider consists of dynamic TSPC D flip flop based Multimodulus prescaler and static D flip flop based integrated P and S counter. The proposed multiband divider is well suited for low power applications.**

***Index Term*—**DFF, prescaler, dynamic and static logic, frequency divider, true single phase clock (TSPC).

I. INTRODUCTION

Wireless LAN (WLAN) in the multigigahertz bands, such as HiperLAN II and IEEE 802.11a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like IEEE802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer. The integrated synthesizers for WLAN applications at 5 GHz reported in [1] and [2] consume up to 25 mW in CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range.The best published frequency synthesizer at 5 GHz consumes 9.7mWat 1-V supply, where its complete divider consumes power around6 mW [3], where the first-stage divider is implemented using the source-coupled logic (SCL) circuit [4], which allows higher operating frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers. The TSPC [5] and E-TSPC [6] designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem [5]. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5 GHz [11] The frequency synthesizer reported in [6] uses an E-TSPC prescaler as the first-stage divider, but the divider consumes around 6.25 mW. The TSPC and E-TSPC design are well suited for dynamic logic latches. These designs are able to drive the dynamic latches with a single clock phase and avoid the skew problem. The Multimodulus prescaler which is one of the functional in the frequency divider often consumes more power because it operates in high frequency. In this paper a new low power Multimodulus prescaler using 5T TSPC and static D flip flop based integrated P and S counter is proposed to achieve the low power consumption by reducing the switching activities and loss of signal at low frequency.

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II. DESIGN CONSIDERATIONS

The key parameters of high speed digital circuits are propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated by the method which is given below

$$f_{max} = \frac{1}{t_p\ LH + t_p\ HL} \qquad (1)$$

where t_p LH t_p HL are the propagation delays of the low-to-high and high-to-low transitions of the gates, respectively. The total power consumption of the digital circuits is determined by the switching and short circuit power [10]. The switching power is linearly proportional to the operating frequency and is given by the sum of witching power at each output node as in

$$p_{switching} = \sum_{i=1}^{n} f_{clk}\, C_{Li}\, V_{dd}^2 \qquad (2)$$

where, n is the number of switching nodes, f_{clk} is the clock frequency, C_{Li} is the load capacitance at the output node of the ith stage, and V_{dd} is the supply voltage. Normally, the dynamic circuits when there exist direct paths from the supply to ground which is given by

$$P_{SC}=I_{SC} * V_{dd} \qquad (3)$$

Where, I_{SC} is the short circuit current. In CMOS circuit, only for a very small period within which the pMOS and then MOS are turned on simultaneously. Thus, the direct path power consumption is considered as negligible [6]. However, at high frequencies this short circuit power consumption can increase significantly. To eliminate the short circuit current in this paper TSPC based multimodulus prescaler and static based integrated P and S counter is proposed.

III. 5T TSPC D FLIP FLOP

The prescaler is designed using the 5T TSPC D flip flop shown in Figure 2 consumes less switching power. This flip-flop is built using 3 nMOS transistors and 2 pMOS transistors. It is the positive edge D latch. When CLK and input IN are high then the transistors M1, M5 are OFF and remaining transistors M2, M3, M4 are ON. The output becomes high. During ON clock period whatever is the value of input it becomes output. This flip flop reduces the number of clocking transistors [7].

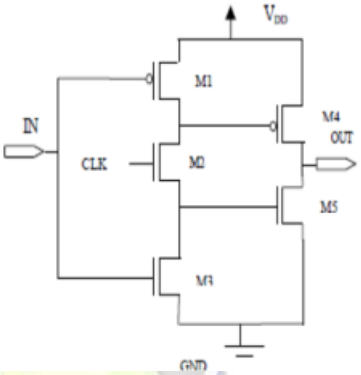

Figure 1. 5t TSPC D flip flop

IV. LOW POWER 2/3 PRESCALER

The low power 2/3 which consists of two D-flip-flops and two NOR gates embedded in the flip-flops as in Figure 3. The reduction of clock load results in low power consumption in the prescaler design. The operation of the prescaler using this flip flop is given below

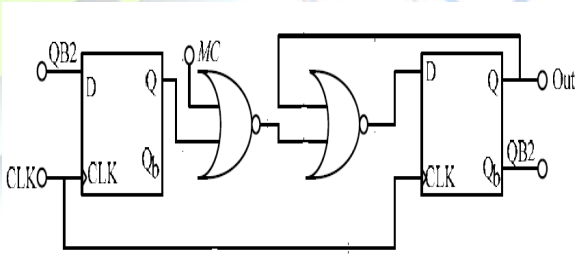

Figure 2. 2/3 prescaler using 5T TSPC D flip flop

Case 1:

When logic signal *MC* switches from '0' to '1', the prescaler switches to divide-by-2 mode.

Case 2:

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When logic signal MC switches from "1"to "0," the logic value at the input of DFF1 is transferred to the input of DFF2 as one of the input of the NOR gate embedded in DFF1 is "0" and the wideband prescaler operates at the divide-by-3 mode Thus by reducing the clock load the overall power consumption of prescaler is reduced more than 25% in the divide by 2 operations.

V. MULTIMODULUS 32/33/47/48 PRESCALER

The multimodulus prescaler can divide the input frequency by 32, 33, 47, and 48 is shown in Figure 3. The multimodulus prescaler consists of the wideband 2/3 (N1 / (N1 + 1)) prescaler, four asynchronous TSPC divide-by-2 circuits ((AD) = 16) and combinational logic circuits to achieve multiple division ratios. Besides the usual MOD signal for controlling N / (N + 1) divisions, the additional control signal Sel is used to switch the prescaler between 32/33and 47/48 modes

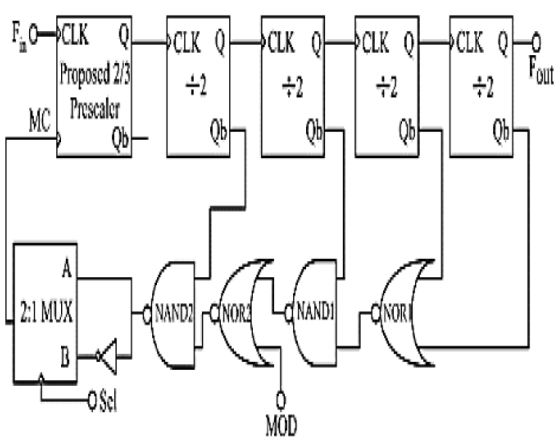

Figure 3. Multimodulus 32/33/47/48 Prescaler

Case 1: Sel = 0

When Sel = 0, the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC = 1, the 2/3 prescaler operates in the divide-by-2 mode and when MC = 0, the 2/3 prescaler operates in the divide-by-3 mode. If MOD = 1, the NAND2 gate output switches to logic "1" (MC = 1) and the wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multimodulus prescaler is

$$N = (AD * N1) + (0 * (N1 + 1)) = 32 \quad (4)$$

where N1 = 2 and AD = 16 is fixed for the entire design. If MOD = 0, for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the divide-by-3 mode. The division ratio N + 1 performed by the multimodulus prescaler is

$$N + 1 = ((AD - 1) * N1) + (1 * (N1 + 1)) = 33 \quad (5)$$

Case 2: Sel = 1

When Sel = 1, the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal . If MC = 1, the 2/3 prescaler operates individe-by-3 mode and when MC = 0, the 2/3 prescaler operates individe-by-2 mode which is quite opposite to the operation performed when Sel = 0. If MOD = 1, the division ratio N + 1 performed by the multimodulus prescaler is same as (4) except that the wideband prescaler operates in the divide-by-3 mode for the entire operation given by

$$N + 1 = (AD * (N1 + 1)) + (0 * N1) = 48 \quad (6)$$

If MOD = 1, the division ratio N performed by the multimodulus prescaler is

$$N = ((AD - 1) * (N1 + 1)) + (1 * N1) = 47 \quad (7)$$

However at the very low frequency the TSPC flip flop cannot hold the value, it leads to drop the signal i.e. degradation of the signal. As per the

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ISSN 2394-3785 (Online)
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concern of signal degradation, the second part of the frequency divider i.e integrated P and S counter is designed using static D flip flop. The usage os static D flip flop leads to static power consumption.

The static power of a Complementary Metal Oxide Semiconductor circuits is the power dissipated during steady state conditions. For nanoscale Very Large Scale Integration circuits, the leakage current is due to mainly for sub threshold voltage. Although dynamic power is dominant for technologies at 0.18µm and above, leakage (static) power consumption becomes another dominant factor for 0.13µm and below. One of the main contributors to static power consumption in Complementary Metal Oxide Semiconductor is subthreshold leakage current i.e., the drain to source current when the gate voltage is smaller than the transistor threshold voltage. Power consumption is dominated by leakage power dissipation when the device dimension brought down to sub-22 nm technology. Here, low power flip flop is choose to meet the requirement of low power consumption and less leakage current without any data degradation.

VI. STATIC LOW POWER D FLIP FLOP

The low power D flip flop is shown in Figure . which is one of the fastest classical structures and its main advantage is the short direct path and low power feedback. It is basically a Master Slave flip flop structure and it consists of two data paths. A network restructuring low power technique is used in this design produces lower delay. When the CLK signal is at logic level 'HIGH' and CLK' is at logic level 'LOW'. In this state, the Master latch consisting of M1 and INVI is functional and the inverse of data at input D is stored to an intermediate node X. When the clock is at logic level 'LOW', CLK signal is at logic level 'LOW' and CLK' is at logic level 'HIGH'. In this state, the Slave latch consisting of M6 and a regenerative feedback loop in master becomes functional and holds the data in Y and produces the data in output Q. In next CLK cycle master latch becomes active and the feedback loop in slave holds the data in Q [5].

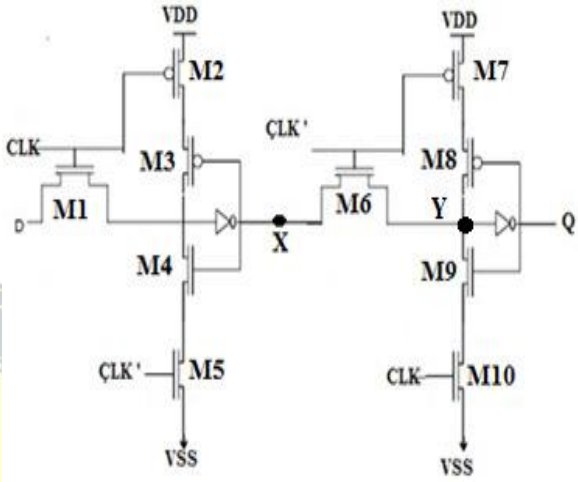

Figure 4. Static Low power D flip flop

VII. DIVIDE BY 2 CIRCUIT

The D flip flop is a binary counter. Here the inverted output terminal Q (NOT-Q) is connected directly back to the Data input terminal D giving the device "feedback" as shown in Figure 5. By feeding the inverted Q into the D input, the output pulses at Q have a frequency that are exactly one half (f ÷ 2) that of the input clock frequency it means that every time we get a rising edge on the clock signal, our

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output will flip states.

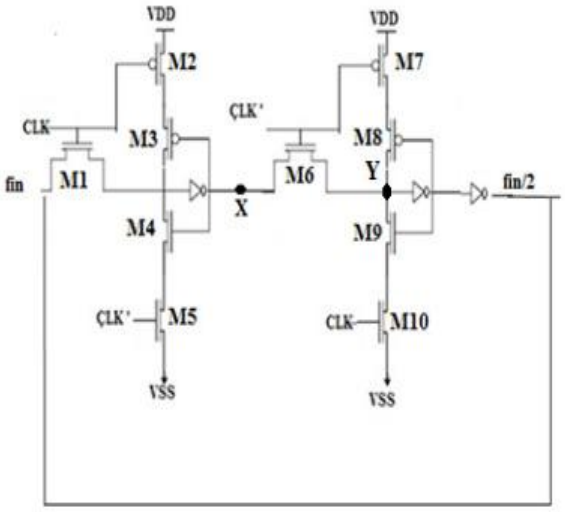

Figure 5. Static Divide by 2 circuit

VIII. INTEGRATED P AND S COUNTER

The Integrated P&S counter is shown in Figure 5. As it is apparent, this counter consists of a divide-by-128 (P counter) that is made up of 7 divide-by-2. Digital circuit consists of XNOR gates (X0 – X5), AND gate and a RESETSET Flip Flop (RSFF). This digital section has replaced S counter in conventional ones and has the duty to control modulus bit of dual modulus prescaler. A1 gate is driven by XNOR gates (X0 – X5). When inputs of XNOR equal (both of them are 0 or 1), output of XNOR gate is logic one. So when the value of P counter (P6P5P4P3P2P1P0) is equal to predefined C number (1C5C4C3C2C1C0), output of A1 gate becomes logic 1 (CC5- C0 bits are defined by transceiver system that changes the frequency channel of PLL). In this moment, as P6 is 1 as well, RSFF is set by A2 gate and dual modulus prescaler divide input frequency by N. When P6 changes to 0, RSFF is reset and dual modulus prescaler return to divide-by-(N + 1) state. Christo Ananth et al. [8] proposed a system, this paper presents an effective field programmable gate array (FPGA)-based hardware implementation of a parallel key searching system for the brute-force attack on RC4 encryption. The design employs several novel key scheduling techniques to minimize the total number of cycles for each key search and uses on-chip memories of the FPGA to maximize the number of key searching units per chip. Based on the design, a total of 176 RC4 key searching units can be implemented in a single Xilinx XC2VP20-5 FPGA chip. Operating at a 47-MHz clock rate, the design can achieve a key searching speed of 1.07 x 107 keys per second. Breaking a 40-bit RC4 encryption only requires around 28.5 h.

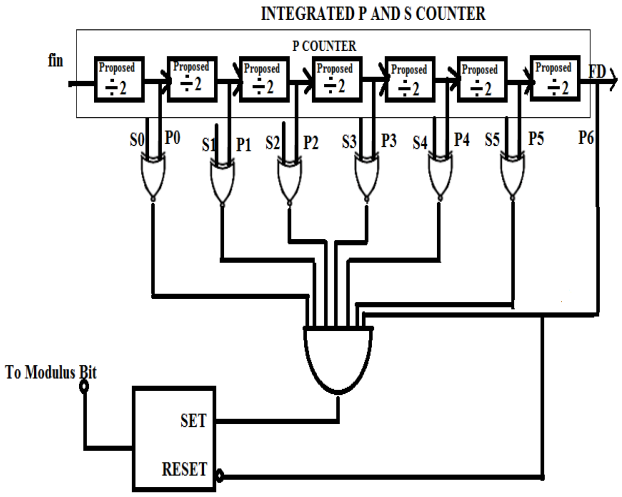

Figure 6. Integrated P and S counter

IX. SIMULATION RESULTS

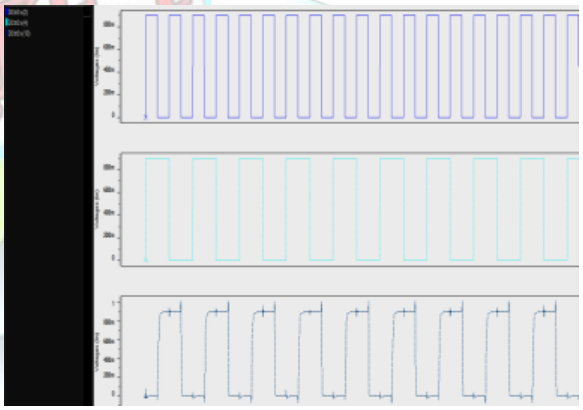

Figure 7. Simulation result of 5T TSPC D flip flop at an input frequency of 2.4GHz

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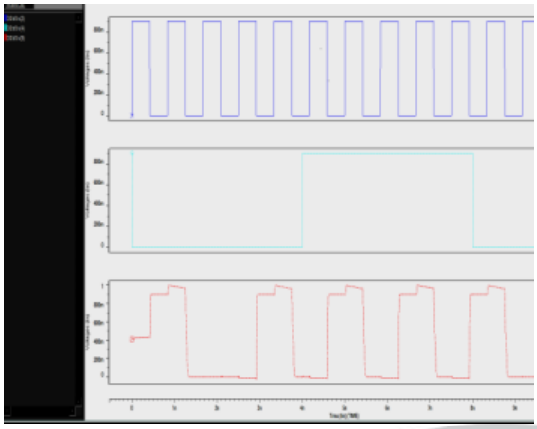

Figure 8. Simulation result of 2/3 prescaler at an input frequency of 2.4GHz

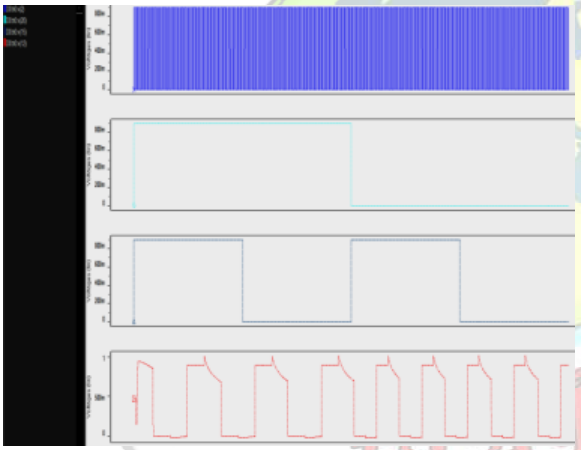

Figure 9. Simulation result of Multimodulus prescaler at an input frequency of 2.4GHz

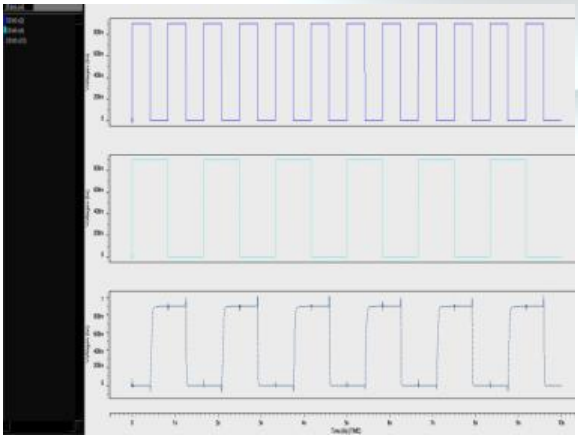

Figure 10. Simulation result of static D flip flop at an input frequency of 2.4GHz

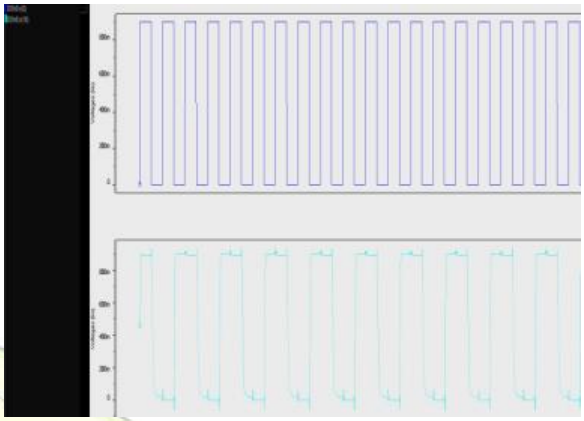

Figure 11. Simulation result of divide by 2 using static flip flop at an input frequency of 2.4GHz

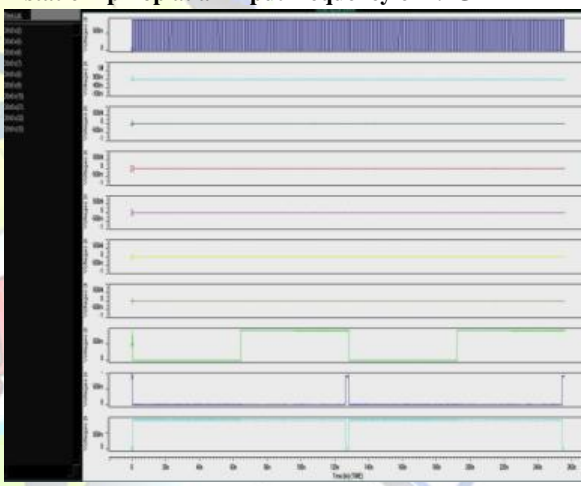

Figure 12. Simulation result of integrated P and S counter at an input frequency of 2.4GHz

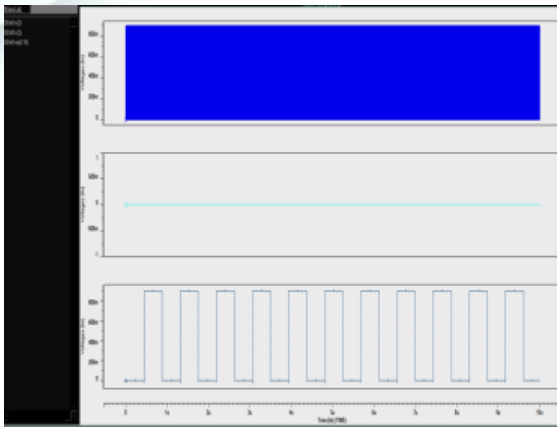

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Figure 13. Simulation result of frequency divider at an input frequency of 2.4GHz

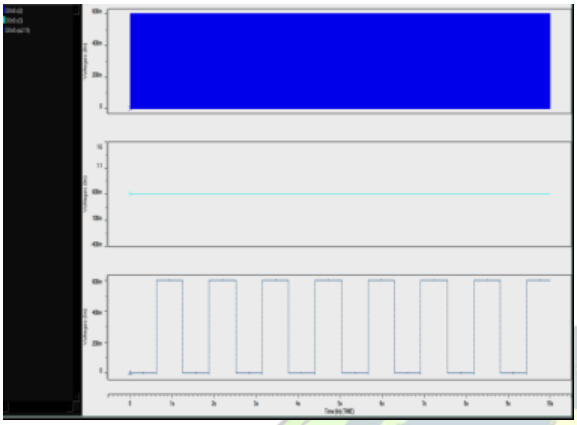

Figure 14. Simulation result of frequency divider at an input frequency of 5.818GHz

Table 1- Performance Analysis

Functional blocks	Average Power (µW)	Delay (ps)	Power Delay Product(J)
TSPC 5T D FF	0.9099	20.493	0.0186
2/3 prescaler	1.831	12.379	0.02305
Multimodulus prescaler	5.976	150	0.01770
Static low power D flip flop	4.16	16.545	0.6884
Int. P and S counter	42.19	411.21	17.348
FD at 2.4GHz	28.16	409.11	11.520
FD at 5.818GHz	57.76	432.11	24.958

X. CONCLUSION

An area efficient multiband divider has been proposed. The design of low power 5T TSPC based multimodulus prescaler and static integrated P and S counter has been designed and it is simulated in HSpice tool using 32nm CMOS technology. The proposed multiband divider consumes 28.16µW and 57.76µW at 2.4GHz and 5.818GHz . The proposed multiband divider can be used in low power frequency synthesizer and it is well-suited for Zigbee, IEEE 802.15.4 and IEEE 802.11a/b/g WLAN applications in reduced nanometer level.

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