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DESIGN AND VERIFICATION OF LPDDR4 CONTROLLER AND DRAM

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Abstract–*Low Power Double Data Rate 4(LPDDR4) is the recent technology designed for increasing memory bandwidth, low-power, high-performance, boost memory speed and efficiency for mobile computing devices such as smart phones, tablets, and ultra-thin notebooks. LPDDR4 will eventually operate at an I/O rate of 4266 MT/s, twice that of LPDDR3.LPDDR4's LVSTL (Low-Voltage Swing-Terminated Logic) I/O signaling voltage of 367 or 440mV is less than 50% the I/O voltage swing of LPDDR3. The operating voltage was reduced from the 1.2V of previous generations to 1.1V. This paper represents the overall design and verification of Low Power Double Data Rate 4(DDR4) memory controller. In this paper UVM (Universal Verification Methodology) is used to design the LPDDR4.*

Keywords–LPDDR4, UVM Methodology, Smartphone, RAM Technology, Memory Controller.

INTRODUCTION

The Double Data Rate (DDR) interfaces aim at addressing parallel digital communications between μ-processors and memories. Various DDR standards exist for specific applications including DDRx standard for general-purpose application, GDDRx standard for graphical application requiring high-bandwidth capability and LPDDRx Standard for mobile application requiring low power feature.

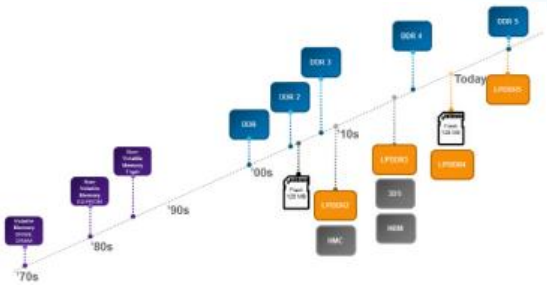

Fig.1. Memory Technology Evolution

LPDDR4 is designed to be a single 32-bit wide die with two independent 16-bit wide channels. This is the first traditional DDR SDRAM that defines more than one channel for the die. The LPDDR4 JEDEC standard describes a single device with two independent channels on one DRAM die. It also includes package options that include multi-die packages with four independent channels.

Power efficiency for the I/O interface is about 2.3mW/Gb/s/pin with 1.1V supply in 2y-nm DRAM process, which is 31% lower than that of LPDDR3. LPDDR4 offers huge bandwidth in a physically small PCB area and volume; up to 25.6 GByte/s of bandwidth at a 3,200 Mbps data rate from a single 15mmx15mm LPDDR4 package when two dies are packaged together.

Fig.2. LPDDR4 Energy Efficiency

LPDDR4 builds on the success of LPDDR2 and LPDDR3 by adding new features and introducing a major architectural change. The demands on higher bandwidth with reduced power consumption in mobile market are driving mobile DRAM with advanced design techniques. Proposed LPDDR4 in this paper achieves over 39% improvement in power efficiency and over 4.3 Gbps data rate with 1.1 V supply voltage. These are challenging targets compared with those of LPDDR3.This work describes design schemes employed in LPDDR4 to satisfy these requirements, such as multi-channel-per-die

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architecture, multiple training modes, low-swing interface, DQS and clock frequency dividing, and internal reference for data and command-address signals. What's more, DRAM memory bandwidth increases in line with screen resolution and processor performance, which leads to even more power drain. 4K video (3840 x 2160), which was originally conceived for home entertainment and large TV screens, has already found a place on the spec sheets of recent laptops, but the prospect of 4K used for tablet devices is a true innovation.

I. BLOCK DIAGRAM OF LPDDR4

The low power DDR4 system has following blocks.

-Memory model

-Memory controller

-Monitor

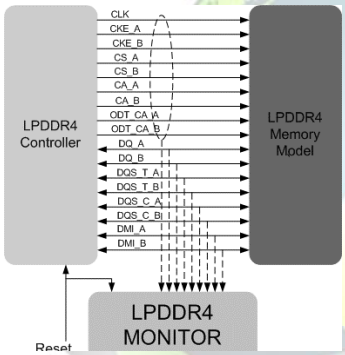

Fig.3. Memory Technology Evolution

II. UNIVERSAL VERIFICATIONMETHODOLY (UVM)

The most important phases are represented in fig.4; Phases are ordered steps of execution implemented as methods. When we derive a new class, the simulation of our test bench will go through these different steps in order to construct, configure and connect the test bench component hierarchy.

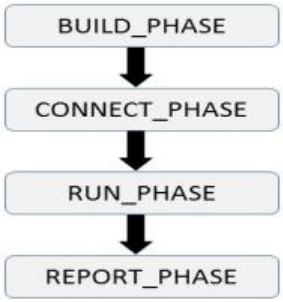

Fig.4. Partial list of UVM phases

UVM provides the best framework to achieve coverage-driven verification (CDV). CDV combines automatic test generation, self-checking test benches, and coverage metrics to significantly reduce the time spent verifying a design.

The purpose of CDV is to:

— Eliminate the effort and time spent creating hundreds of tests.

— Ensure thorough verification using up-front goal setting.

— Receive early error notifications and deploy run-time checking and error analysis to simplify debugging.

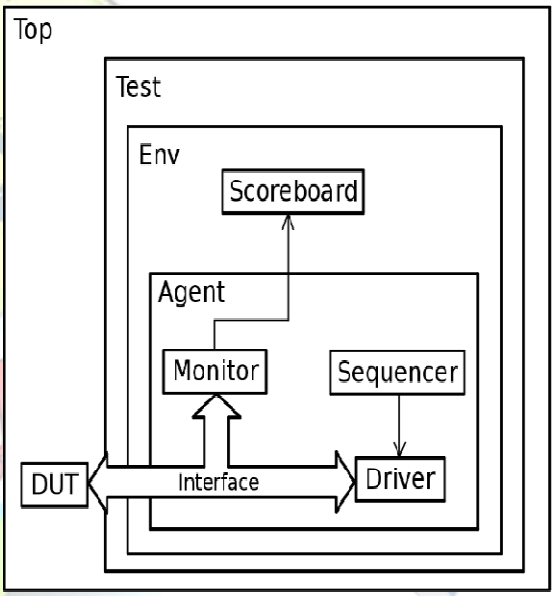

Fig.5. Typical UVM test bench

III. VERIFICATION COMPONENT OVERVIEW

Data Item (Transaction) - Data items represent the input to the device under test (DUT). Examples include networking packets, bus transactions, and instructions.

Driver (BFM) - A driver is an active entity that emulates logic that drives the DUT. A typical driver repeatedly receives a data item and drives it to the DUT by sampling and driving the DUT signals.

Sequencer-A sequencer is an advanced stimulus generator that controls the items that are provided to the driver for execution. By default, a sequencer behaves similarly to a

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simple stimulus generator and returns a random data item upon request from the driver.

Monitor-A monitor is a passive entity that samples DUT signals but does not drive them. Monitors collect coverage information and perform checking.

Agent-UVM recommends that environment developers create a more abstract container called an agent. Agents can emulate and verify DUT devices. They encapsulate a driver, sequencer, and monitor. Verification components can contain more than one agent.

Environment-The environment (env) is the top-level component of the verification component. It contains one or more agents, as well as other components such as a bus monitor. The env contains configuration properties that enable you to customize the topology and behavior and make it reusable.

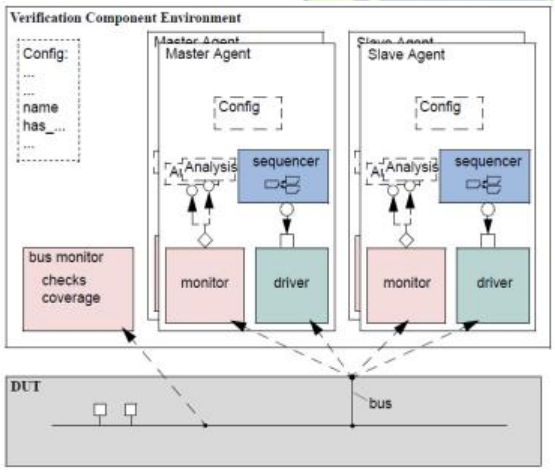

Fig.6. Typical Verification Component Environment

IV. TRANSACTION LEVEL MODELLING

TLM, transaction-level modeling, is a modeling style for building highly abstract models of components and systems. It relies on transactions, objects that contain arbitrary, protocol-specific data to abstractly represent lower-level activity.In practice, TLM refers to a family of abstraction levels beginning with cycle-accurate modeling, the most abstract level, and extending upwards in abstraction as far as the eye can see. Christo Ananth et al. [2] proposed a system which can achieve a higher throughput and higher energy efficiency. The S-BOX is designed by using Advanced Encryption Standard (AES). The AES is a symmetric key standard for encryption and decryption of blocks of data. In encryption, the AES accepts a plaintext input, which is limited to 128 bits, and a key that can be specified to be 128 bits to generate the Cipher text. In decryption, the cipher text is converted to original one. By using this AES technique the original text is highly secured and the information is not broken by the intruder. From that, the design of S-BOX is used to protect the message and also achieve a high throughput, high energy efficiency and occupy less area.

Common transaction-level abstractions today include: cycle-accurate, approximately-timed, loosely-timed, untimed, and token-level. TLM-1and TLM-2.0 are two TLM modeling systems which have been developed as industry standards for building transaction-level models. Both were built in System and standardized within the TLM Working Group of the Open SystemC Initiative (OSCI). TLM-1 achieved standardization in 2005 and TLM-2.0 became a standard in 2009.Transaction-level interfaces define a set of methods that use transaction objects as arguments. A TLM port defines the set of methods (the application programming interface (API)) to be used for a particular connection, while a TLM export supplies the implementation of those methods. Connecting a port to an export allows the implementation to be executed when the port method is called.

V. DEVELOPING REUSABLE VERIFICAION COMPONENT

This describes the basic concepts and components that make up a typical verification environment. It also shows how to combine these components using a proven hierarchical architecture to create reusable verification components and when developing a verification component:

—Modeling Data Items for Generation
—Transaction-Level Components
— Creating the Driver
— Creating the Sequencer
— Creating the Monitor
— Instantiating Components
— Creating the Agent
— Creating the Environment
— Enabling Scenario Creation
— Managing End of Test
—Implementing Checks and Coverage

VI. READ AND WRITE OPERATION

The LPDDR4-SDRAM provides a fast column access operation. A single Read or Write command will initiate a burst read or write operation, where data is transferred

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to/from the DRAM on successive clock cycles. Burst interrupts are not allowed, but the optimal burst length may be set on the fly. For READ operations the pre-amble is 2*tCK, but the pre-amble is static (no-toggle) or toggling, selectable via mode register. LPDDR4 will have a DQS Read post-amble of 0.5*tCK (or extended to 1.5*tCK). Standard DQS post amblewill be 0.5*tCK driven by the DRAM for Reads.

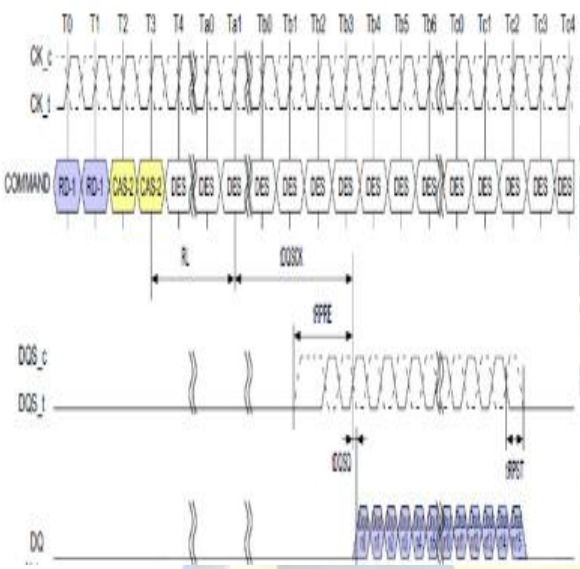

Fig.7. Toggling Preamble and 0.5nCK Post amble

A burst Read command is initiated with CS, and CA[5:0] asserted to the proper state at the rising edge of CK,the read latency (RL) is defined from the last rising edge of the clock that completes a read command (Ex: the second rising edge of the CAS-2 command) to the rising edge of the clock from which the tDQSCK delay is measured. The first valid data is available RL * tCK + tDQSCK + tDQSQ after the rising edge ofClock that completes a read command.

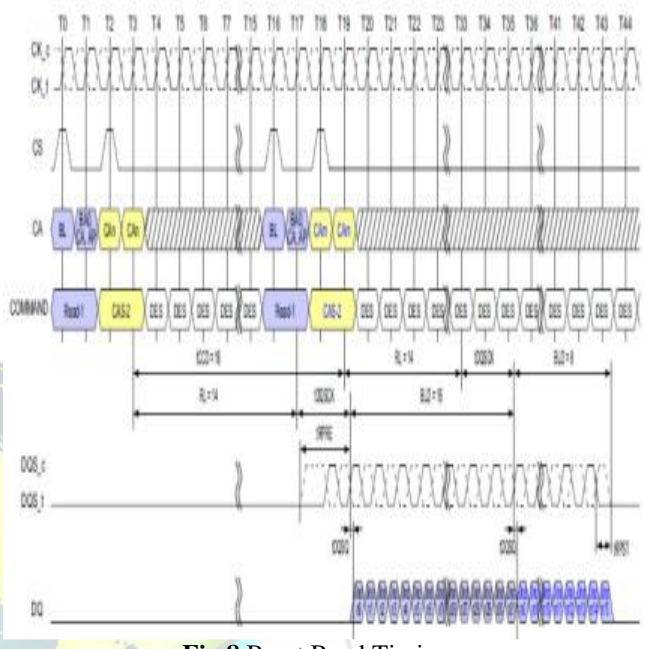

Fig.8. Burst Read Timing

The data strobe output is driven tRPRE before the first valid rising strobe edge. The first data-bit of the burst is synchronized with the first valid (i.e., post-preamble) rising edge of the data strobe. Each subsequent data out appears on each DQ pin, edge-aligned with the data strobe. At the end of a burst the DQS signals are driven for another half cycle post-amble, or for a 1.5-cycle post amble if the programmable post-amble bit is set in the mode register.

There are eight possible combinations for LPDDR4 device with DM and DBIdc function. LPDDR4 SDRAM supports the function of Data Mask and Data Bus inversion. Its details are shown below.

- LPDDR4 device supports Data Mask (DM) function for Write operation.
- LPDDR4 device supports Data Bus Inversion (DBIdc) function for Write and Read operation.
- LPDDR4 supports DM and DBIdc function with a byte granularity.
- DBIdc function during Write or Masked Write can be enabled or disabled through MR3 OP[7].
- DBIdc function during Read can be enabled or disabled through MR3 OP[6].

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• DM function during Masked Write can be enabled or disabled through MR13 OP[5].
• LPDDR4 device has one Data Mask Inversion (DMI) signal pin per byte; total of 2 DMI signals perChannel.
• DMI signal is a bi-directional DDR signal and is sampled along with the DQ signals for Read and Write or Masked Write operation.

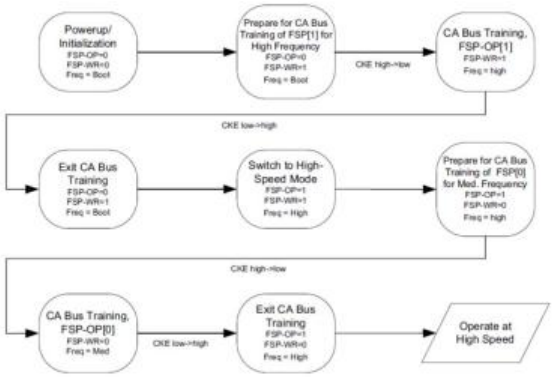

Fig.9. Two Frequency Set-Points

VII. CONCLUSION

This paper proposed a design and verification for LPDDR4 memory controller with LVSTL driver. LPDDR4 memory will be used in mobile devices to enable powerful computing, high-resolution video, larger displays with more pixels, and an enhanced user experience, all while maintaining battery life. LPDDR4 is expected to rapidly become mainstream technology for mobile platforms. The purpose of this specification is to define the minimum set of requirements for JEDEC compliant 4 Gb through 32 Gb for x16x2channel SDRAM devices. LPDDR4 has 2-channel-per-die architecture for a shorter latency and lower power consumption. The LPDDR4 achieves the 4.35 Gbps at 1.1 V and over 30% power reduction per bandwidth compared with the previous generation device (LPDDR3).This design is simulated in Modelsim by Mentor graphics tool and successfully synthesized in and EDA playground tool.

VIII. FURTHER ENHANCEMENT

Further enhancement can be done such as HBM (High Bandwidth Memory), HMC (Hybrid Memory Cube).so that the Memory size can be reduced and low power consumption, High speed is achieved.

IX. ACKNOWLEGMENT

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