ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Special Issue 19, April 2016

Mismatch Correction of Analog-to-Digital Converter in Digital Communication Receiver

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Abstract- **To overcome the errors caused by the offset, gain, sample-time, and bandwidth mismatches among time-interleaved analog-to-digital converters in a digital communication receiver. The errors introduced by these mismatches are corrected using least-mean-square adaptation. Gain, sample-time, and bandwidth mismatches are corrected by modifying the operation of the adaptive receive equalizer itself to minimize the hardware.**

Index Terms – **Analog-to-digital conversion, calibration, communication receiver.**

1. Introduction

In Digital communication receiver equalizer is overcome the effect of Intersymbol Interference.The residual effect of all the transmitted bits over ith transmitted bit. Consider a baseband signal in which there is a direct representation of binary symbol 0 and 1 in terms of equivalent amplitude levels. In the bandpass signal there is a representation of the symbols by using high frequency signal in RF range.Equalization is to reduce the ISI and convert analog input to digital output and also mismatch in bandwidth, offset, gain, sample time.

Digital communication receivers take an analog input from the communication channel and extract digital data that were sent from the far-end transmitter. In modern CMOS technologies,digital processing of signals is more attractive than analog processing due to the low power-supply voltage, which makes analog design difficult, and the superior capabilities of computer-aided design and verification tools for complex digital systems. In addition, digital blocks can take full advantage of scaling as CMOS technology advances. An extreme example of a mixed-signal receiver would consist of an analog-to-digital converter (ADC) digitizing the received analog signal from the channel, followed by digital-signal-processing (DSP) blocks. In such a system, the received signal undergoes minimal analog processing, and reducing the analog processing before the ADC increases the requirements on the ADC. When the received signal has a wide dynamic range, a high-resolution ADC is

required. The resolution required in the ADC will be typically at least 10 bits, because it must not overload when receiving a strong signal and must give a reasonable output signal-to-quan-tization-noise-and-distortion ratio when receiving a weak signal. For example, if the range of the received signal is 30 dB, the peak-to-rms ratio of the receive signal is 12 dB, and the desired signal-to-noise-and-distortion ratio (SNDR) is 30 dB, then an ADC with 12 bits of resolution is required. While high-resolution ADCs can be built, their conversion rates are limited.

If the data rate is high, such a receiver may be limited by the conversion rate of the high-resolution ADC. Time interleaving of ADCs is an attractive way to increase the overall conversion rate in a given technology while providing high resolution. Time interleaving is a technique involving multiple ADC channels clocked with different clock phases; each ADC channel samples the input in turn. With M ADC channels operating in parallel, the overall sampling rate increases by the factor M over that of a single channel. However, mismatches among he time-interleaved ADCs generate undesired spectralcomponents and can significantly degrade the SNDR of the system [2]–[4]. Mismatches that have been considered in the past are gain mismatches, offset mismatches, sample-time errors, and bandwidth mismatches among the time-interleaved ADC channels [3]. Without any calibration, careful layout techniques have shown a limitation of about 7–8 bits of accuracy because of these mismatches [2].

In some time-interleaved ADCs, a front-rank sample-and- hold amplifier (SHA) has been used to sample the input at the overall sampling rate, avoiding sample-time errors and bandwidth mismatches that could arise when sampling the input using a different SHA in each channel [5]. However, significant power dissipation is

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required to provide the required SHA bandwidth of 5–10 times the input signal bandwidth in practice. When a front-rank SHA is not used, the sampling operation can be done by a SHA in each time-interleaved channel. However, the interleaved SHAs each have finite bandwidth, and these bandwidths can be mismatched [3], [4]. In addition, other mismatches between the SHAs as well as mismatches of sampling-clock delays can introduce sample-time errors. Several adaptive correction techniques to overcome mismatches among time-interleaved ADCs in digital communication receivers have been presented. Christo Ananth et al. [1] discussed about Improved Particle Swarm Optimization. The fuzzy filter based on particle swarm optimization is used to remove the high density image impulse noise, which occur during the transmission, data acquisition and processing. The proposed system has a fuzzy filter which has the parallel fuzzy inference mechanism, fuzzy mean process, and a fuzzy composition process. In particular, by using no-reference Q metric, the particle swarm optimization learning is sufficient to optimize the parameter necessitated by the particle swarm optimization based fuzzy filter, therefore the proposed fuzzy filter can cope with particle situation where the assumption of existence of "ground-truth" reference does not hold. The merging of the particle swarm optimization with the fuzzy filter helps to build an auto tuning mechanism for the fuzzy filter without any prior knowledge regarding the noise and the true image. Thus the reference measures are not need for removing the noise and in restoring the image. The final output image (Restored image) confirm that the fuzzy filter based on particle swarm optimization attain the excellent quality of restored images in term of peak signal-to-noise ratio, mean absolute error and mean square error even when the noise rate is above 0.5 and without having any reference measures.

In this paper, an "all-digital" receiver for digital communi- cation is presented that adaptively corrects the errors caused by gain, offset, sample-time, and bandwidth mismatches in a time-interleaved ADC. The corrections are carried out entirely in the digital domain, so the receiver, including the correction blocks, can take advantage of device scaling as CMOS technology advances. With these correction schemes, a front-rank SHA is not required, which allows many ADC channels to be time interleaved. The offset and gain corrections are performed separately on each ADC channel and require relatively simple hardware.

2. ARCHITECTURE OF DIGITAL-RECEIVER

A block diagram of an "all-digital receiver is shown in Fig.1. In this "all-digital receiver, the only analog circuit is the high-resolution ADC that digitizes the received input signal x(t).The ADC is followed by a digital automatic-gain-control(AGC) block, which scales the digitzed ADC output,a digital adaptive equalizer, which compensated for intersymbol interference (ISI) introduced by the communication channel, and a digital interpolated-timing-recovery (ITR) block.

In Fig. 1, the ADC samples the received signal x(t) at a rate 1/Ts that is somewhat faster than the symbol rate 1/T to provide some oversampling and allow digital timing recovery . This sampling rate is set by a crystal-derived clock. The AGC and equalizer operate at a sampling rate of 1/Ts that is somewhat faster than the symbol rate 1/T. The ITR block uses interpolation to output samples at the symbol rate from the oversampled signal. The resulting signal is sliced at the symbol rate from the oversampled signal. The resulting signal is sliced at the symbol rate to produce an estimate of the transmitted data. The purpose of the AGC shown in Fig. 1 is to scale the digital output from the ADC so that the AGC output can be truncated to fewer bits at its output than at its output than at its input. While high ADC resolution may be needed in part to provide high dynamic range at the ADC input, the signal-to-noise ratio (SNR)
needed in a baseband communication is usually fairly low: typically 20-30dB.

For instance, in the example presented in the last section, the input dynamic range was 30 dB, and a 12-bit ADC was needed. After the AGC, if the signal is scaled perfectly by the AGC, only about 7 bits would be needed to accommodate apeak-to-rms ratio of 12 dB and achieve an SNDR of 30dB.

Such truncation minimizes the number of bits representing the equalizer input and that simplifies the multipliers in the equalizer. The equalizer is an adaptive finite-impulse-response (FIR) filter with enough taps to sufficiently reduce the ISI.

In some receivers, a timing-recovery loop includes a VCO that controls the ADC sampling clock. Inside a decision directed timing-recovery loop that controls the ADC sampling clock, delays through the ADC and equalizer are undesirable. In addition, the changing phase of the ADC sampling clock could introduce significant noise coupling if the ADC samples when the digital circuits are switching.

To avoid these problems, ITR canbe implemented entirely in the digital domain,as shown in the proposed receiver in Fig.1. The inputs to all blocks

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except the slicer are samples at a rate of *1/Ts*, which is greater than the symbol rate. The ITR block uses interpolation to output samples at the symbol rate from the oversampled equalizer output. A tradeoff exists between the complexity of the interpolation filter and the oversampling factor *T/Ts*.

In Fig. 1, the AGC gain, equalizer coefficients, and interpolation filter coefficients in the ITR are determined by feedback that acts to minimize a function of the slicer error e ,which is the difference between the output and input of the slicer in Fig. 1. Minimization of the mean-squared error (MSE) is often the goal, which can be achieved using least-mean-square (LMS) adaptation. In the ITR block, linear interpolation converts e (at a sampling rate of *1/T*) to e (at a sampling rate of 1/Ts) for LMS adaptation in the equalizer and AGC

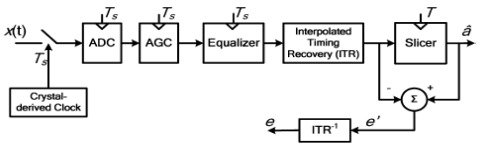

Fig. 1.Blockdiagram of an all-digital communication receiver

The receiver shown in Fig. 1 includes the key functions of gain adjustment, equalization, and timing recovery that are present in most receivers but does not contain all possible receiver blocks. For example, a decision-feedback equalizer, Viterbi detector, echo canceller, or crosstalk canceller(s) could be added. In addition, the functions operating in the digital domain shown in Fig. 1 could be split between the analog and digital domains in other receivers .For example,an analog

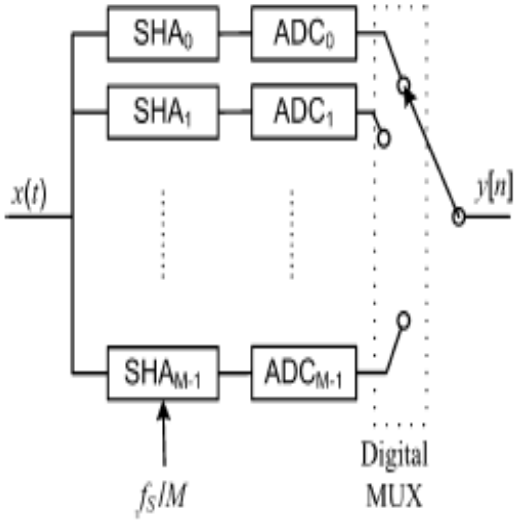

Fig. 2. Block diagram of the time-interleaved ADC

programmable gain amplifier with coarse gain settings could precede the ADC to reduce the required ADC resolution,allowing the AGC shown in Fig. 1 to be used in a fine mode with small gain steps. In addition, an analog pre-equalizer boost to compensate for the roll-off of a typical communication channel. Such an analog equalizer would simplify the task of the digital equalizer and reduce its required length.

A high-performance ADC is required in Fig. 1. To achieve high resolution at sampling rates near and above 1 Gb/s, for example, multiple ADCs could be time interleaved as shown in Fig. 2. Possible applications of time-interleaved ADCs include read channels for magnetic recording and receivers for ten GBased-T Ethernet, backplane, chip-to-chip, and optical communications . At very high conversion rates, many ADC
channels may be needed. As the number of channels increases, the physical separation increases between ADC channels, worsening the channel-to-channel mismatches.

3. MISMATCHES EFFECTS

The ADC input signal x(t) is assumed to be band-limited to half the ADC sampling rate.

A. Gain Mismatch

Gain mismatch between channels stems from mismatches in reference voltages, transistors, and/or passive components. For example, the gain of its input SHA, which may be affected by capacitor ratios, finite opamp gain, and opamp settling time. If the gain of the *kth* interleaved channel is g, the sequence of channel gains.

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The ADC input samples are amplitude modulated by the periodic gain sequence. This modulation causes scaled copies of the input spectrum to appear in the ADC output spectrum at integer multiples of the channel sampling rate *1/MT*.
The undesired copies of the input spectrum centred at frequencies othe than dc effectively increase the noise floor at the ADC output.

B. Offset Mismatch

Offset voltage in the *kth* ADC channel can be modeled by adding a constant to the *kth* channel output. If the offsets are mismatched, they introduce an additive periodic sequence with period *M* in the ADC output. In the frequency components at integer multiplies of the channel sampling rate, reducing the SNR.

C. Sample-Time Errors

Deviations from the ideal sasmple times in each channel stem from different propagation delays through the clock distribution paths, nonideal sampling-clock edges, and mismatches among the transistors that sample the input signal. Sample-time error in channel causes channel k to sample seconds after the previous channel. The sample-time errors are deterministic systematic timing skews and can be positive or negative.

The sequence of sample-time errors are periodic with period *M* .With small sample-time errors, scaled copies of the spectrum of the derivative of the ADC input appear in the ADC output spectrum at integer multiples of the channel sampling rate,increasing the noise floor. The spectral copy centered at dc introduces some filtering of the input signal.

D. SHA Bandwidth Mismatch

In each channel,assume that the ADCs are ideal and the SHA samples the input using a MOS switch in series with a capacitor, which introduces one-pole filtering of the SHA in channel *k* can be modeled during the sample mode by a first-order filter with time constant. The sampled output from this channel is the result of the ADC input signal passing through a linear filter with frequency responses and then being sampled. SHAs with mismatched bandwidths cause filtered copies of

the input spectrum to appear at integer multipies of the channel sampling rate in the ADC output spectrum.

4. SIMULATION

The input signal is equalized to a three-level output signal; the resulting equalized signal is a partial-response (PR4) signal that could be processed by a viterbi detector to achieve a lower bit-error rate (BER) than a simple slicer. However , the correction techniques described are general and would work for any pulse-amplitude- modulated (PAM) signal.

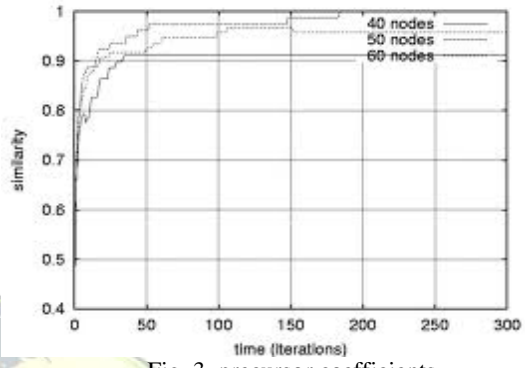

Fig. 3 precursor coefficients

The ADC oversampling rate allows the use of digital ITR. The three-level slicer outputs are zero. The gain G is adapted when a periodic sequence is stored on the disk. During that time, the equalizers are bypassed to eliminate their delay in the gain adaptation loop.

Then G is frozen, and the equalizers and offset-cancellation start to adapt. Then, they continue to adapt while
data decisions are made . Then, they continue to adapt while data decisions are made

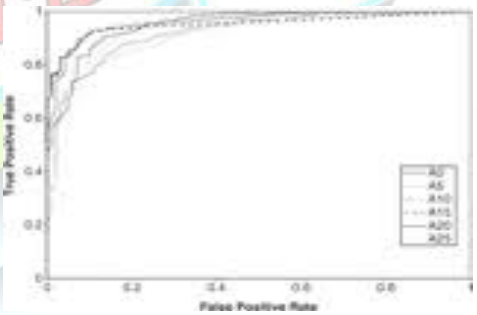
Fig. 4 . precursor coefficients

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ISSN 2394-3785 (Online)
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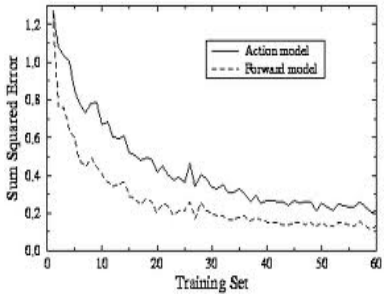

Fig.5 Traning sequence

5. CONCLUSION AND FUTURE WORK

The error caused by offset, gain, sample-time, and bandwidth mismatches the among time-interleaved analog-to-digital converters during data transmission By simulation of offset, gain, sample-time, and bandwidth mismatches .we can reduces the error.

References

[1] Christo Ananth, Vivek.T, Selvakumar.S., Sakthi Kannan.S., Sankara Narayanan.D, "Impulse Noise Removal using Improved Particle Swarm Optimization", International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Volume 3, Issue 4, April 2014,pp 366-370

[2] K.Asami, "An algorithm to improve the performance of M-channel time-interleaved A-D converters,"IEICE Trans.Fundamentals, vol.E90-A, no.12,pp.2846-2852,Dec. 2015.

[3] T. Komuro,S .Sobukawa, H. Sakayori, M. Kono, and H. Kobayashi , "Total harmonic distortion measurement system for electronic devices up to 100MHZ with remarkable sensitivity," IEEE Trans. Instrum. Meas.,vol.56,no.6,pp.2360-2368, Dec. 2015

[4] H.Johansson and P.Lowenborg, "Least-squares filter design technique for the compensation of frequency response mismatch errors in time-interleaved A/D converters,"IEEETrans.Circuits Syst.II,Exp.Briefs,vol. 55, no. 11, pp. 1154-1158, Nov. 2015.

[5] P. Satarzadeh, B. Levy, and P. Hurst, "Bandwidth mismatch correction for a two-channel time-interleaved A/D converter," in Proc. IEEE ISCAS,May 2015, pp. 1705-1708.