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MITIGATION OF POWER CONSUMPTION IN ASYNCHRONOUS DOMINO LOGIC PIPELINE DESIGN USING ECRL GATE

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Abstract: This paper presents mitigation of power consumption in Asynchronous domino logic pipeline.Each pipeline stage in the APCDP circuit is made up of efficient charge recovery logic (ECRL) gate, which carry out the logic part of the stage, and a handshake controller, which handles handshaking with the neighboring stages and provide power to ECRL gates. In the APCDP circuit, ECRL gates acquire power and become alive only when performing useful computations, and idle ECRL gates are not powered and thus have negligible power dissipation. The partial charge reuse (PCR) mechanism can be integrated in the circuit. With the PCR mechanism, part of the charge on the output nodes of an ECRL gate entering the discharge phase can be reused to charge the output nodes of another ECRL gate about to evaluate, reducing the energy dissipation required to complete the evaluation of an ECRL gate. This further saves a lot of power by reducing the overhead of logic circuits. An 8 × 8 array style multiplier is used for evaluating the proposed pipeline method.

1. Introduction:

The semiconductor industry is giving serious consideration to the adoption of asynchronous circuit technology which uses local handshake instead of externally supplied global clock. As technology scaling progresses, the clock design becomes an obstacle to high-performance VLSI systems. Clock distribution is a serious challenge with the requirement of high-speed and low-power in VLSI systems design, and the clock source has large electromagnetic missions which affects circuits design. On the other hand, asynchronous circuits avoid issues related to global clock. It has potential for high-speed, low-power, low electromagnetic interference, and a natural match with heterogeneous system timing. Asynchronous design has recently attracted industry due to its potential for high-speed, low-power, low electromagnetic interference, and a natural match with heterogeneous system timing. Although asynchronous circuit has these

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attractive properties for VLSI systems, it also has some drawbacks.

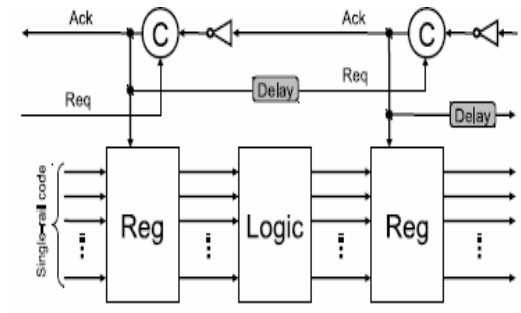
1.1 TYPES OF ASYNCHRONOUS CIRCUIT

Depending on the encoding scheme, asynchronous circuit implementations are separated into two types.

- Bundled-data asynchronous circuit
- Dual-rail asynchronous circuit

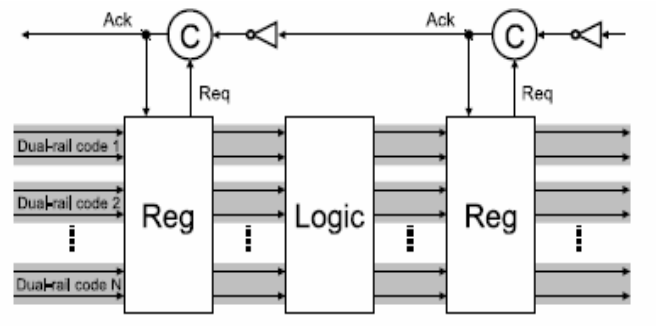
1.1.1 Bundled-data encoding

This is the same encoding as in synchronous circuits: it uses one wire per data bit. The request and the acknowledgement are sent on separate wires with various protocols. These circuits usually assume a bounded delay model, the completion signals being delayed long enough for the calculations to take place. Such circuits are often referred to as *micropipelines*, whether they use a two-phase or four-phase protocol, even if the word was initially introduced for two-phase bundled-data.



Block diagram of bundled rail protocol

1.1.2 Dual-data encoding



1.2 DOMINO LOGIC PIPELINE DESIGN:

Domino logic is the CMOS based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors. It allows a rail to rail logic swing. It was developed to speed up the circuits. The term derives from the fact that in domino logic (cascade structure consisting of several stages),each stage ripples the next stage for evaluation, similar to a Domino failing one after the other. Christo Ananth et al. [1] proposed a system which can achieve a higher throughput and higher energy efficiency. The S-BOX is designed by using Advanced Encryption Standard (AES). The AES is a symmetric key standard for encryption and decryption of blocks of data. In encryption, the AES accepts a plaintext input, which is limited to 128 bits, and a key that can be specified to be 128 bits to generate the Cipher text. In decryption, the cipher text is converted to original one. By using this AES technique the original text is highly secured and the information is not broken by the intruder. From that, the design of S-BOX is used to protect the message and also achieve a high throughput, high energy efficiency and occupy less area.

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3.1 ASYNCHRONOUS DOMINO LOGIC PIPELINE DESIGN

PS0 is a well-known implementation style of asynchronous domino logic pipeline based on dual-rail protocol. It is an important foundation for most lately proposed styles.PS0 is introduced to demonstrate the advantages and problems of asynchronous domino logic pipeline based on dual-rail protocol. Several related designs are also simply introduced. PS0 is designed based on the four-phase dual-rail protocol. The four-phase dual-rail encoding encodes a request signal into the data signal using two wires, (w_t,w_ f). The data value 0 is encoded as (0, 1), and value 1 is encoded as (1, 0), the spacer is encoded as (0, 0); (1, 1) is not used. When transferring the valid data, a spacer is inserted between them. A receiver can easily obtain the valid data by monitoring the two wires.

Table 3.1 Code table for four phase dual rail encoding

	Codeword (w_t,w_f)
Data 0	(0,1)
Data 1	(1,0)
Spacer	(0,0)
Not used	(1,1)

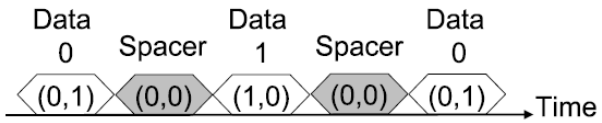

Fig 3.1 Data transfer based on four phase bundled data encoding

3.1.1 Structure of PS0:

In PS0, each pipeline stage is composed of a function block and a completion detector. Each function block is implemented using dual-rail domino logic. Each completion detector generates a local handshake signal to control the flow of data through the pipeline. The handshake signal is transferred to the precharge/evaluation control port of the previous pipeline stage.The diagram shows a block diagram of PS0. Christo

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Ananth et al. [2] proposed a system which contributes the complex parallelism mechanism to protect the information by using Advanced Encryption Standard (AES) Technique. AES is an encryption algorithm which uses 128 bit as a data and generates a secured data. In Encryption, when cipher key is inserted, the plain text is converted into cipher text by using complex parallelism. Similarly, in decryption, the cipher text is converted into original one by removing a cipher key. The complex parallelism technique involves the process of Substitution Byte, Shift Row, Mix Column and Add Round Key. The above four techniques are used to involve the process of shuffling the message. The complex parallelism is highly secured and the information is not broken by any other intruder.

3.2ASYNCHRONOUS PIPELINING:

PCHB is atiming-robust pipeline style that uses quasi-delay insensitivecontrol circuits. Two completion detectors in a PCHBstage: one on the input side (Di) and one on the outputside (Do). The complete cycle of events for a PCHB stage isquite similar to that of PS0, except that a PCHB stage verifiesits input bits. Because of the input completion detector (Di),a PCHB stage does not start evaluation until all input bits arevalid. This design absorbs skew across individual bits in the data paths. Although this design makes PCHB more timingrobust, it causes a two-time overhead in handshake controllogic compared with PS0. Besides, PCHB has the same dual railencoding overhead as PS0. The blockdiagram of precharge half-buffer pipeline (PCHB) shown.

3.2.1.2 LP2/2:

LP2/2 is a high-throughput pipeline style, which has both dual-rail protocol design and bundled-data, protocol design. The block diagram of LP2/2 based on the dual-rail protocol is shown below. LP2/2 improves the throughput of PS0 by optimizing the sequential of handshake events. The handshake speed is accelerated by employing asymmetric completion detectors placed ahead of function blocks. Although this pipeline structure reduces the handshake cycle

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time, the asymmetric completion detectors still consume a lot of power since they have to detect the entire data paths.

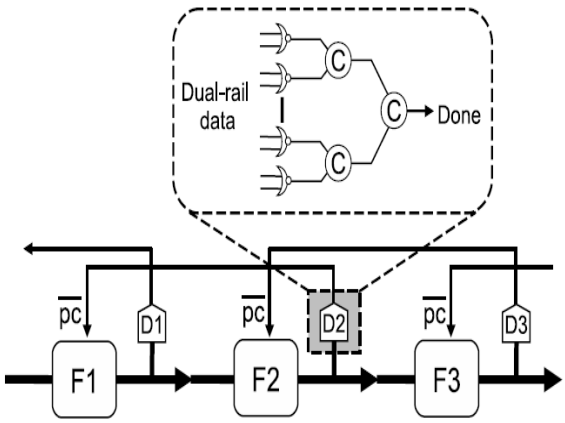

Fig 3.2 Block diagram of PS0

3.3.2 Delay Elements:

Adding delay elements is an intuitive way to construct a stable critical data path. However, this method needs complex timing analysis and would cause huge overhead of delay elements. This paper introduces an efficient solution that uses SLGs to construct the critical dataAlthough such design reduces the power consumption in handshake control logic, the overhead problem in function block logic remains unsolved since dual-rail domino logic still has to be used to compose the domino data path.

3.3.3 Logic Gates:

In VLSI circuits, it is difficult to get a stable critical data path using traditional logic gates due to the gate-delay data

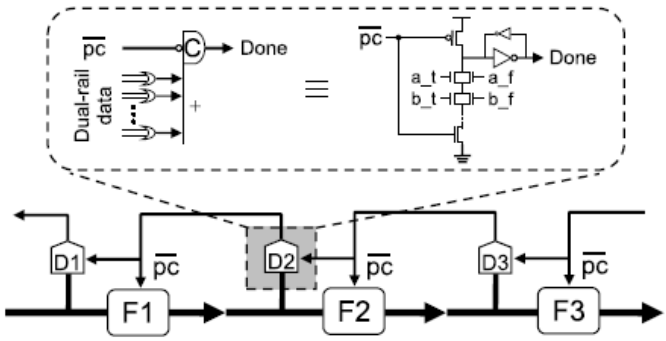

Fig 3.3 Block diagram of LP2/2 based on dual-rail protocol

The block diagram of LP2/2 based on the bundled-data protocol (LP2/2-SR) is shown. LP2/2-SR avoids the detection overhead problem by implementing a single extra bundling signal. The bundling signal serves as a completion signal, which matches the worst case delay in function blocks. Although such design reduces the power consumption in handshake

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control logic, the overhead problem in function block logic remains unsolved since dual-rail domino logic still has to be used to compose the domino data path.

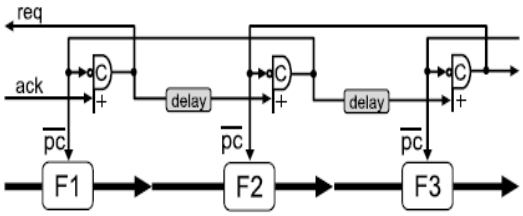

Fig 3.4 Block diagram of LP2/2 SR

dependence problem. The traditional dual-rail domino AND gate is shown below.

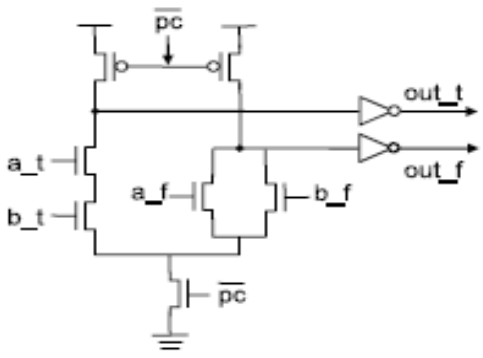

Fig 3.8 Logic diagram of dual rail domino logic and gate

The true side of logic is implemented by out_t = a_t · b_t and the false side by out_ f = a_ f +b_ f .

Data patterns (a_t,a_f,b_t ,b_f)	Pull-down transistor paths						
	Conventional			Synchronizing AND gate			
	(a_t,b_t)	(a_f)	(b_f)	(a_t,b_t)	(a_t,b_t)	(a_t,b_f)	(a_f,b_f)
(0,1,0,1)	OFF	ON	ON	OFF	OFF	OFF	ON
(0,1,1,0)	OFF	ON	OFF	OFF	OFF	ON	OFF
(1,0,0,1)	OFF	OFF	ON	OFF	ON	OFF	OFF
(1,0,1,0)	ON	OFF	OFF	ON	OFF	OFF	OFF

Table 3.2 states of pull-down transistor paths on different data patterns

In traditional dual-rail domino AND gate, there are three transistor paths:

1) [a_t, b_t];

2) [a_ f];

3) [b_ f].

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First of all, these paths have different number of transistors at the sequential position. When they turn ON, respectively, [a_ f] and [b_ f] cause less delays than[a_t, b_t]. Moreover, when the data pattern is (0, 1, 0, 1), [a_ f] and [b_ f] will be both ON, which leads to a much quicker signal transfer. As a result, the gate delay has a large variation depending on different data patterns. To solve the gate-delay data-dependence problem, SLG and SLGL are introduced gates that have no gate-delay data-dependence problem. The synchronizing AND gate and the truth table of dual rail AND logic is shown logic circuits. The principle is that, in the pull-down network, there is exactly one path activated according to one data Pattern and the stack of all possible paths is kept constant at the sequential position. Compared with the traditional design, the false side logic expression is changed to out_ f = a_t ·b_ f + a_ f .

Table shows that there are four transistor paths:

1) [a_t, b_t];

2) [a_t, b_ f];

3) [a_ f, b_t]; and [a_ f, b_ f].

3.4 Structure of APCDP:

3 .4.1 Synchronizing Logic Gates:

Every path has two transistors at the sequential position, and there is only

One path turns ON corresponding to an input data pattern. As a result, the gate delay becomes independent on different data patterns. This kind of gates is named as SLGs because they can synchronize their inputs. The SLGs verify that all data signal transitions have arrived on their inputs before changing their outputs.

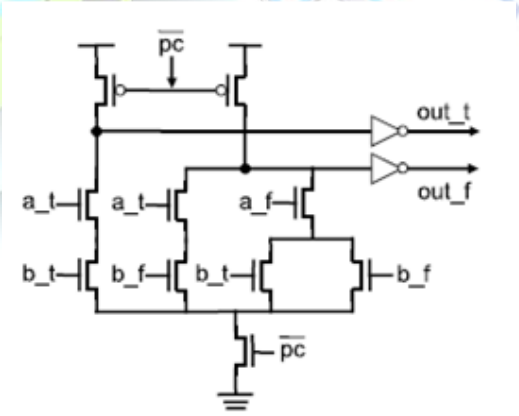

Fig 3.9 Logic diagram of synchronous AND gate

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Table 2.3 Truth table of dual rail AND gate

PC	a_t	a_f	b_t	b_f	out_t	out_f
0	-	-	-	-	0	0
1	0	1	0	1	0	1
1	0	1	1	0	0	1
1	1	0	0	1	0	1
1	1	0	1	0	1	0

The characteristics of SLGs are listed as follows.

1) An SLG has a certain number, inputs' number, of transistors in pull-down transistor paths at the sequential position.

2) An SLG has no gate-delay data-dependence problem. Its gate delay mainly relates to the inputs number.

3) An SLG can synchronize its inputs. The SLG cannot start evaluation until all valid data arrive.

3.4.2 Logic Gates with a Latch Function:

Based on the characteristics of SLGs, SLGLs are extended. The diagram shown below represents a synchronizing AND gate with a latch function and the table of latch states. An SLGL has an enable port *(*en_*t,* en_ *f)*, which controls the opaque and transparent state of the SLGL.

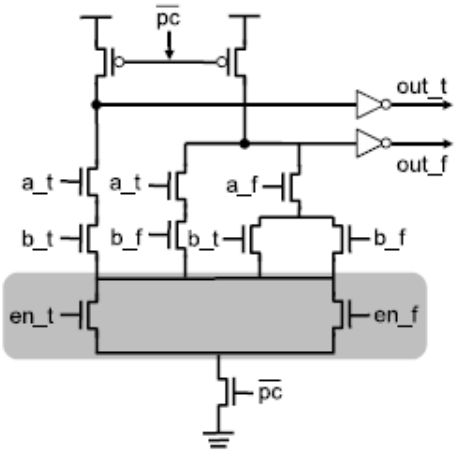

Figure 3.10 logic diagram of synchronous AND gate with latch function

The principle is that SLGLs cannot start evaluation without the presence of the enable signal. Same as the dual-rail AND logic, all traditional dual-rail domino logic can be redesigned to become an SLG or an SLGL.

Table 3.4 Truth table of latch states

PC	en_t	en_f	States
0	-	-	Opaque
1	0	0	Opaque
1	0	1	Transparent
1	1	0	Transparent

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1	1	1	No used

The critical data path in dual-rail asynchronous pipeline can be easily constructed using SLGs and SLGLs.

3.4.3 ECRL:

Power gating is one of the most efficient techniques for leakage reduction. In general, power gating techniques increase the effective resistance of leakage paths by inserting sleep transistors (power gating transistors) between power supply rails and transistor stacks. In the idle mode, the sleep transistors are turned off, turning off the pull-up pull-down networks off from one (or) both power rails, and thus leakage current are inhibited. In the active mode, the sleep transistors are turned on, reconnecting the pull-up pull-down networks to power supply rails.ECRL adopts dual-rail data encoding; that is, each input to an ECRL gate requires both polarities to be represented, and each ECRL gate computes both a logic function and its complement. As shown in the diagram below, an ECRL gate acquires Power from the power node, denoted by *Vp*.

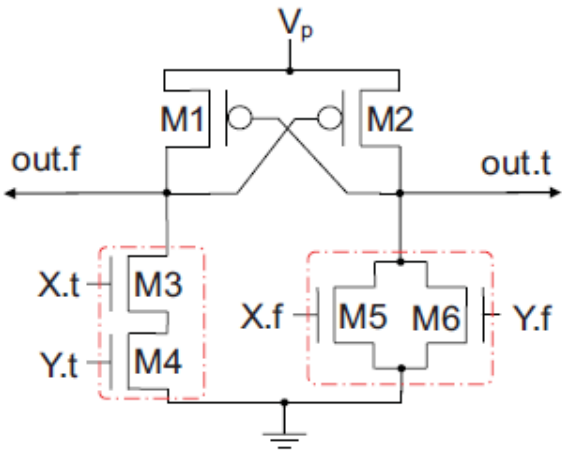

Fig 3.11 Logic diagram of ECRL logic gate

The ECRL gates in the AFPL pipeline acquire their power from the handshake controllers instead from a conventional fixed DC power supply. The operation cycle of an ECRL gate comprises four phases, wait, evaluate, hold and discharge. The current operation phase of an ECRL gate Gi is determined by the voltage of the associate power node Vpi.

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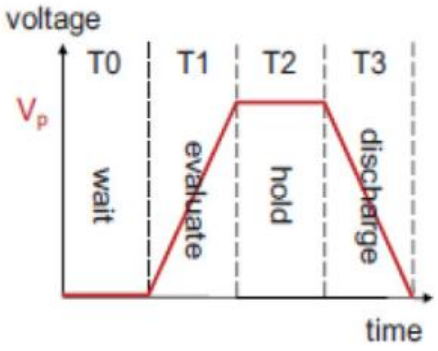

Fig 3.12 Operation phase of ECRL

The voltage waveform of the power node Vpi is shown in the diagram. During the wait phase, the power node Vpi is kept at 0V, and gate Gi cannot draw any current from Vpi. Christo Ananth et al. [3] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S- Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message.

3.4.4 Encoding Conversion:

Since the completion detector detects only the constructed critical data path, the noncritical data paths do not have to transfer encoded handshake signal anymore. The logic overhead in the noncritical data paths canbe reduced using single-rail domino gates instead of dual-rail domino gates. However, single-rail domino gate and dual-rail domino gate use different encoding schemes. It has encoding compatibility problem when a single-rail domino gate connects to a dual-rail domino gate. Encoding converter needs to be designed to solve the problem.

In precharge phase pc = 0, encoding converter outputs a dual-rail data0 (out, out) = (0, 1).In evaluation phase pc = 1, if the input is a single-rail data0 in = 0, the converterkeeps the dual-rail data0. If the input is a single-rail data1 in = 1, the converteroutputs a dual-rail data1 (out, out) = (1, 0). Since single-rail encoding only has twostates that, respectively, represent data0 and data1,

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there is no other state that can be converted to spacer (out, out) = (0, 0).

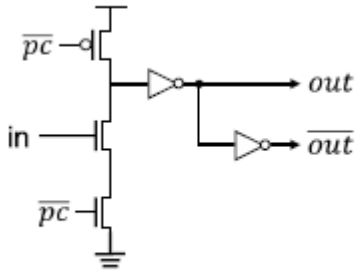

Fig 3.13 logic diagram of encoding converter

The disappearance of spacer violates the four-phase dual-rail protocol, which would cause data transfer error.

Table 3.5 Truth table of encoding converter

$\overline{PC}$	In	Out	$\overline{O}$
0	-	0	1
1	0	0	1
1	1	1	0

The diagram shows two examples that encoding converters are used to bridge the connection between single-rail domino gate and dual-rail domino gate. Focusing on the encoding converter in Stage2, when Stage2 enters the precharge phase, the SLG outputs a spacer, but the converteroutputs a invalid data0. This invalid data0 cannot be absorbed by the SLGL in Stage3 since the spacer impedes its evaluation. However, when Stage2 enters the evaluation phase, it has a risk that the invalid Data0 might be erroneously absorbed if the output of the SLG becomes valid earlier than the output of the converter. Christo Ananth et al. [4] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated

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with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm .By this design, the power dissipation, delay and noise can be reduced.

We only have to focus on improving the conversion from the single-rail data1 in = 1 to the dual-rail data1 (out, out) = (1, 0).

3.4.5 ARCHITECTURE OF APCDP

The architecture represents a constructed critical data path (dual-rail data path), the dotted arrow represents the noncritical data paths (single rail data paths), and the dashed arrow represents the output of single-rail to dual-rail encoding converter. In each pipeline stage, a static NOR gate is used as 1-bit completion detector to generate a total done signal for the entire data paths by detecting the constructed critical data path. Driving buffers deliver each total done signal to the precharge/evaluation control port of the previous stage. Since the completion detector only detects the constructed critical data path, the noncritical data paths do not have to transfer encoded handshake signal anymore. Therefore, single rail domino gates are used in the noncritical data path to save logic overhead. Encoding converter is used to bridge the connection between single-rail domino gate and dual-rail domino gate.

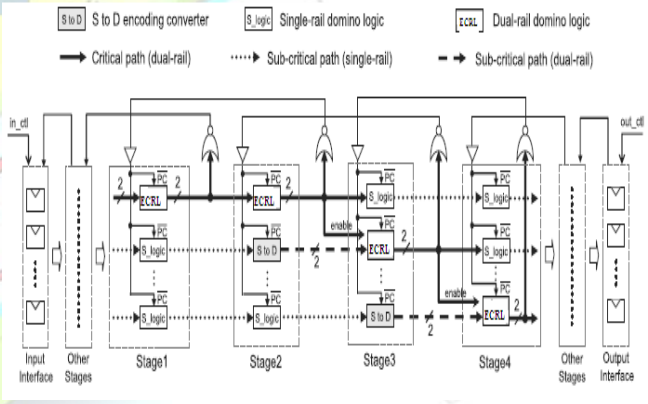

Fig 3.14 structure of APCDP

It is difficult to construct a stable critical data path using traditional logic gates for their gate-delay data-dependence problem. The critical signal transition varies from one data path to others according to different input data patterns.

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Since ECRLs have solved the gate-delay data-dependence problem, a stable critical data path can be easily constructed by the following step

- ✓ Finding a gate (named as Lin gate) that has the largest number of inputs in each pipeline stage;
- ✓ Changing these Lin gates to ECRLs;
- ✓ Linking ECRLs together to form a stable critical data path.

The basic idea of finding the critical signal transition is that embedding an ECRL in each pipeline stage and making the ECRL to be the last gate to start and finish evaluation. First of all, the embedded ECRL has the largest gate delay in a pipeline stage. The reasons are as follows.

- ✓ The ECRL has the largest stack in the pull-down network compared with other gates.
- ✓ The ECRL has only one pull-down transistor path activated for each input data pattern.

Then, if all gates evaluate at the same time or the ECRL is the last gate to start evaluation in the pipeline stage, the critical signal transition would present on the output of the ECRL. In practice, making all gates evaluate at the same time is difficult, especially without the help of intermediate latches or registers. Therefore, we make the ECRL become the last gate to start evaluation by linking each pipeline stage's ECRL together. In the first pipeline stage, the critical signal transition is on the output of the ECRL because all gates evaluate at the same time for the input control of latches or registers. After linking each pipeline stage's ECRL together, the ECRL in the following pipeline stage would be the last gate to start evaluation since it always waits for the critical signal transition from the previous ECRL. As a result, the linked ECRL data path becomes a stable critical data path. Linking each pipeline stage's ECRL together is partially done in the process of selecting Lin gate in each pipeline stage. When searching Lin gate, there might be more than one option. It is

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best to select the Lin gate that is originally linked to the Lin gate in the following pipeline stage. After changing these Lin gates to ECRLs, ECRLs are naturally linked.

SOFTWARE/TOOLS USED

4.1 TANNER EDA:

Tanner EDA, a leading provider of integrated circuit design, verification and simulation software products, is looking for an outstanding Senior Scientist/Developer to work on our HiPer Verify product line. You will be member of a team of experts creating innovative algorithms for design rule checking (DRC), layout extraction, and layout versus schematic (LVS) products used in integrated circuit chip verification.

The candidate should have a strong background developing graph and geometric algorithms in large scale applications. Experience developing EDA algorithms in particular is highly desirable. Our environment is team-oriented, very technical and fast paced. You will have the opportunity to make immediate significant contributions to our products.

This position requires expert level C/C++ programming ability, STL experience, cross platform development ability and proficiency in large scale algorithm computing. Excellent communication and organization skills and the ability to effectively learn complex software are also required. If you find excitement in creating products that rely on the development of advanced algorithms from multiple domains (electrical, mathematical, etc.) and are delivered as finely tuned, industrial strength software solutions, you should contact us now.

4.2 FEATURES OF TANNER EDA:

The Tanner Tools suite of products offers today's designers:

- **Low total cost of ownership**. Tanner has created a software platform that is cost-effective and easy to use,

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while still being powerful enough to handle complex designs. Through the years Tanner EDA has remained true to its mission by delivering tools on the Windows infrastructure that can easily augment a company's existing design tool flow.

- **Technological innovation**. While Tanner EDA's design tools are significantly less expensive than those of the competition, they do not sacrifice performance. Tanner EDA tools are suitable for start-ups, mid-size, and million-dollar top-tier players working on a range of innovative and cutting-edge designs. Tanner EDA's continued innovation makes its tools cost-effective solutions that grow with a company as its performance needs change.

- **Flexible PC-based solutions**. Tanner EDA tools are fully optimized for the Windows PC platform, enabling users to leverage their existing infrastructure and work at the office or at home. The flexibility of this platform, along with its familiar, intuitive interface gives designers customizable solutions that are fully portable. This is a good choice for designers who need high-performance EDA tools at a reasonable price.

- **Calibre/Dracula foundry compatible**. Tanner EDA solutions are the only EDA tools on the market that natively support the Mentor Graphics Calibre and Cadence Dracula formats. This support enables them to use foundry rule decks without the need to translate the rules to another format and possibly lose data in the process. When the foundry updates its rule decks, Tanner EDA solutions automatically incorporate the changes, ensuring that the designer remains in line with the foundry.

- **Production proven tools:** During its 20-year history, Tanner EDA has established a reputation as a leading technology innovator and supplier of cost-effective, flexible, and reliable production tools. Today the company

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boasts 4,000 customers and over 25,000 active licenses in 64 countries worldwide.

RESULTS AND DISCUSSION

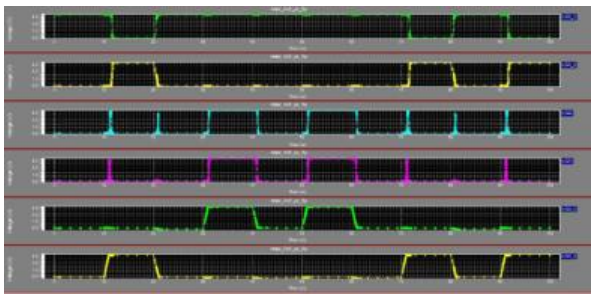
The performances of throughput are evaluated without considering design margins, which are ideal results. The results show that APCDP has high throughput, the smallest transistor count, and the lowest forward latency in all designs.

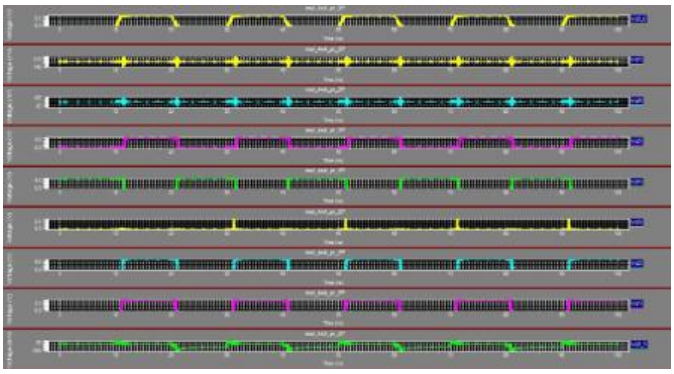
5.1 2x2 Array Multiplier:

Average power consumed using SGL : 1.899264e-002 watts

Average power consumed using ECRL gate: 1.681685e-002 watts

5.2 4x4 Array Multiplier:

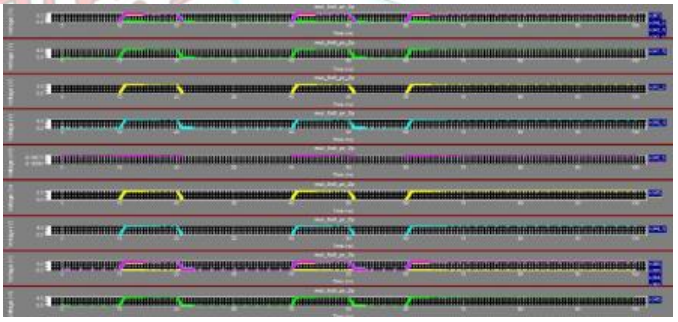




Average power consumed using SLG : 2.972562e-002 watts

Average power consumed using ECRL gate: 2.578980e-002 watts

5.3 8x8 Array Multiplier:



Average power consumed using SLG :1.280206e-001 watts

Average power consumed using ECRL gate: 1.079368e-001 watts

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6.1 CONCLUSION

In this project work, asynchronous domino logic pipeline was designed. The pipeline is realized based on a constructed critical data path In the APCDP circuit, the logic blocks become active only when performing useful computations, and the idle logic blocks were not powered and have negligible leakage power dissipation. With fine-grain power gating, the APCDP approach has more opportunities to reduce leakage at run-time than other coarse-grain power gating techniques.

A simulation is done in TANNER EDA to accomplish an 8 × 8 array style multiplier is used for evaluating the proposed pipeline method. The effectiveness of the system is analysed through the graph achieved from the simulation. The results show that by using ECRL negligible power dissipation was achieved.

6.2 FUTURE WORK

As a future work, Null conventional logic is going to include in the pipeline design for the purpose of increasing the throughput.

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