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Design Of Pulsed Latch Based Shift Register Using Multiplexer With Reduced Power And Area

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Abstract: Power consumption and Area reduction is a major role in sequential circuit design .A novel approach to design a pulsed latch based shift register with reduced area and power is proposed.. In this the, conventional data Flip flops are replaced with pulsed latches to reduce area occupation .This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. In the existing system, shift register uses single pulsed clock signal for data transition, which consumes more power. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using Multiplexer and additional temporary storage latches. To minimize power consumption multiple non overlap delayed pulsed clock signal scheme is proposed for data synchronization in a multi bit shift register. The proposed system will be carried out using Tanner T- Spice.

Index Terms-flip-flop, pulsed clock, pulsed latch, shift register.

I. INTRODUCTION

Low power has emerged as a principal theme in today's world of electronics industries. Powerdissipation has become an important consideration as performance and area for VLSI Chip design.For power management leakage current also plays an important role in low power VLSI designs. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs .As the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip usesa 4K-bshiregister. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption.

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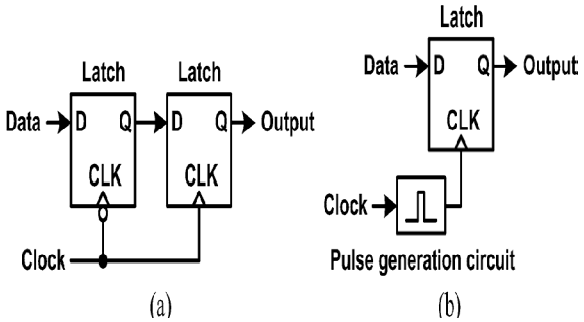


Fig. 1. (a) Master-slave flip-flop. (b) Pulsed latch.

Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop.But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.This paper proposes a pulsed latch based shift register with reduced area and power. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. The rest of the paper describes the proposed shift register architecture and the result measures.

II. CONVENTIONAL SYSTEM

A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.

The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2. The shift register in Fig. 2(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 2(b) shows the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width (TPULSE). One solution for the timing problem is to add delay circuits between latches,However, the delay circuits cause large area and power occupation.

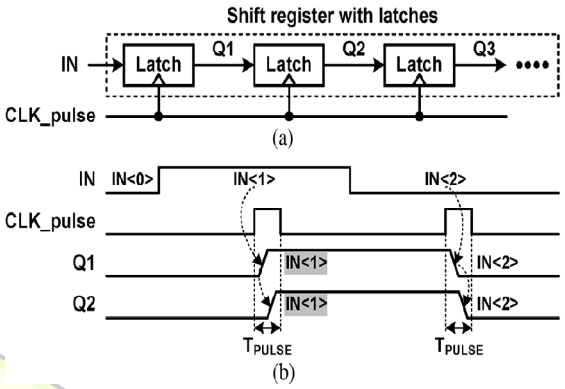
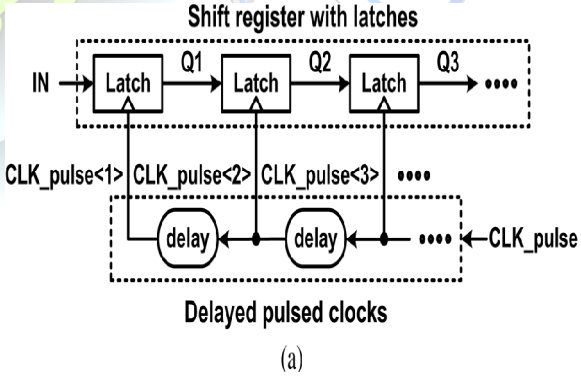


Fig. 2. Shift register with latches and a pulsed clock signal. (a) Schematic. (b) Waveforms.

Other solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 3(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.



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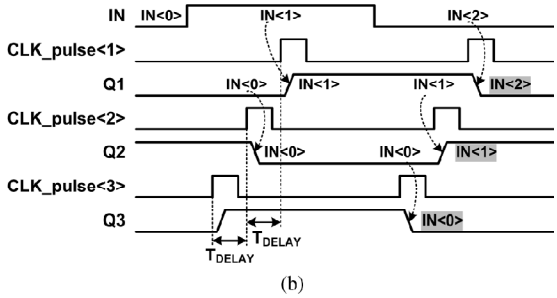

Fig. 3. Shift register with latches and delayed pulsed clock signals. (a) Schematic. (b) Waveforms.

III. LITERATURE SURVEY

Wenxu Zhao has proposed a new mechanism that performs functionality of flip-flop based on generating explicit transparency window where the transition is allowed. HLFF(Hybrid Latch Flip flop)provides high performance and should be able to toggle at 5GHz with the difference between Q and Qbar outputs at full transition. In this paper, several analysis approaches and iterating, power consumption is calculated while running at 5GHz.All transistors are equally sized to match timing constraints and finally power consumption to be minimized.[1]

Vinoth,R. et al. have designed Low Power Dual Dynamic Node Hybrid Flip-Flop. They designed a Low power high performance dual dynamic node hybrid flip-flop and embedded logic module with SVL Circuit. This design eliminates large capacitance in the precharge node that separately drives the output pull-up and pull-down transistors. Their design carried out comparison of the dual dynamic node hybrid flip-flop (DDFF), dual dynamic node hybrid flip flop with logic embedding capability (DDFF-ELM) with dual dynamic node hybrid flip flop self-controllable-voltage-level (DDFF-SVL) logics and they obtained the best power -delay-performance [2].

Vladimir Stojanovic and Vojin G. Oklobdzija give a comparative study of master slave flip flop and latches for high performance and low power systems. They identified three main sources of power dissipation in latch: internal power dissipation of the latch, local clock power dissipation, local data power dissipation and also measured the power dissipated by the circuit driving the inputs of the latch to determine the local clock and data power dissipation[3].

Xiangyu Zhang proposed a paper of reduced power shift register with clock gating. He analysed that by clock gating technique, clock to an idle portion is disabled, thus avoiding power dissipation due to unnecessary charging and discharging of the unused circuit.

In this design, he used a 8-bit shift-left register with positive-edge clock, serial In, and serial Out. He made a comparison of power dissipation without clock gating and power dissipation with clock gating and concluded that clock gating technique significantly reduces dynamic power of shift register[4].

V.Kavipriya and K.Sedhuramalingam proposed a paper on Design and Analysis of Low Power Pulse Triggered Flip-Flop .They give a comparative analysis of a classic explicit pulse triggered flip flop (ep-DCO), modified hybrid latch flipflop (MHLFF) with proposed P-FF design using signal feed through technique. The P-FF design also employs a static latch structure and a conditional discharge scheme to avoid unwanted switching inside the transistors. By using simple pass transistors they achieved a better result in power consumption[5].

Madge Deepali Harish et al. have designed a paper on pulsed triggered flip flop for low power applications. In this design, they introduces a series pass transistor which helps in reducing discharging path and made improvement in delay. They compared power and delay of many flip flops and proved that pulse triggered flip flop operates in low power[6].

Chi-Ken Tsai et al. have proposed a pulse edge triggered latches design in low power. The clock storage elements using the low power technique are realized in this paper. A Low swing conditional capture edge-trigged flip-flop(LSCCFF) and conditional precharged double edge-triggered flip-flop (CPDFF) are the two used to reduce clock power. The comparison has been performed on the basis of number of transistors, staticpower, dynamic power and average clock used.

Based on this comparison, the proposed CPDFF could save 42%~79% of the static power and 8%~52% of the dynamic power[7].

Survey based report gives the comparison output as shown in table 1.

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TABLE 1 Comparison Result

TYPE	NO. OF. TRANSISTORS	DELAY	POWER
Transmission Gate Flip flop(TGFF)	18	107.1	11.0
Hybrid Latch Flip Flop(HLFF)	20	73.7	27.6
Sense Amplifier based FF(SAFF)	18	190.2	21.3
Dual rail static edge triggered latch(DCCER)	26	253.3	31.5
Low swing conditional capture edge-trigged flip-flop(LSCCFF)	25	138.1	7.1
Single-ended Conditional Capturing Energy Recovery (SCCER)	17	64.84	17.25
Modified Hybrid Latch based Flip flop(MHLFF)	19	60.86	16.297
Implicit-pulsed data-close-to-output (ip-DCO)	23	66.96	19.72

Byung-Do Yanghave proposed a paper on shift register using pulsed latches.In this, Shift register is divided into **M** sub shifter registers as shown in Fig. 4(a) to reduce the number of delayed pulsed clock signals. Each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate. A 4-bitsub shifter register consists of five latches and it performs shiftoperations with five non-overlap delayed pulsed clock signals(CLK_pulse□1:4□□and CLK_pulse□T□). Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator.In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Christo Ananth et al. [10] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm .By this design, the power dissipation, delay and noise can be reduced.

The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches.The sequence of the pulsed clock signals is in the opposite order of the five latches.The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register.Fig. 4(b) shows the operation waveforms in the proposed shift register.

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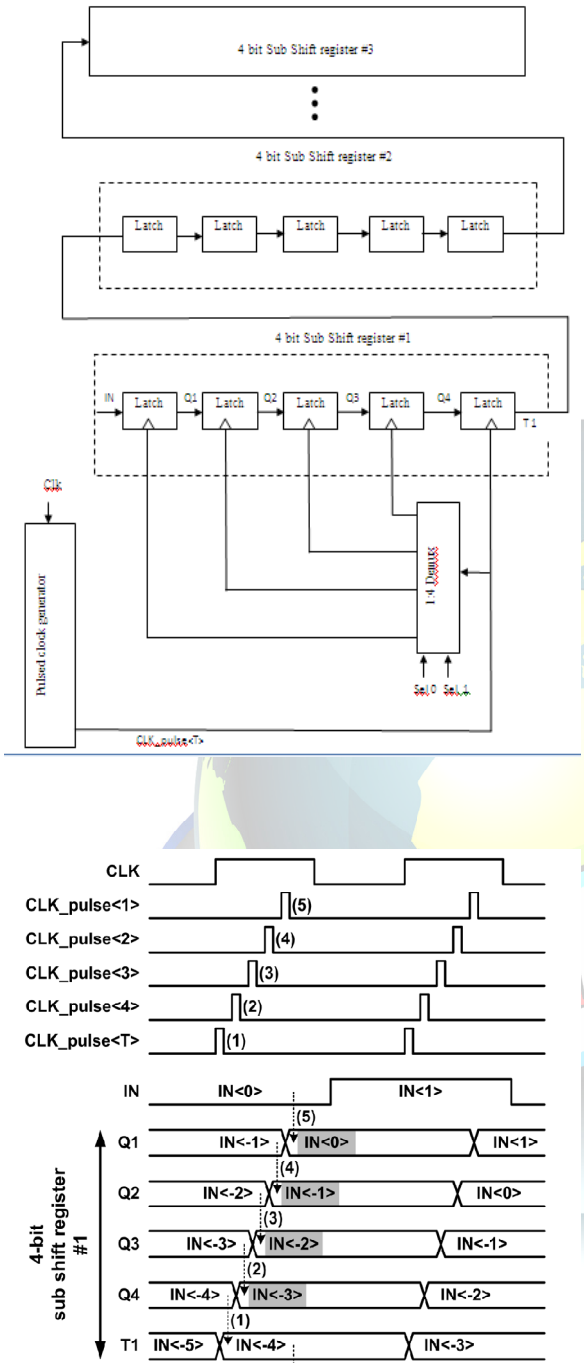

Fig. 4. Pulsed latch based shift register (a)Schematic. (b) Waveforms.

The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register **(K)**.**K** is selected by considering the area, power consumption, speed.

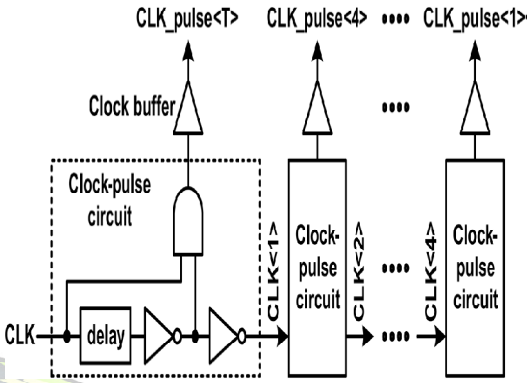

Fig. 5. Delayed pulsed clock generator.

In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. All pulsed clock signals have almost the same pulse skews when they arrive at the same sub shift register. Therefore, in the same sub shift register, the pulse skew differences between the pulsed clock signals are very small. The clock pulse intervals larger than the pulse skew differences cancel out the effects of the pulse skew differences. Also, the pulse skew differences between the different sub shift registers do not cause any timing problem, because two latches connecting two sub shift registers use the first and last pulsed clocks (CLK_pulse⟨T⟩ and CLK_pulse⟨1⟩) which have a long clock pulse interval.

IV. SIMULATION RESULTS

The proposed pulsedlatch based shift register is designed againstexisting flip flop design and this design is designed in Tanner90n meter technology and simulated both in pre-layout. Aftersimulation delay, number of transistor and power is lesscompare to existing flip flop this is shown in table2 and Fig 6 show the circuit and Fig 7 shows waveform of pulsed latch output.

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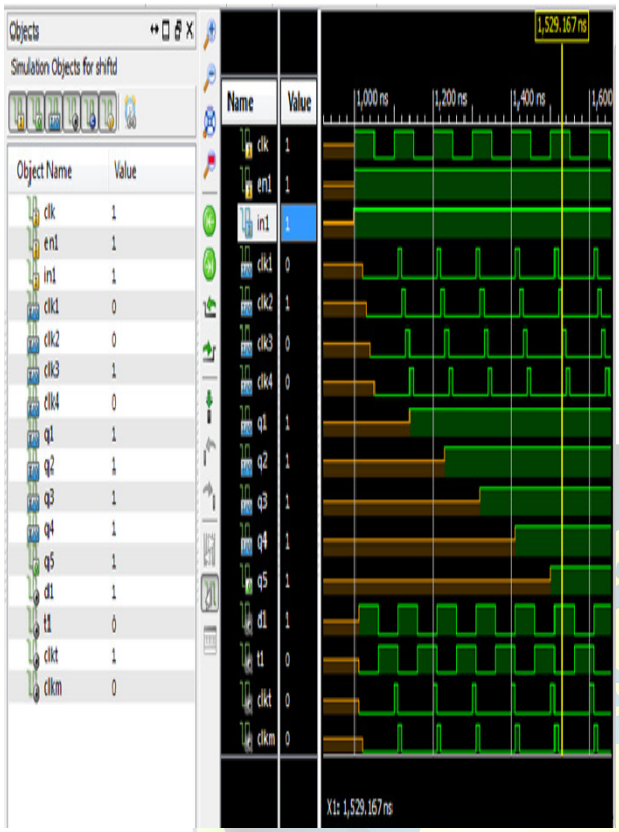

Fig. 7. . Simulation Waveform

TABLE 2 Comparison Result of Proposed shift register

FLIP FLOP		PULSED LATCHES
Total number of transistors	16	7
Number of transistors connected to clock	8	1
Clock	8	1
Area	9600	5530
Power	0.991	0.441
Clock frequency	2.8GHZ	483MHZ

V. CONCLUSION

In this paper several architectures of pulsed latch based shift register design is discussed. In many architectures, the area and power consumption are reduced by implementing pulsed latches for shift register design instead of flip flop. Power and area occupation of pulsed latch based shift register is comparatively less with rest architectures is discussed in table 1 and 2. The pulsed latch based shift register design uses less number of pulsed clock signals by merging the latches to multiple sub shift register and also using additional temporary storage latches. But still there is an unwanted switching's in the static differential sense amp shared pulse latch may lead to excess dynamic power dissipation and also area occupation. Modify the transistor level design latch will reduce area and power consumption in shift register design further.

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