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DESIGN AND ANAYSIS OF SHIFT REGISTER USING DUAL DYNAMIC FLIP-FLOP

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Abstract: - **Low Power analysis is a major concern in today's VLSI world. Much, continuance system like flip-flop (FF) consumes giant portion of total chip power. Thus during this paper we tend to discuss concerning style the planning the look} of the clock system exploitation novel Flip-Flop design. During this paper, a unique low-power current mode pulsed flip-flop (CMPFF) style is bestowed. Current mode pulsed FF (P-FF) has been thought-about as a well-liked different to the traditional master –slave primarily based F. A low-power flip-flop (FF) style that includes a particular kind current mode with the clock distribution network for low leakage was present. The planned style with success solves the long discharging path drawback in standard express kind Current mode Pulsed FF (CMPFF) styles and achieves higher speed and power performance within the applications of high speed. These circuits are simulated exploitation Tanner Tools with 50nm technology.**

Keywords: Current mode Pulsed flip-flop (CMPFF), true single phase clock, clocking distribution network.

I. INTRODUCTION

Flip-flops (FFs) square measure the essential storage parts and that they square measure used extensively in styles of all digital system. Today's technology adopts the pipelined design in each and every system to enhance its [7] performance. Clock system consists of a clock generator, clock distribution network and no of Flip-Flops. it\'s conjointly calculable that the ability consumption of the clock system is as high as half-hour to hr of [4] the overall system power. So as to cut back the CDN (Clock distribution network) load and to cut back the clock power we tend to introduce a current mode [2] pulsed flip flops. Current mode pulsed FF (CMPFF) has been thought-about a serious various to the standard master–slave-based FF within the applications of high-speed operations [2]–[5]. Beside the speed advantage, its circuit simplicity is additionally accustomed lowering the ability.

Consumption of the clock tree system rather than ancient Master-Slave Flip-Flop a [3] CMPFF consists of a generator for generating strobe light signals and a latch for information storage. Since triggering pulses generated [9] on the transition edges of the clock signal square measure terribly slim in pulse dimension, the latch acts like Associate in edge-triggered FF. The circuit complexness of a CMPFF is simplified since just one latch, as critical 2 utilized in standard master–slave configuration, is needed. CMPFFs

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conjointly enable time borrowing across clock cycle boundaries and have a zero or maybe negative [11] setup time. CMPFFs square measure so less sensitive to clock interference. Despite these benefits, pulse generation electronic equipment needs delicate pulse dimension management within the face of method [10] variation and also the configuration of pulse clock distribution network .Depending on the tactic of pulse generation, CMPFF styles are often classified as implicit or express [6]. In Associate in nursing implicit-type CMPFF, the heart [5] beat generator may be a constitutional logic of the latch style, and no express pulse signals square measure generated. In Associate in nursing explicit-type CMPFF, the styles [6] of generator and latch square measure separate. Implicit pulse generation is commonly thought-about to be a lot of power economical than express pulse generation [2].

This can be as a result of the previous simply [4] controls the discharging path whereas the latter has to physically generate a pulse train [6]. Implicit-type styles have elongated discharging path in latch style that ends up in inferior temporal arrangement characteristics. Things deteriorate any once [3] low-power techniques like conditional capture, conditional pre-charge, conditional discharge, or conditional information mapping square measure applied. As a consequence, the transistors of pulse generation logic [9] square measure typically enlarged to assure that the generated pulses square measure sufficiently wide to trigger the information capturing of the latch [8]. Explicit-type P-FF styles face the same pulse dimension management issue, however the matter is any sophisticated within [4] the presence of an oversized electrical phenomenon load, e.g., once one generator is shared among many latches [1].

During this paper, we are going to gift a completely unique low-power explicit-type P-FF style [6] that includes a conditional pulse-enhancement theme. 3 extra transistors [7] square measure utilized to support this feature. In spite of a small increase in total semiconductor count, transistors of the heart [5] beat generation logic get pleasure from vital size reductions and also the overall [2] layout space is even slightly reduced. This provides rise to competitive power and power–delay–product performances against alternative P-FF styles [9].

II. CURRENT MODE PULSED FLIP-FLOP

Current mode pulsed Flip-Flop consists of Current comparator, voltage generator and a Register storage element.

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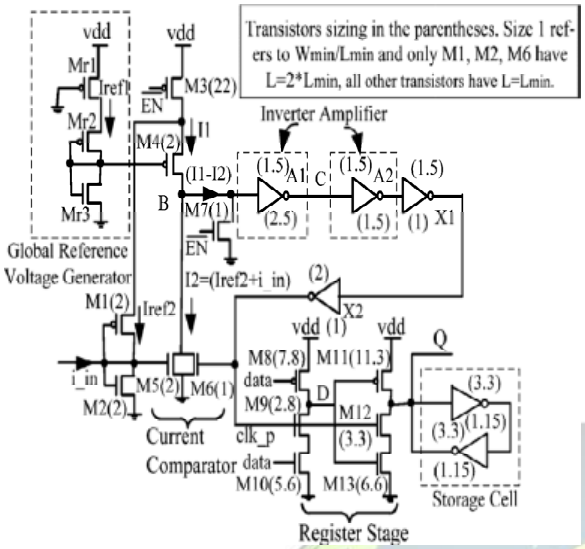

Fig 1: Circuit Diagram of CMPFF

This current mode pulsed signal has been get from the clock distribution network for the analysis of the internal structure. The transmitter and the receiver module have to be declared as the communication port for the reliable communication between all the channels. This flip-flop consists of the voltage generator block with the input generator for the reference input. This will be considered as the CMOS inverter with the current level variations in the circuits. Then this output will be get into the current comparator for the details as per the reference input. The current comparator can be comparing the pulsed signal from the enable input such as clock and the data.

There are unit 3 major variations that result in a novel TSPC structure and build the planned style distinct from the previous one. Christo Ananth et al. [12] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S- Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message.Stage one is to blame for capturing the LOW-to-HIGH transition.

If the input is HIGH within the sampling window, the interior node is discharged, assumptive that were at first (LOW, HIGH) for the discharge path to be enabled. As a result, the output node is charged to HIGH through PMOS of D input within the second stage. Stage a pair of captures the HIGH-to-LOW input transition. If the input was LOW throughout the sampling amount, then the primary stage is disabled, and node retains its pre-charge state. Whereas, node are HIGH, and also the discharge path within the second stage are enabled within the sampling amount, permitting the output node to discharge and to properly capture the input file.

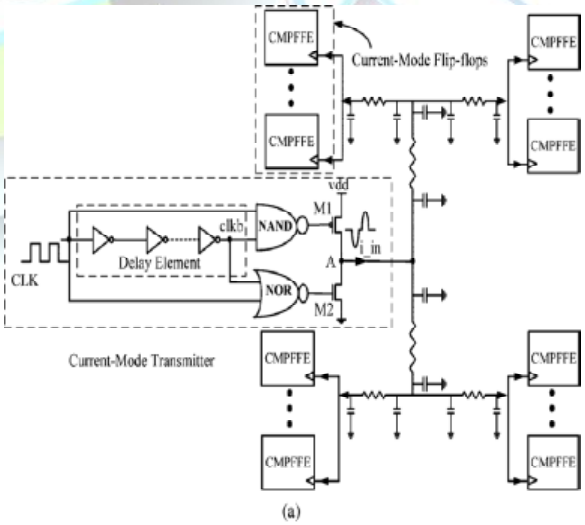

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Fig 2: The proposed current mode pulsed flip-flop with its implementation

The CMPFF has been implemented into the system level for the current mode transmitter with the external level of flip-flop for the desired data communication. The storage element with the required data's can be added into the circuits with the relevant information for this implementation. The several units from this structure have been recovered as the custom signal and into the related structures.

First, a weak pull-up p-MOS semiconductor unit with gate connected to the bottom is employed within the 1st stage of the Current mode transmitter. This provides rise to a pseudo-n-MOS logic vogue style, and also the charge keeper circuit for the interior node with resistance will be saved. Additionally to the circuit simplicity, this approach additionally reduces the load capacitance of node [20], [21]. Second, a pass semiconductor unit controlled by the heart beat clock is enclosed in order that input file will drive node letter of the latch directly. The pull down network of output node was cut back that the we have a tendency to reduce the discharge path.

III. MODIFICATION:

Here we are modify the circuit with the dual dynamic flip-flop and dual dynamic flip-flop with pass transistor logic. The pass transistor logic could be used to reduce the transisotr count from the circuits and it can be lead to a low power and less delay paramter as it sense. The sectional view from the all above proposed flip-flop the perfromance get improved from this modified circuit.

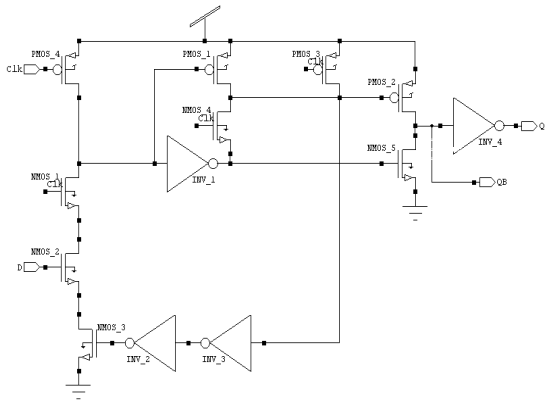

Fig 3: Dual dynamic flip-flop

The Dual Dynamic Flip-Flop (DDFF) is used to decrease circuit complexity, increasing operating speed and lower power dissipation. The glitch problems resulting from charge sharing could be reduced. An unconditional shutoff mechanism in DDFF overcomes the drawback all FF'S. The reason for this in clocking is the charge sharing, which becomes uncontrollable as the number of n-MOS transistors in the stack increases. This node between the structures can be use the environmental modules with the reliable communication. This flip-flop securely reduces the power leakage present in the circuit for the operation of the whole data communication between the channels.

IV. SHIFT REGISTER WITH DDFF:

The shift register implementation has been a sequential logic and it can be used for the converter applications. The serial and the parallel data's can be converted over the communication between the channels which

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will be transferred for the hardware through software.

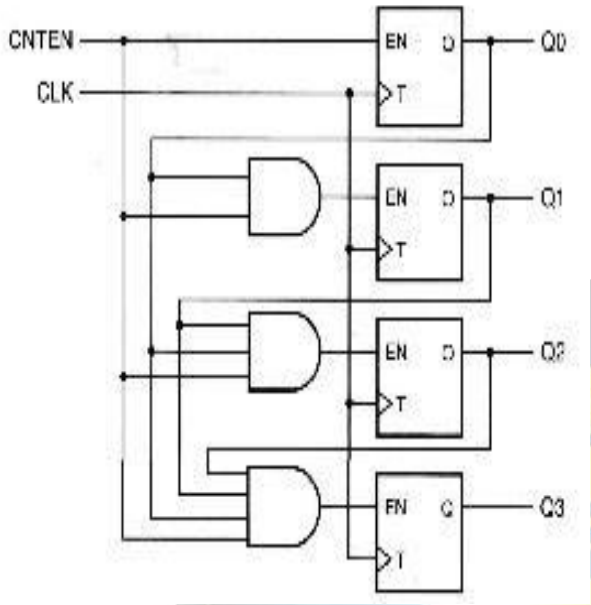

Fig 4: Circuit diagram of the shift register

There are the 4 types of the shift register such as serial in/serial out, serial in/parallel out, parallel in/parallel out, and parallel in/serial out. These 4 types can also to be designed and verified with the CMPFF and the DDFF. Then finally we are going to declare as the one have been considered as the less power consumption and the delay. This solution is to be transferred as per the detailed information for serial wise and the parallel wise for the required transformation through the signals.

V. SIMULATION RESULTS

Tanner Software (Pre format simulation) is utilized for recreation. All circuits have been mimicked in 50nm CMOS engineering with low VDD. The postponement of adjusted current mode pulsed flip-flop is essentially lessened in low voltage supplies. By diminishing the supply voltage, structures are begun to carry on in an unexpected way.

The CMPFF can work speedier and can be utilized in low supply voltages, while devouring almost the same power as the customary (single tail) comparator. The case is far and away superior for the adjusted flip-flop when contrasted with the customary element based on the shift register.

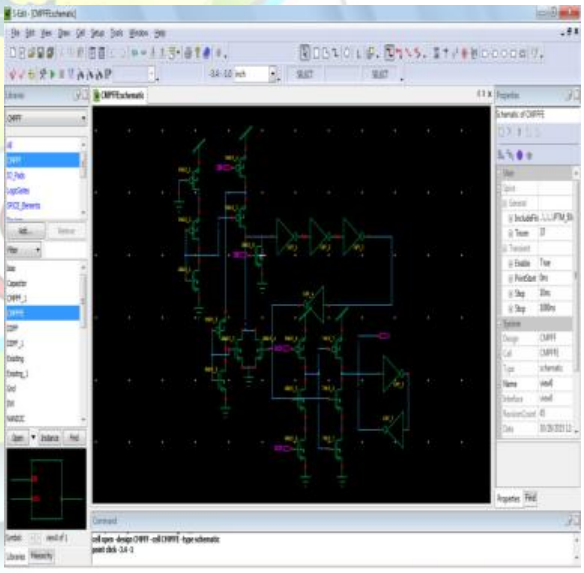

Fig 5: Schematic circuit for CMPFF

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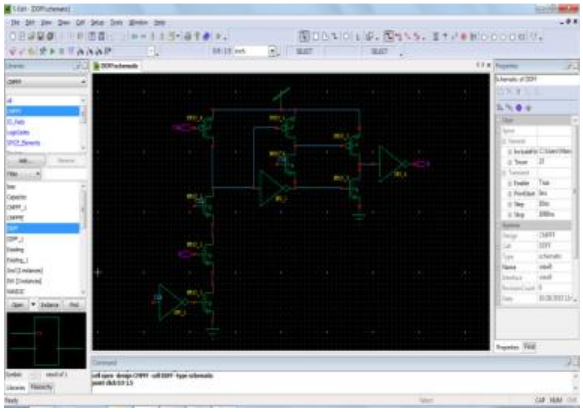

Fig 6: Schematic circuit for DDFF

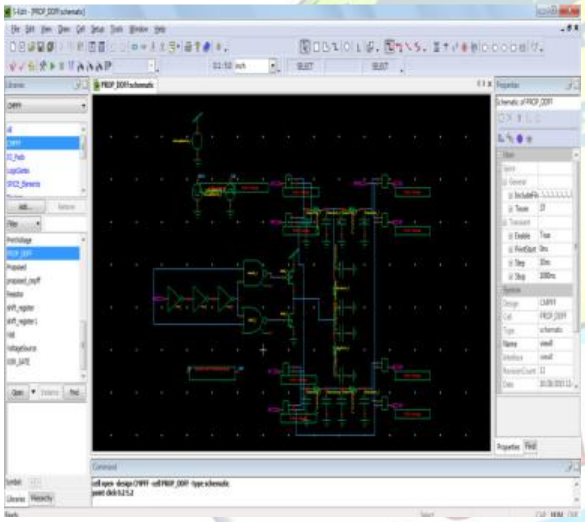

Fig 7: Schematic circuit for proposed implementation transmitter

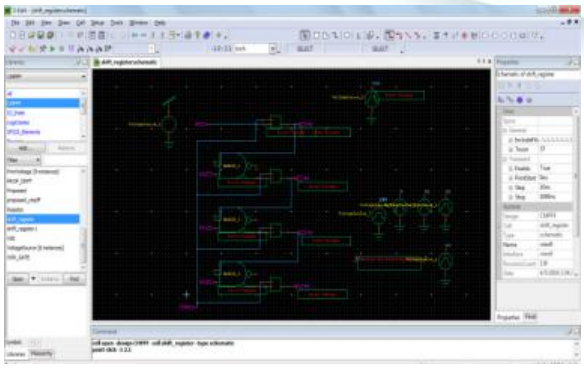

Fig 8: Schematic circuit for the shift registers

Circuit	Power in watts	Delay in sec	Using Nanometer
Proposed_ CMPFF	2.24885e-001	4.7500 e-008	50nm
Proposed_ DDFF	1.119559e-001	4.4958 e-008	50nm
SR_CMPFF	2.375164e-002	4.9700 e-008	50nm
SR_DDFF	1.696286e-002	4.4700 e-008	50nm
Existing	2.720612e-001	5.2500 e-008	50nm
Existing_1	4.427439e-001	5.2500 e-008	50nm

VI. CONCLUSION

In this transient, we tend to a CMPFF style by using a changed current mode transmitter structure incorporating a mixed style vogue consisting of a pass semiconductor unit and pseudo-n-MOS logic and it carries with it generator style. The most plans was to produce an indication feed through from input supply to the interior node of the latch, which might facilitate further driving to shorten the transition time and enhance each power and speed performance. They was created the prevailing flip flop will be designed exploitation less no of semiconductor unit count additionally as power dissipation. Then the proposed CMPFF and the DDFF with the shift register implementation for less power consumption.

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