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LOW POWER MULTIPLIER IMPLEMENTATION WITH FULLADDER

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Abstract: – Low power is major implementation process which could be considered for all the applications. The adders and the multipliers based circuits for its implementations. Adder can be implemented with the ALU's and the floating adder unit. The processor and the controller level implementations. In this paper we are going to design the 3 modules based full adder structure with the SUM and the CARRY module. The input generator module has been implemented from the 1st unit module such as XNOR module output. This will be given into the SUM unit. Then this process could be further given into the carry module. This process having the structure of three modules which will be further implemented with the full adder. These modules are generally with less transistor count when compared with the existing system full adder. The structure can be varied in terms with the full adder modules such as ripple carry adder, carry look ahead adder. The multiplier also has been implemented with this full adder. This circuit has been designed and verified by using TANNER EDA tools.

Keywords: - Ripple carry adder, Multiplier, Low power Full adder, XOR-XNOR.

I. INTRODUCTION

With technological advancements and also the mobile applications expansion, power consumption [4] has become a primary focus of attention in VLSI digital style. Therefore Digital sub-threshold circuit style is one [8] amongst the most focus areas for low power [11] to ultra-low power applications. The provision voltage that's applied to the circuits [3] operational within the sub-threshold region is extremely close to our but the brink [2] voltages of the transistors, so it permits a major reduction of each dynamic and static power [12].

Low-power style of VLSI [7] circuits has been identified as a crucial technological would like in recent [9] years thanks to high demand for transportable client electronics product. With the [10] explosive growth in laptops, transportable personal communication [4] systems and the evolution of the shrinking [5] technology, the attempt in low-power micro electronics has been intense [8] and low-power VLSI systems have emerged high in demand. Adder is one of the foremost necessary parts of a [7] CPU (central process unit), Arithmetic logic unit (ALU), floating-point unit [4] and address generation unit like cache or operation unit.

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One of the foremost common logic family used for [8] sub-threshold operations presently is that the Complementary Metal compound Semiconductor [12] (CMOS) logic family. Moderate low Voltage (ULV) operation originally introduced in 1972 was originally used [10] for low turnout applications like articulation plane watches, sensors [9] and biomedical devices. It provides low to moderate performance and maintains low- power [3] dissipation.

The application of [4] aggressive circuit style techniques that only [8] target enhancing circuit speed while not consider power is no longer a suitable approach in most high complexness digital systems. The facility consumed [5] in high performance integrated circuits has enhanced to levels that impose a limiting issue on the [4] system performance and practicality. A good methodology for reducing [8] the facility consumption is to lower the provision voltage [2].

In this paper, we have a tendency to report the look and [11] performance comparison of 2 full-adder cells enforced with [12] another internal logic structure, supported the multiplexing of the mathematician functions XOR/XNOR [7] and to get balanced delays in total and CARRY [5] outputs, severally, and pass-transistor powerless/groundless logic styles, so as to scale back power consumption. Christo Ananth et al. [1] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm.

EXISTING SYSTEM

The conventional full adder with large number of transistor size could be used for improving the area, delay and the power. This could be a heavy related structure to design the full adders with the generation of all the transistor sizes. The conventional circuit could not be used for the high level applications and the implementation. The unit cannot be succeeding for the device in the basis of created net list generation. But another important conclusion has pointed out over there: the major problem on regards of propagation delay for a full adder built upon the logic structure. So the static power dissipation is affected.

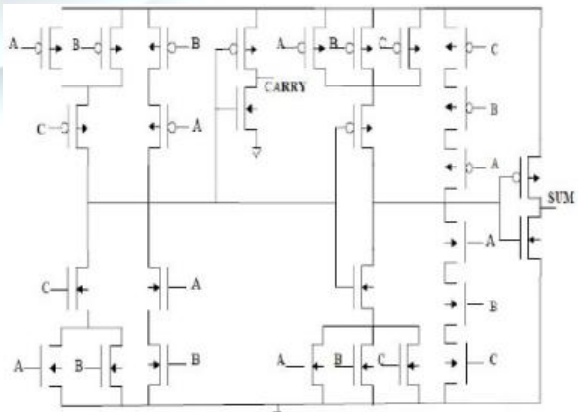

Fig 1: Conventional full adder structure

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II. PROPOSED SYSTEM

The proposed system could be implemented by using the two logics such as XOR and the XNOR. The proposed modules based XOR and XNOR operation could be possible to implement the full adder with les number of transistor circuit. The NMOS and PMOS chains are completely symmetrical. A maximum of two series transistors can be observed in the carry generation circuitry. Only the transistors in the carry stage have to be optimized for optimal speed. All transistors in the sum stage can be minimal size.

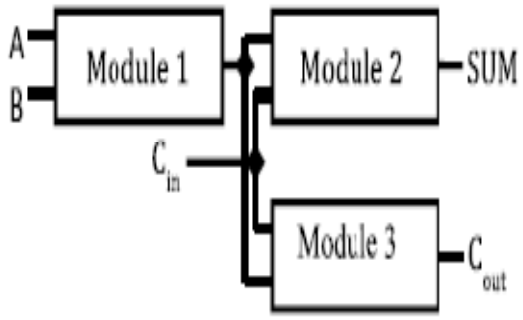

Fig 2: Proposed full adder module

The common 3 Modules based Full adder has been proposed here. This could be used to slightly reduce the area and the main power dissipation. The logic level structure could be recognized in the various applications for the related units based on the architecture view. This could be from the gate level into the adder level. Based on this structure we are implementing the proposed full adder with 8T. This is also studied for the implementation of the XOR logic with the CMOS based. The level of 2 XOR and the coupling of PMOS and the NMOS combined to form the full adder. Another drawback is current back through junction transistor MN1 happens once A=1 and B=0. The output of the pass transistor junction is fed back through transistor MN1 that it operates within the active region. This will overcome by reducing the W/L quantitative relation of junction transistor MN1.

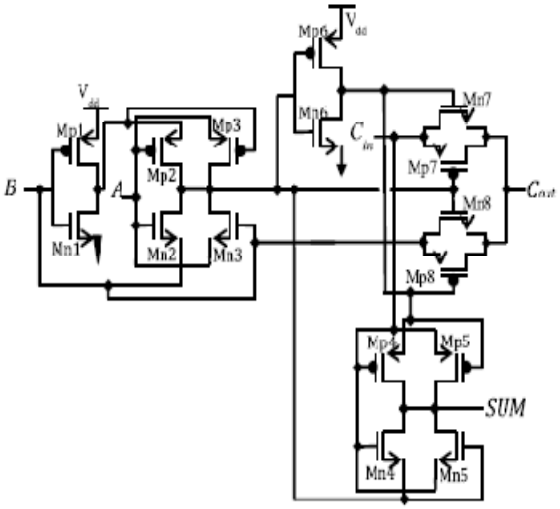

Fig 3: Proposed full adder Schematic

This full adder could be constructed over by using the 3 Modules with SUM and CARRY. The logic level could be able to combine with the structure oriented process for the reduction of the transistor count in the adder implementation. The logical structure could be combined with the proposed process of the related units OR and the PTL or TG type. The sum output from the logic of the valued stages from the each and every logical based transistor. This voltage level drop to be added in the transistor for the further reducing of the

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power and the delay combination for the aspect ratio of the related units in the proposed full adder.

Same as in the 3 Modules based full adder the Existing full adders are to be analyzed in the performance of the sectional details in the sum and the carry output. The structure consists of two XNOR modules with the extra transistors of PMOS and the NMOS coupling based transistor level operation for the full adder implementation. The voltage drop could be note down and the enabled input structure for the real valued function may be recognized in the sum and the carry units of the adder circuit. This could be gives the better delay and the power comparison of the conventional full adder circuit.

III. IMPLEMENTATION

A. RIPPLE CARRY ADDER

A ripple carry adder (RCA) could be a form of adder utilized in digital logic. A carry-look ahead adder improves speed by reducing the quantity of your time needed to see carry bits. It is contrasted with the easier, however sometimes slower, ripple carry adder that the carry bit is calculated aboard the total bit, and every bit should wait till the previous carry has been calculated to start hard its own result and carry bits (see adder for detail on ripple carry adders). The ripple carry adder calculates one or additional carry bits before the total that reduces the wait time to calculate the results of the larger price bits.

A ripple-carry adder works within the same means as pencil-and-paper strategies of addition. Beginning at the right (least significant) digit position, the 2 corresponding digits area unit additional and a result obtained. It's conjointly doable that there could also be a of this digit position (for example, in pencil-and-paper strategies, "9+5=4, carry 1"). Consequently all digit positions apart from the right got to take into consideration the likelihood of getting to feature an additional one, from a carry that has are available from consequent position to the correct.

This implies that no digit position will have associate completely final price till it's been established whether or not or not a carry is coming back in from the correct. At worst, once a full sequence of sums involves ...99999999... (In decimal) or ...11111111... (in binary), nothing is deduced the least bit till the worth of the carry coming back in from the correct is thought, which carry is then propagated to the left, one step at a time, as every digit position evaluated "9+1=0, carry 1" or "1+1=0, carry 1". it's the "rippling" of the carry from right to left that offers a ripple-carry adder its name, and its slowness. Once adding 32-bit integers, as an example, allowance needs to be creating for the likelihood that a carry to ripple through each one of the thirty two one-bit adders.

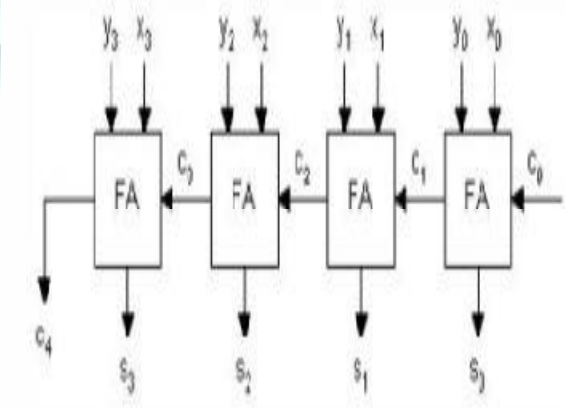

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Fig 4: Ripple carry adder

Ripple carry adder depends on 2 things:

1. Calculating, for every digit position, whether or not that position goes to propagate a carry if one comes in from the correct.

2. Combining these calculated values to be ready to deduce quickly whether or not, for every cluster of digits, that cluster goes to propagate a carry that comes in from the correct.

B. MULTIPLIER

Multiplier is a crucial part in Digital Signal process (DSP) like convolution, filtering & inner product. During this paper, a High speed & Low power religious text number is intended supported religious text arithmetic. The design of the number is predicated on the Urdhva-Triyakbhyam Sanskrit literature or "Vertical Cross Algorithm" of ancient Indian arithmetic. Similarly the adiabatic religious text number is enforced victimization Tanner EDA Tool.

The word multiplier comes from a Greek word that's wont to describe thermo dynamical processes that exchange no energy with the setting and so, no energy loss within the variety of dissipated heat. In real-life computing, such ideal method can't be achieved due to the presence of dissipative components like resistances in an exceedingly circuit. However, one can do terribly low energy dissipation by retardation down the speed of operation and solely switch transistors below sure conditions. The signal energies hold on within the circuit capacitances are recycled instead, of being dissipated as heat.

It ought to be noted that the totally adiabatic operation of the circuit is a perfect condition which can solely be approached asymptotically because the switch method is delayed. In most sensible cases, the energy dissipation related to a charge transfer event is sometimes composed of a multiplier element and a non-multiplier element. Therefore, reducing all the energy loss to zero might not potential, despite the switch speed. With the adiabatic switch approach, the circuit energies are preserved instead of dissipated as heat. Reckoning on the appliance and also the system necessities, this approach will generally be wont to cut back the ability dissipation of the digital systems.

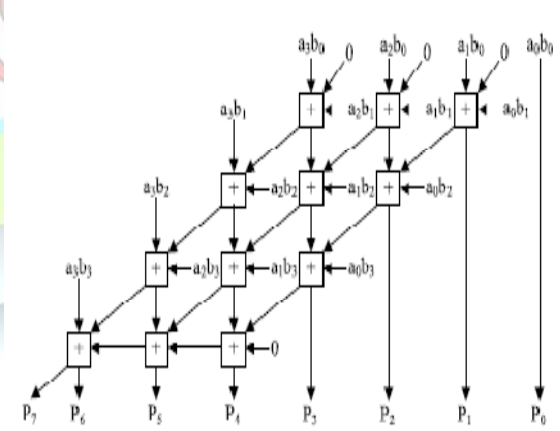

Fig 5: Multiplier Schematic

Any digital system with multiple stages/ cascades primarily based upon the delineate adiabatic power continuance theme should have a minimum of four clocks, every

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leading its previous section by 90°. Sensible adiabatic circuits use curving power clock. This is often an approximation of the tetragon undulation with the period of the hold section tending to zero.

The proposed full adder with the logical level implementation of the 3 modules for the carry look adder and the multipliers has less power consumption. This efficient implementation can also to be maintained for the low power IC manufacturing technologies in the process of all the variations.

IV. SIMULATION RESULTS

The simulation results has been analyzed and verified with the TANNER EDA tools for the further implementation. The proposed multiplier has the efficient power and the delay variations when compared with the existing system. Then we are going to implement the ripple carry adder and the multiplier. This could be also verified using this tool for the efficient implementation.

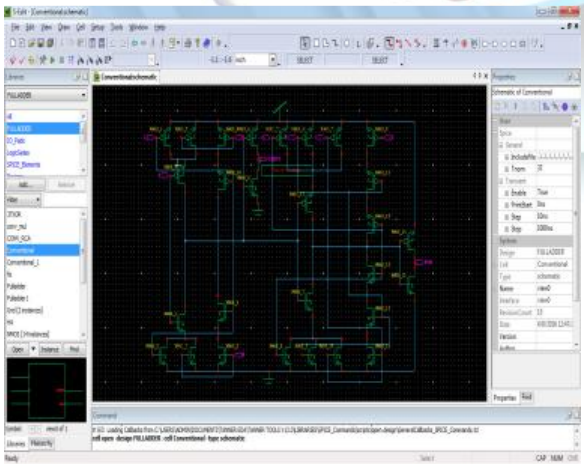

Fig 6: Schematic of the conventional full adder

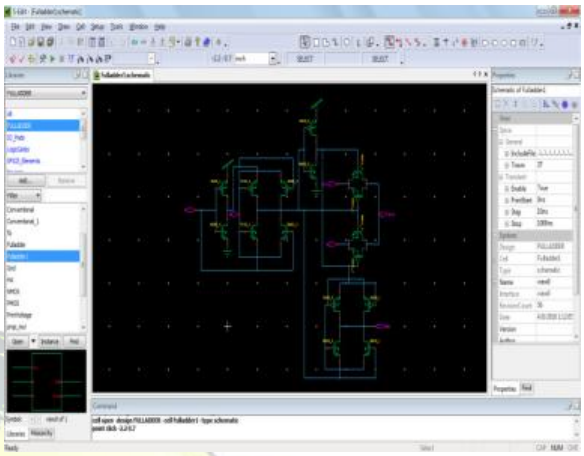

Fig 7: Schematic of the proposed full adder

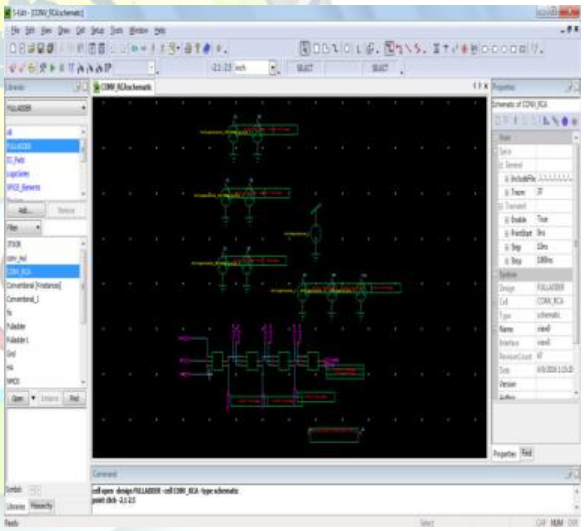

Fig 8: Schematic of the RCA

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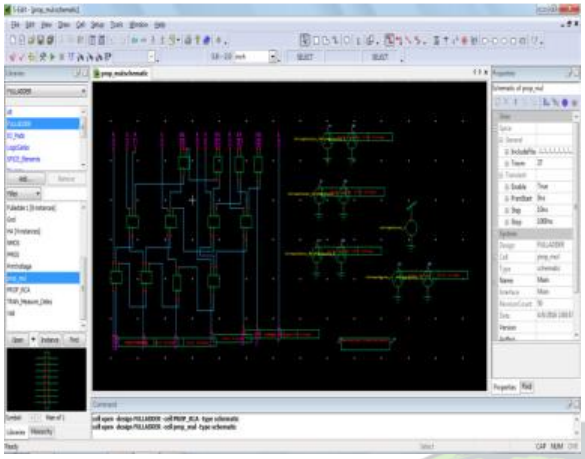

Fig 9: Schematic of the Multiplier

CIRCUIT	POWER IN WATTS	DELAY IN SEC	NM
Conventional_FA	1.510026e-002	5.0767e-008	90
Proposed_FA	5.182192e-003	3.1125e-011	90
Conventional_RCA	1.225009e-001	5.0123e-008	90
Proposed_RCA	2.072922e-002	3.0993e-011	90
Conventional_MUL	3.104424e-001	5.7500e-008	90
Proposed_MUL	5.465163e-002	5.2500e-008	90

Fig 10: Table of the schematic results comparison

V. CONCLUSION

In this paper we are presented the full adder with less number of transistors for low power consumption. This full adder can be capable of implement the ripple carry adder and the multipliers for the processors and the controllers. The specification can be made from the structure for the architecture of the proposed multipliers. The power consumption less processor can be making the IC life time larger with high reliability and stability. The entire process could be found in the RCA with 4-bit and the multiplier as 4X4. The static power could be reduced with less number of transistors for the implementation process. The verification can be made the table will be plotted.

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