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# FUZZY BASED SYMMETRIC AND ASYMMETRIC DESIGN OF NEW CASCADED MULTILEVEL INVERTER TOPOLOGY

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**ABSTRACT:**

Nowadays, use of multilevel inverters in high power applications clearly can be seen. High quality and lower distortion of the output voltage and low blocking voltage of semiconductor switches are being presented as the major privileges of the multilevel inverter compared to the traditional voltage source inverter. In our project, a new topology of multilevel inverter is proposed as fundamental block. The proposed topology is generalized using series connection of the fundamental blocks. The proposed multilevel inverter has been analyzed in both symmetric and asymmetric operation modes. A great perfection in voltage levels number with minimum switching devices has been obtained in both symmetric and asymmetric modes. Finally a computer simulation using Matlab/Simulink is presented and verifies the results.

## I. INTRODUCTION

Multilevel power converters have widely been paid special attentions because of their distinguished advantages such as possibility of high-voltage (HV) and high-efficiency operation. High quality and low distortion of output voltage and a low blocking voltage of switches can be mentioned as the important privileges of the multilevel inverter compared to the traditional voltage source inverter. Increasing the number of levels will enhance these advantages. But it should be noted that, it can impose a substantial expense due to increase the circuit complexity, and reduces the reliability and efficiency of converter. The other technical and economic aspects for the development of multilevel inverters are:

1- Modular realization
2- High availability
3- Failure management
4- Investment and life cycle cost

There are three well-known types of multilevel inverters; the neutral point clamped (NPC) multilevel inverter, the flying capacitor (FC) multilevel inverter and the cascaded H-bridge (CHB) multilevel inverter. The first generation of multilevel inverters is the NPC multilevel inverter, which has been introduced in exiting system. A flying capacitor multilevel inverter operates with independent capacitors in order to clamp the device voltage to one capacitor voltage level. The flying capacitor topology requires a large number of bulk capacitors to clamp the voltage. The CHB is based on -

-series connection of single-phase inverters with separate dc sources. Each block of the traditional CHB produces 3 voltage levels including positive, negative and zero voltages. The output voltage of CHB is obtained by summing of blocks output voltage. In recent years more attention has been paid to innovative design in multilevel inverter topologies. The number of switches, IGBT drivers and independent DC sources, power losses, complexity of control algorithm, number of levels and total harmonic distortion for output voltage waveform, voltage stress on semiconductor devices and also the rate of standing voltage for switches are the optimization subjects in new topologies.

Some other approaches have been recently suggested such as the topologies which utilize low-switching-frequency and high-power devices. Some applications of new multilevel inverters include industrial drives with efficient operation and smaller size along with low cost such as newly developed T-Type converters, flexible ac transmission systems (FACTS), and electrical vehicles. One other area of utilization for multilevel converters is the renewable photovoltaic energy systems. These structures due to the efficiency and power quality issues have been concerned by the researchers. A new topology of multilevel inverter is proposed in this paper. The suggested topology is generalized using series connection of basic blocks. Each block also can be considered as a multilevel inverter. The fundamental block and generalized topology are presented.

## II. EXISTING SYSTEM

This A cascaded multi-level inverter consists of a number of H-bridge inverter units with separate dc source for each unit and it is connected in cascade or series as shown in Fig.1. Each H-bridge can produce three different voltage levels: $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to ac output side by different combinations of the four switches S1, S2, S3, and S4.

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- The system requires H-Bridge topology for the multi-level inverter function.
- The PWM generation circuitry is somewhat is tedious to design because of this H-bridge topology.

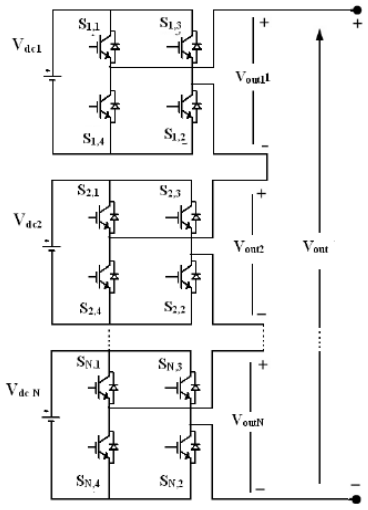


**Figure 1. Existing topology of cascaded inverter**

## III. PROPOSED TOPOLOGY

Figure 2 shows the fundamental block of proposed topology. As can be seen in Fig. 1 the basic block of proposed multilevel inverter consists of 2 dc voltage sources. Generally, the voltage sources can be unequal. If dc voltage sources have same voltages, the basic block will be analyzed in symmetric mode. In this case, the dc voltage sources are considered to be equal to ***dc V.*** The asymmetric analyzes are carried out when the dc sources have different values. The basic block includes 6 semiconductor switches. Each switch should be connected to an anti-parallel diode. As a practical solution, insulated gate bipolar transistor (IGBT) with an anti-parallel diode can be used instead of each switch and relative diode. In addition to mentioned ingredients and to have proper operation of circuit, 8 diodes should be employed. As a matter of fact, anti-parallel diodes and 8 independent diodes are undertaken conduction of backward current. Backward current is caused by inductive characteristic of load.

- The topology is cannot produce higher level of output like 49 level like our proposed system.

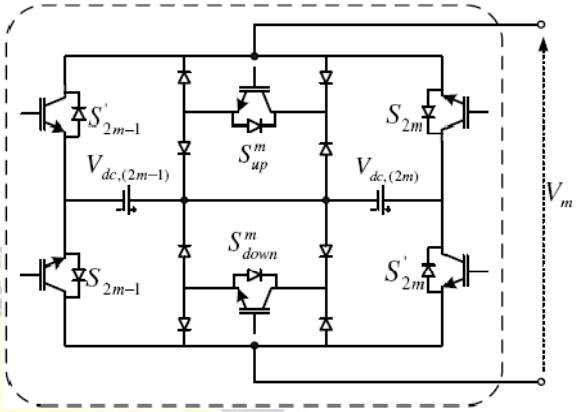


**Figure 2. Fundamental block of proposed multilevel inverter**

It is considered the depicted block is the M[th]block of a generalized multilevel inverter. Hence, if the block is supposed as first block, the names are replaced with

$$S_1, S'_1, S_2, S'_2, S'_{up}, S'_{down}, V_{dc1}, V_{dc2}, V_1$$

### A. Symmetric Mode

In symmetric mode, all dc voltage sources are equal to$V_{dc}$. The basic block can generate 5 levels in output voltage. Turning the appropriate switches on or off produces the expected level on the output voltage. It is notable that, aforementioned 5 levels are zero, 2 positive and 2 negative voltage levels. Switching pattern for symmetric operation of basic block is illustrated in Table 1.

**Table 1. Output voltage and switching states for Symmetric mode**

| State Number | Switches state | | | | | | Output voltage |
|---|---|---|---|---|---|---|---|
| | $S_{2m-1}$ | $S'_{2m-1}$ | $S_{2m}$ | $S'_{2m}$ | $S^m_{up}$ | $S^m_{down}$ | |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | $+2V_{dc}$ |
| 2 | 1 | 0 | 0 | 0 | 1 | 0 | $+V_{dc}$ |
| | 0 | 0 | 1 | 0 | 0 | 1 | |
| 3 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| | 0 | 0 | 1 | 1 | 0 | 0 | |
| | 1 | 1 | 0 | 0 | 0 | 0 | |
| 4 | 0 | 1 | 0 | 0 | 0 | 1 | $-V_{dc}$ |
| | 0 | 0 | 0 | 1 | 1 | 0 | |
| 5 | 0 | 1 | 0 | 1 | 0 | 0 | $-2V_{dc}$ |

As it can be seen in Table 1 there are redundant switching states for 3 of voltage levels. These redundancies in switching states can provide possibilities

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for average power controlling in proposed multilevel inverter in symmetric mode.

**B. Asymmetric Mode**

If the values of ***dc*** voltage sources are chosen to be different, the presented basic block is to be operated in asymmetric mode. The asymmetric mode analyzes are carried out by applying following equation to determine amount of voltage sources:

$$V_{dc(2m)} = 2V_{dc(2m-1)} (1)$$

In this case, 7 voltage levels are obtained on the output of basic block. As it was demonstrated in symmetric mode, the zero, 3 positive and 3 negative levels are generated on the output voltage of basic block in the asymmetric mode.

**C. Design of Proposed topology**

A substantial enhancement in number of output voltage levels is made by a distinct choice for values of ***dc*** voltage sources. In this mode of operation, the values are determined by considering following equations

$$V_{dc(k)} = \begin{cases} 7^{\frac{(k-1)}{2}} & for\ k: odd \\ 2 \times 7^{\frac{(k-2)}{2}} & for\ k: even \end{cases} (2)$$

In equation (2) ***k*** is ***dc*** voltage source number. The other equations for this mode can be written as below:

$$N_{level} = 7^n \quad (3)$$

$$V_{max} = +\frac{(7^n - 1)}{2} V_{dc} (4)$$

$$V_{min} = -\frac{(7^n - 1)}{2} V_{dc} (5)$$

$$N_{IGBT} = 6n \quad (6)$$

$$N_{source} = 2n \quad (7)$$

In above equations n is the total number of employed fundamental blocks.All possible states and output voltages for an asymmetric proposed multilevel inverter are shown in Table 2 for this method. As like as symmetric mode, because of organized and cascaded structure of proposed topology, all prevalent modulation methods that are applicable in multilevel inverters are applicable in asymmetric structure of proposed multilevel inverter, too.

**Table 2. Blocks state and output voltage for asymmetric proposed multilevel inverter**

| State Number | Output voltage of blocks | | | | | | Output voltage |
|---|---|---|---|---|---|---|---|
| | 1 | 2 | … | *m* | … | *n* | |
| 1 | $+3V_{dc}$ | $+2V_{dc}$ | … | $+3\times7^{m-1}$ | … | $+3\times7^{n-1}$ | $+\frac{(7^n-1)}{2}V_{dc}$ |
| 2 | $+2V_{dc}$ | $+2V_{dc}$ | … | $+3\times7^{m-2}$ | … | $+3\times7^{n-2}$ | $+\frac{(7^n-3)}{2}V_{dc}$ |
| ⋮ | … | … | … | … | … | … | ⋮ |
| $\frac{(7^n+1)}{2}$ | 0 | 0 | … | 0 | … | 0 | 0 |
| ⋮ | … | … | … | … | … | … | ⋮ |
| $7^n-1$ | $-2V_{dc}$ | $-2V_{dc}$ | … | $-3\times7^{m-2}$ | … | $-3\times7^{n-2}$ | $-\frac{(7^n-3)}{2}V_{dc}$ |
| $7^n$ | $-3V_{dc}$ | $-2V_{dc}$ | … | $-3\times7^{m-1}$ | … | $-3\times7^{n-1}$ | $-\frac{(7^n-1)}{2}V_{dc}$ |

Because of significant improvement in number of levels, this approach is scrutinized in continue. To analyze issue in details a two blocks proposed multilevel inverter is assumed.

Considering relative equations, with employing just 4 dcvoltage sources and 12 IGBTs, 49-levels are obtainable on the inverter output voltage. Regarding to equation (2) the amounts of sources can be calculated as:

$$V_{dc(1)} = V_{dc}, V_{dc(2)} = 2V_{dc}, V_{dc(3)} = 7V_{dc}, V_{dc(4)} = 14V_{dc}$$

Some operational states of supposed multilevel inverter are illustrated in Table. 3. As it can be seen from Table 3 the output voltage of second block remains constant for state number 1 to 7 while the output voltage of first block changes for 7 times and this is repeated for every 7 states. It is obvious that the semiconductor switches in second block will be switched with lower frequency rather than the first block. This can be generalized to additional blocks in asymmetric operation of proposed multilevel inverter. In practical implementation, the semiconductors of low frequency switching blocks in the multilevel inverter can be selected to be low speed switches. This can be led to a reduction in implementation expenses. Simulation results for supposed multilevel inverter are shown in Fig. 7 and Fig. 8. The *Vdc* is determined as 10*V*.

**Table 3. Blocks state and output voltage for supposed asymmetric multilevel inverter**

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| State Number | Output Voltage of Block | | Output Voltage |
|---|---|---|---|
| | 1 | 2 | |
| 1 | $+3V_{dc}$ | $+2V_{dc}$ | $+24V_{dc}$ |
| 2 | $+2V_{dc}$ | $+2V_{dc}$ | $+23V_{dc}$ |
| 3 | $+V_{dc}$ | $+2V_{dc}$ | $+22V_{dc}$ |
| 4 | 0 | $+2V_{dc}$ | $+21V_{dc}$ |
| 5 | $-V_{dc}$ | $+2V_{dc}$ | $+20V_{dc}$ |
| 6 | $-2V_{dc}$ | $+2V_{dc}$ | $+19V_{dc}$ |
| 7 | $-3V_{dc}$ | $+2V_{dc}$ | $+18V_{dc}$ |
| 8 | $+3V_{dc}$ | $+1V_{dc}$ | $+17V_{dc}$ |
| 9 | $+2V_{dc}$ | $+1V_{dc}$ | $+16V_{dc}$ |
| 10 | $+V_{dc}$ | $+1V_{dc}$ | $+15V_{dc}$ |
| 11 | 0 | $+1V_{dc}$ | $+14V_{dc}$ |
| 12 | $-V_{dc}$ | $+1V_{dc}$ | $+13V_{dc}$ |
| 13 | $-2V_{dc}$ | $+1V_{dc}$ | $+12V_{dc}$ |
| 14 | $-3V_{dc}$ | $+1V_{dc}$ | $+11V_{dc}$ |
| 15 | $+3V_{dc}$ | $+7V_{dc}$ | $+10V_{dc}$ |
| 16 | $+2V_{dc}$ | $+7V_{dc}$ | $+9V_{dc}$ |
| 17 | $+V_{dc}$ | $+7V_{dc}$ | $+8V_{dc}$ |
| 18 | 0 | $+7V_{dc}$ | $+7V_{dc}$ |
| 19 | $-V_{dc}$ | $+7V_{dc}$ | $+6V_{dc}$ |
| 20 | $-2V_{dc}$ | $+7V_{dc}$ | $+5V_{dc}$ |
| 21 | $-3V_{dc}$ | $+7V_{dc}$ | $+4V_{dc}$ |
| 22 | $+3V_{dc}$ | 0 | $+3V_{dc}$ |
| 23 | $+2V_{dc}$ | 0 | $+2V_{dc}$ |
| 24 | $+V_{dc}$ | 0 | $+V_{dc}$ |
| 25 | 0 | 0 | 0 |
| 26 | $-V_{dc}$ | 0 | $-V_{dc}$ |
| 27 | $-2V_{dc}$ | 0 | $-2V_{dc}$ |
| ⋮ | … | … | ⋮ |
| 48 | $-2V_{dc}$ | $-2V_{dc}$ | $-23V_{dc}$ |
| 49 | $-3V_{dc}$ | $-2V_{dc}$ | $-24V_{dc}$ |

**D.Fuzzy Logic Controller design**

The switching pattern selection is handled with the help of Fuzzy logic controller in this work. The process in the fuzzy inference system involves the following sections and the following figure represents the data flow inside the fuzzy inference system

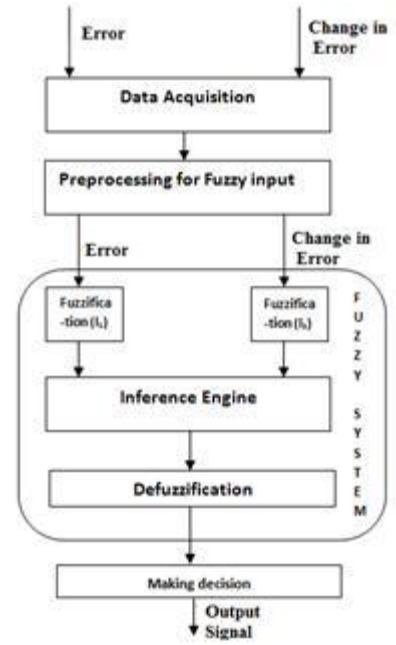


**Figure 3. Fuzzy inference system**

*i) Fuzzification*

Fuzzy logic uses linguistic variables as an alternative of numerical variables. In the real world, measured quantities are real numbers (crisp). The procedure of converting a numerical variable (real number) into a linguistic variable (fuzzy number) is called Fuzzification. It is the arrangement of input data into suitable e linguistic values or sets.

*ii) Inference method*

Fuzzy inference is a process that makes a conclusion in parallel. In accordance with this property, there is no data loss throughout the course of action and so final fault detection will be far more specific than that of conventional relaying techniques.

*iii) Defuzzification*

Defuzzification is the process of producing a quantifiable result in fuzzy logic, given fuzzy sets and corresponding membership degrees. It is typically needed in fuzzy control systems.

## IV. SIMULATION RESULTS

Fuzzy Inference system Design

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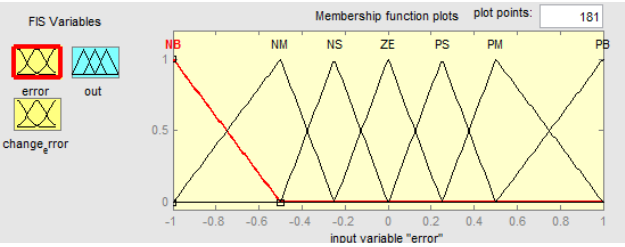


**Figure 4. Input1- fuzzy membership function**

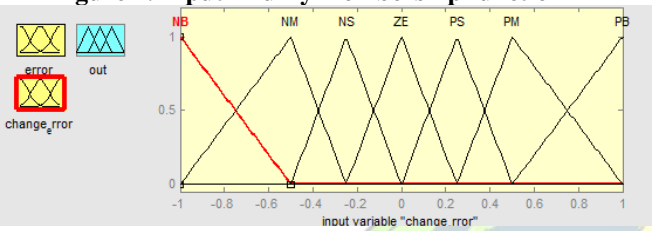


**Figure 5.Input2 - fuzzy membership function**

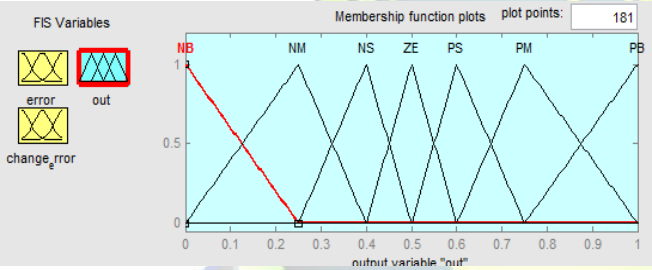


**Figure 6. Output – fuzzy membership function**

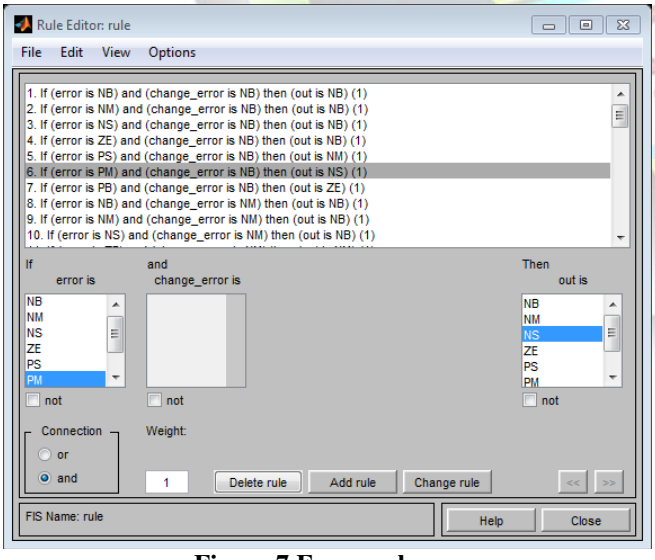


**Figure 7.Fuzzy rules**

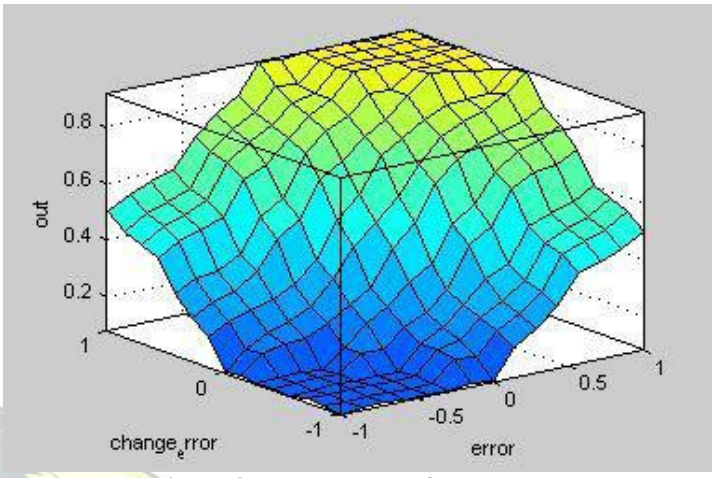


**Figure 8. Fuzzy rule surface**

**A. Simulation of symmetrical 9 level inverter:**

The following figure represents the overall topology of the 9 level inverter.

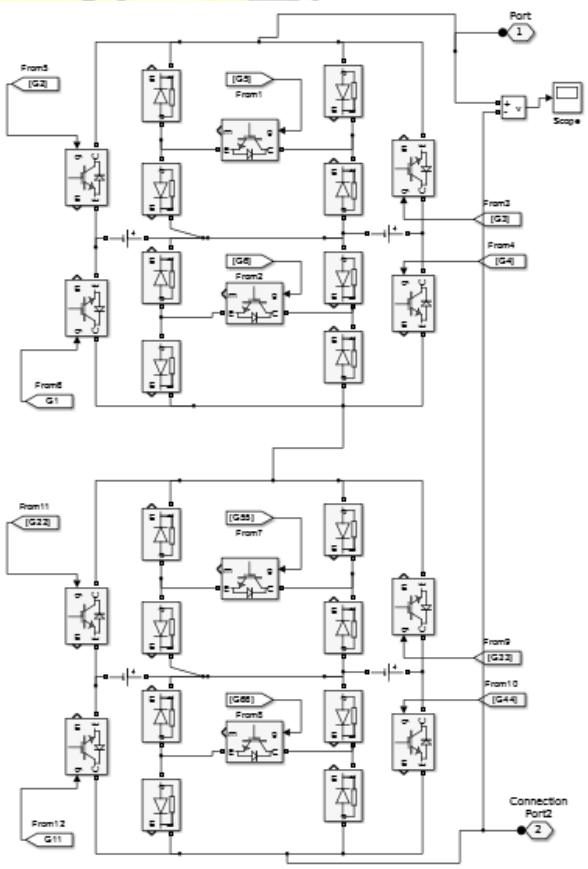


**Figure 9. Simulink model for symmetrical 9 level inverter**

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The switches of the proposed topology are switched by the sinusoidal PWM technique and the switching pattern generation block is shown in below figure. As mentioned in previous section, the symmetrical configuration can be declared with the similar voltage levels as a DC input. The following figure depicts the DC input voltage values on MATLAB Simulink.

**Table 4DC input level 9 level inverter**

| Symmetrical Design | |
|---|---|
| Vdc1 | 50V |
| Vdc2 | 50V |
| Vdc3 | 50V |
| Vdc4 | 50V |

The obtained output AC voltage is shown following figure and it clearly explains that a single waveform is having 9 levels.

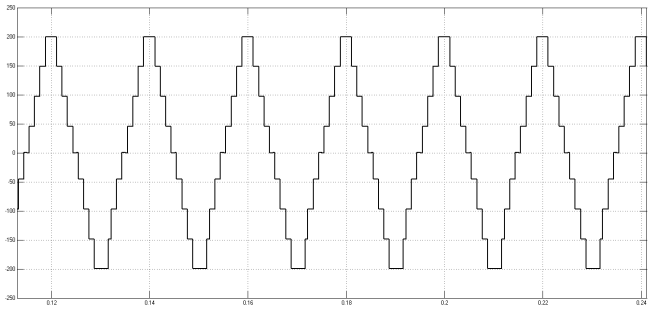

**Figure 10. Output voltage for 9 level inverter**

**B. Simulation of Asymmetrical 7 level inverter:**

The switches of the proposed topology are switched by the sinusoidal PWM technique and the switching pattern generation block is shown in below figure. As mentioned in previous section, the symmetrical configuration can be declared with the similar voltage levels as a DC input. The following figure depicts the DC input voltage values on MATLAB Simulink.

**Table 5 DC input voltage at 7 level inverter**

| Asymmetrical Design | |
|---|---|
| Vdc1 | 100V |
| Vdc2 | 200V |

The obtained output AC voltage is shown following figure and it clearly explains that a single waveform is having 7 levels.

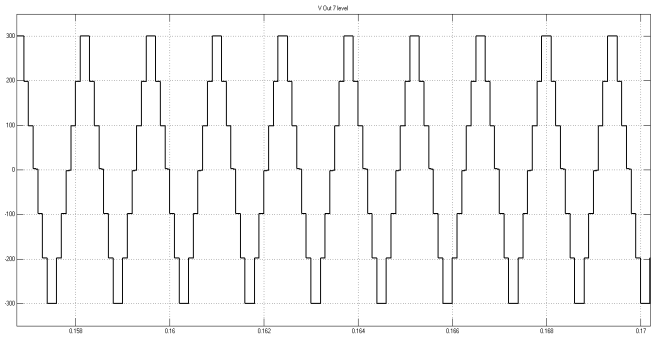

**Figure 11. Output voltage for 7 level inverter**

**C. Simulation of Asymmetrical 49 level inverter:**

The switches of the proposed topology are switched by the sinusoidal PWM technique and the switching pattern generation block is shown in below figure. As mentioned in previous section, the symmetrical configuration can be declared with the similar voltage levels as a DC input. The following figure depicts the DC input voltage values on MATLAB Simulink.

**Table 6. DC input voltage for 49 level inverter**

| Asymmetrical Design | |
|---|---|
| Vdc1 | 10V |
| Vdc2 | 20V |
| Vdc3 | 70V |
| Vdc4 | 140V |

The obtained output AC voltage is shown following figure and it clearly explains that a single waveform is having 49 levels.

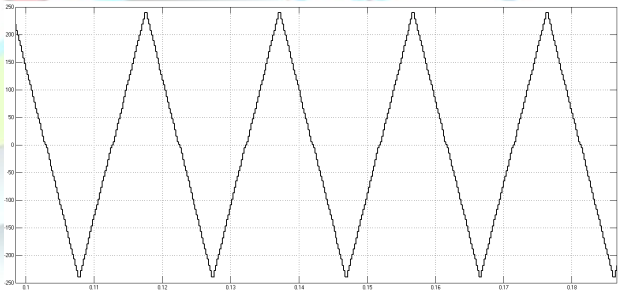

**Figure 12. Output voltage for 49 level inverter**

## V. CONCLUSION

A new multilevel inverter topology has been proposed in this project. The proposed topology has superior features over conventional and recently published new topologies in terms of the required power semiconductor switches, isolated dc supplies, number of output voltage level, driver number, total power losses and cost. Because of substantial increase in voltage levels with less

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semiconductor switches this topology can be a good candidate for converters used in power applications especially in high voltage applications. In the mentioned topology, the switching operation is separated into high and low frequency parts. The implemented multilevel circuit has been tested in 3 different operation modes. Hence the simulation and experimental results of the developed prototype for 7-level, 9-level and 49-level operation modes are simulated in the project.

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