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LEAKAGE CURRENT REDUCTION IN GRID-CONNECTED PV MULTI LEVEL INVERTERS

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***Abstract*— A hybrid multicarrier pulse width modulation (H-MCPWM) technique is proposed to reduce leakage current in a transformerless cascaded multilevel inverter for photovoltaic (PV) systems. The proposed system has the advantages of simple structure, low weight and provides higher efficiency. However, the topology operates by making a path for leakage current to flow through parasitic capacitance formed between the PV module and the ground. The proposed H-MCPWM technique ensures low leakage current in the transformerless PV inverter system with simplicity in implementation of the modulation technique using lesser number of carriers.**

***Index Terms*—Cascaded H-bridge multilevel inverter, hybrid multicarrier pulse width modulation (H-MCPWM), leakage current reduction, photovoltaic (PV) system with no transformer.**

I. INTRODUCTION

The total power generation from the photovoltaic (PV) system is relatively small as compared to other common energy resources due to its high installation cost. One of the solutions to reduce the cost of the PV power system is to remove transformer required in the output of the PV inverter [1]–[3]. In the last years, multilevel converter topologies have been also considered in PV applications. However, the use of transformers increases weight, size, and cost of the PV system, and reduces the power conversion efficiency. This has motivated the research community to work in the transformerless PV system. The advancement of power electronics technology has made the use of transformerless PV inverter popular in kilo watt (kW) range [4], [5]. However removal of the transformer introduces harmful leakage current to flow through the parasitic capacitance which exists between the PV module and the ground. This leakage current may increase the system losses, total harmonic distortion in the grid current, electromagnetic inferences, and safety concerns [6]–[9]. The factors used to limit magnitude of the common mode voltage include nature of the output pulse width of the inverter, number of commutation, and grounding of the PV system [10].

Next-generation PV inverter has reached higher power ratings with modularity, and redundant topologies will be adopted in the design for reliability of the inverter. Among various multilevel inverters, cascaded H-bridge multi-level inverter has various advantages compared to other topologies [13]. This use of cascaded H-bridge multilevel inverter opens up the option to eliminate the transformer from the PV system. In general, following two well-established modulation techniques are available for the multilevel inverter topologies which provide constant common mode voltage: space vector modulation (SVM) and multicarrier pulse width modulation (MCPWM). In [14] the author has demonstrated the use of SVM to reduce the leakage current in transformer-less PV inverter topology by placing zero active vectors at appropriate switching instants. However, selection of switching states is not easy for practical

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implementation. The MCPWM technique eliminates the problem of common mode voltage applied in the neutral clamped multilevel inverter, which in-creases the computational burden due to more number of carrier signals [15].

This model uses a hybrid multicarrier pulse width modulation (H-MCPWM) technique to reduce leakage current in transformerless cascaded H-bridge multilevel inverter for PV systems. When the common mode voltage changes in a large step value, it induces high leakage current in the PV system through the parasitic capacitance between the PV module and the ground. The reduced voltage transition in the common mode voltage reduces the leakage current. It is easy to implement the proposed modulation technique without much complexity and require half the number of carriers as required in the conventional MCPWM techniques.

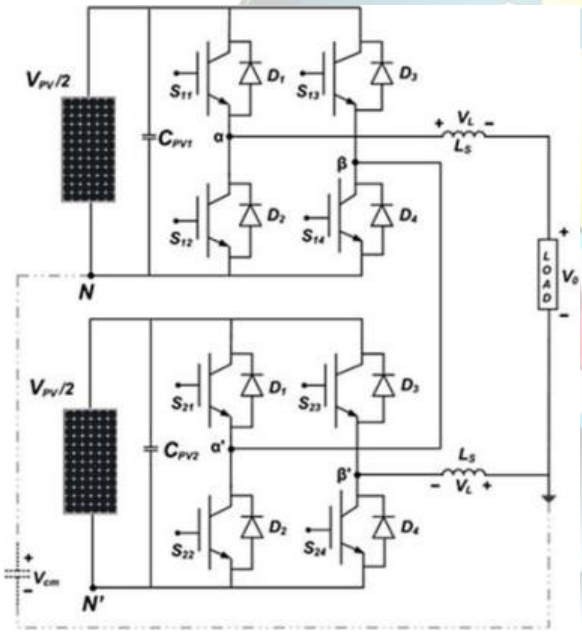

Fig.1. PV-supported transformerless single-phase five-level cascaded multi-level inverter

II. CONSTANT COMMON MODE VOLTAGE

The detailing of fig 1, showcases configuration of two cascaded H-bridges adding the output voltage of the upper and lower bridges to generate five-level stepped output voltage at the ac side, i.e., V_{PV}, $V_{PV}/2$, 0, $-V_{PV}/2$, and $-V_{PV}$. It is assumed that the grid does not contribute common mode voltage in the system [9]. The converter topology and modulation method have significant contribution in leakage current generation. Therefore, a simple resistive load for the proposed system is used for evaluation of the proposed modulation technique. The leakage current is generated in the parasitic capacitance formed between the PV module and the ground, where common mode voltage is also induced at the same point as shown in Fig. 1. The common mode voltage of any electrical circuit is the mean value of voltage between the outputs and a common reference point.

The negative terminal of the dc bus, i.e., terminal N is called here as common reference point for upper H-bridge inverter. Similarly, for lower H-bridge inverter, N^- is the common reference point. The parasitic capacitance formed for the lower H-bridge and upper H-bridge is assumed to be the same, be-cause both the H-bridges are supplied from the similar rated PV modules [11]. The common mode voltage (CMV) and leakage current in the two H-bridges are also same; hence, the capacitive currents flow from point N to ground and N^- to ground is considered equal. The common mode voltage V_{cm} for the upper full-bridge (H-bridge) inverter is defined as follows [3]:

$$V_{cm} = (V_{\alpha N} + V_{\beta N}) / 2 \quad (1)$$

VαN and VβN are the voltages between the mid-point of the upper H-bridge inverter legs to the negative terminal of the dc link, $V_{\alpha'\beta'}$ is the voltage between the mid points of the two legs of the lower H-bridge inverter, and let Vo is the output voltage across the load.

$V_{\alpha N}$ and $V_{\beta N}$ are the voltages between the mid-point of the upper H-bridge inverter legs to the negative terminal of the dc link, Vα' β ' is the voltage between the mid points of the two legs of the lower H-bridge inverter, and let Vo is the output voltage across the load. The leakage current mainly depends upon the magnitude of the inverter common mode voltage. In order to derive the expression of the common mode voltage in the cascaded multilevel inverter, the following equations can be written from Fig. 1:

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$$V_{cm} + V_{\alpha N} - V_L - V_O = 0 \quad (2)$$

$$V_{cm} + V_{\beta N} + V_L - V_{\alpha'\beta'} = 0 \quad (3)$$

The expression of the common mode voltage can be obtained in (4) by adding (2) and (3) as follows:

$$2V_{cm} + V_{\beta N} + V_{\alpha N} - V_{\alpha'\beta'} = 0. \quad (4)$$

Using (4), the CMMV can be expressed as follows:

$$V_{cm} = (V_{\alpha'\beta'} - V_{\alpha N} - V_{\beta N}.) / 2 \quad (5)$$

The proposed H-MCPWM is the modified version of the phase opposite disposition (POD) pulse width modulation technique, where the number of carriers required is half of that required in POD PWM and therefore computational burden is reduced. In this modulation method, the carrier signals used are in-phase with each other. The phase of all the carriers is shifted by 180°after each half-cycle. Table I shows the different switching instants and their corresponding magnitude of CMV. It has six switching instants, in which one instant has zero CMV, three instants have $2V_{PV}/4$, and two instants have $V_{PV}/4$, CMV. There is no voltage transition in zero CMV. The CMV may take the values depending upon the inverter switch states selected since the voltage-source inverter cannot provide pure sinusoidal voltages and has discrete output voltage levels synthesized from the output voltage of the PV [10]. The voltage transition depends upon the direction of the current in the inverter; hence, the proposed H-MCPWM modulation technique ensures the reduced common mode voltage generation in the band limit of maximum $\pm V_{PV}/4$.

TABLE I
SWITCHING INSTANTS OF THE H-MCPWM TECHNIQUE FOR CONSTANT COMMON MODE VOLTAGE

Logic conditions	*Switches on upper H-bridge*				*Switches on lower H-bridge*				*Common mode voltage*
Mode-1: (0 to T/2)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	V'_{cm}
$V_{c1} > V_{ref} < V_{c2}$	1	1	0	0	0	0	1	1	$2V_{PV}/4$
$V_{c1} > V_{ref} > V_{c2}$	0	1	0	1	0	0	1	1	$V_{PV}/4$
$V_{c1} < V_{ref} > V_{c2}$	0	0	1	1	0	0	1	1	$2V_{PV}/4$
Mode-2: (T/2 to T)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	–
$V_{c2} > V_{ref} < V_{c1}$	1	1	0	0	0	0	1	1	$2V_{PV}/4$
$V_{c2} > V_{ref} > V_{c1}$	1	1	0	0	1	0	1	0	$V_{PV}/4$
$V_{c2} < V_{ref} > V_{c1}$	1	1	0	0	1	1	0	0	0

A. Mode-1 (0 to T/2)

In this mode, all the carrier signals are in-phase with each other, the three-level voltages, i.e., 0, $-V_{PV}/2$, and $-V_{PV}$, is generated using following switching scheme:

1) When the reference signal V_{ref} is smaller than the carrier signals V_{c1} and V_{c2}, then the switches S_{11}, S_{14}, S_{23}, and S_{22} are turned ON and the complimentary switches, S_{13}, S_{12}, S_{21}, and S_{24}, are turned OFF. In this situation $V_{\alpha N} = V_{PV}/2$, $V_{\beta N} = 0$, and the output voltage is $V_{\alpha\beta} = +V_{PV}/2$.

2) When the reference signal V_{ref} is greater the carrier signal V_{c2} , and lesser than the carrier signal V_{c1} , then the switches S_{14}, S_{12}, S_{23}, and S_{22} are turned ON and the complimentary switches S_{11}, S_{13}, S_{21}, and S_{24} are turned S_{11}, S_{13}, S_{21}, and S_{24} are turned OFF. In this situation $V_{\alpha N} = 0$, $V_{\beta N} = 0$, and the output voltage is $V_{\alpha\beta} = 0$.

3) When both the carrier signals, $V_{c1}$and V_{c2}, are smaller than the reference signal V_{ref}, then the switches, S_{13}, S_{12}, S_{23}, and S_{22}, are turned ON and the complimentary switches, S_{11}, S_{14}, S_{21}, and S_{24}, are turned OFF. In this situation $V_{\alpha N} = 0$, $V_{\beta N} = V_{PV}/2$, and the output voltage is $V_{\alpha\beta} = -V_{PV}/2$.

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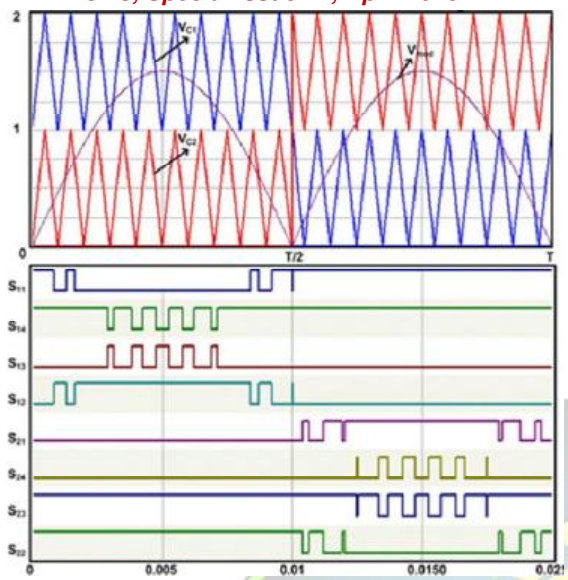

Fig 2: Switching pattern of the proposed H-MCPWM technique for the five levels cascaded multilevel inverter.

B. Mode-2 (T/2 to T)

In this mode, all the carrier signals are phase shifted by 180°,the three-level voltages, i.e., 0, +VPV/2, and +VPV, are generated using following switching scheme.

1) When the reference signal Vref is smaller than the carrier signals V_{c1} and V_{c2}, then the switches, S_{11}, S_{14}, S_{23}, and S_{22}, are turned ON and the complimentary switches, S_{13}, S_{12}, S_{21}, and S_{24}, are turned OFF. In this situation $V_{\alpha', N'} = 0$, $V_{\beta', N'} = +V_{PV}/2$, and the output voltage is $V_{\alpha', \beta'} = -V_{PV}/2$.

2) When the reference signal V_{ref} is greater the carrier signalsV_{c1}, and lesser than the carrier signal V_{c2}, then the switches, S_{11}, S_{14}, S_{21}, and S_{23}, are turned ON and the complimentary switches, S_{13}, S_{12}, S_{22}, andS_{24}, are turned OFF. In this situation $V_{\alpha', N'} = +V_{PV}/2$, $V_{\beta', N'} = +V_{PV}/2$, and the output voltage is $V_{\alpha', \beta'} = 0$. When both the carrier signals, V_{c1} and V_{c2}, are smaller than the reference signal V_{ref}, then the switches, S_{11}, S_{14}, S_{21}, and S_{24}, are turned ON and the complimentary switches, S_{13}, S_{12}, S_{23}, and S_{22}, are turned OFF. In this situation $V_{\alpha', N'} = V_{PV}/2$, $V_{\beta', N'} = 0$, and the output voltage is $V_{\alpha', \beta'} = +V_{PV}/2$.

III. SIMULATION ANALYSIS AND WAVEFORMS

The circuit diagram used to show the reduction of leakage current in the PV system which flow through the parasitic capacitor existing between the PV module and the ground, and its remedy is mentioned as simulation circuit diagram in figure below. It is MATLAB prepared circuit diagram for simulation to shown the reduced leakage current.

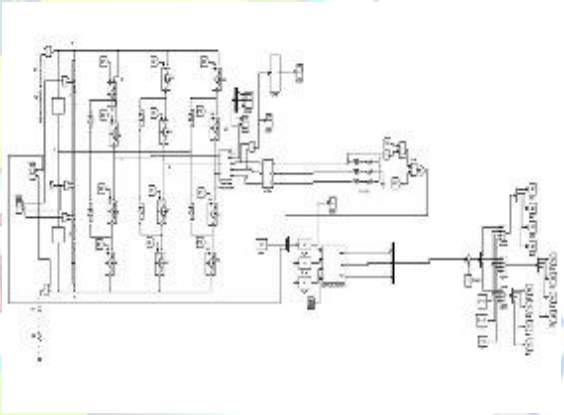

Fig3: The simulation circuit using MATLAB

The parameters used in simulation are: PV output voltage of 120 V across the dc link of each H-bridge, parasitic capacitance (0.1 μF), modulation index (0.9), filter inductance (1.8 mH), and load (20 Ω). The table clearly shows the advantage of the proposed H-MCPWM as compared to the other multicarrier PWM techniques. Also the proposed H-MCPWM has less computational burden, as compared to the conventional MCPWM.

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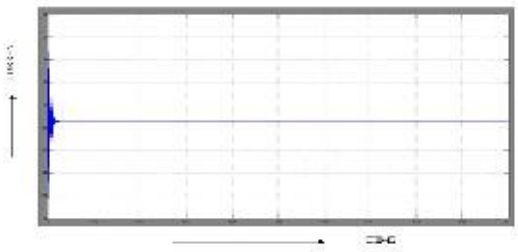

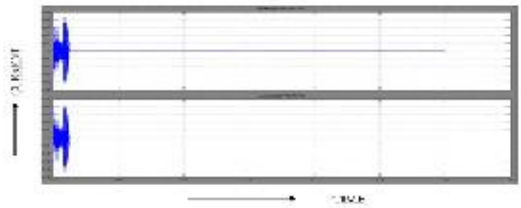

Fig 4: Unsuppressed and suppressed leakage current waveforms

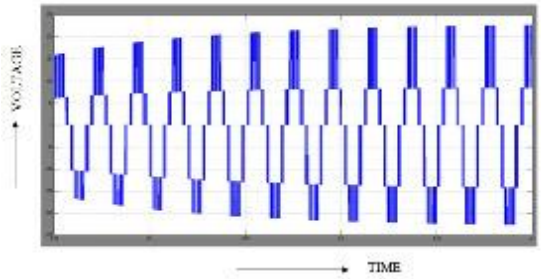

Fig 5: Output voltage waveform

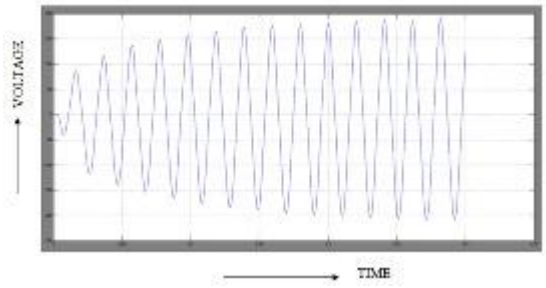

Fig 6: Filtered output voltage waveform

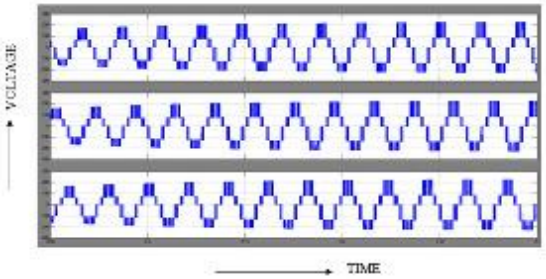

Fig 7: Inverter three phase voltage waveform

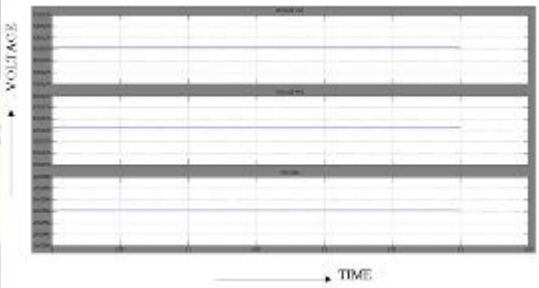

Fig 8: PV voltage waveform

IV. CONCLUSION

In this dissertation, new cost-effective and high-performance inverter topologies and advanced inverter control systems were researched and developed a software model for the next generation PV systems.

The ground leakage current issue in CMI-based PV system was studied. The removal of the transformer resulted in galvanic connections among the grid and the separate PV panels/ strings interfaced with different cascaded inverters. The inter-module leakage current loop formed among the cascaded inverter modules is a unique feature for PV CMI. It prevents the existed string inverter leakage current suppression techniques to be directly applied in the PV CMI. A filter-based leakage current suppression method, which is suitable for the cascaded inverter with high switching frequency, was presented. It was successfully applied in the PV cascaded inverters simulation circuit. The suppression filters utilized in the two solutions can be designed based on the simplified leakage current analytical models. The design results from the derived models were

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consistent with the simulation results. Simulation results were provided to validate the effectiveness of the proposed leakage current solutions.

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